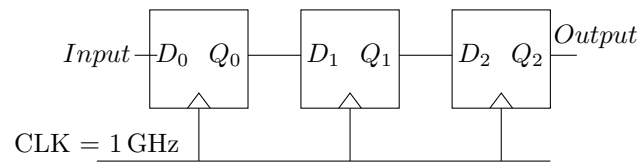# GATE EC 2023

Hemant

October 2023

1. The synchronous sequential circuit shown below works at a clock frequency of $1\,\text{GHz}$. The throughput, in $\text{Mbit}\,\text{s}^{-1}$ and the latency, in ns, respectively, are

(a) $1000, 3$

(b) $333.33, 1$

(c) $2000, 3$

(d) $333.33, 3$

<div align="right">(GATE EC 2023)</div>