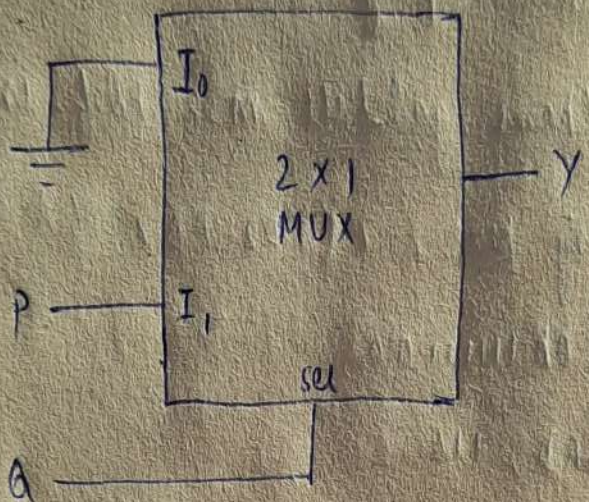
21-11-2023

FPGA

.V → file
[Ex → fhgs.V]

GATE EC 2023

Q23. In the circuit shown below, P & Q are the inputs. The logical function realized by the circuit shown below is.



(a) $Y = PQ$ (b) $Y = P + Q$ (c) $Y = \overline{PQ}$ (d) $Y = \overline{P+Q}$

SOLUTION:-

$$\text{output} = \bar{Q} \cdot I_0 + Q \cdot I_1$$

$$= \bar{Q} \cdot 0 + Q \cdot P$$

$$= PQ$$

$\therefore Y = PQ$ option (a) $Y = PQ$ //

→ FPGA
→ ALM
→ ESP

ESP