Holden Sandlar

Advanced Computer Architecture

A Survey of Multi-core Processors

The goal of this paper was to compile a general overview of the features of today's multi-core processors and then analyze some of the more common processors for their specific applications. Every engineer knows that it is crucial to specify the system requirements of the application being designed for. By assessing the characteristics of different processors in the market today this paper guides the reader to understanding when/why to select a given design. The main focus of the analysis in the paper is on the application domain, power to performance ratio, processing elements, memory system, and accelerators/integrated peripherals (ASICs).

The first section of the paper defines the analysis of each of the aforementioned specifications. They note that there are several markets within computer architecture in which designers can specifically tailor to. Among those markets are embedded/real-time which require extremely low power, general purpose (varying power depending on the specific chip), and high end computing (typically high power – warehouse scale is mentioned). Complexities in architectural layout are also discussed with regard to SIMD and VLIW ISA's as well as typical memory hierarchy and coherence strategies. One of the more interesting points from this section of the paper is in relation to the two consistency models of the memory system (weak and sequential). "Weak consistency models make the memory system easier to design but place an onus on the programmer to correctly identify and place instructions in the program that enforce proper behavior "… "sequential consistency makes programming easier but makes the memory system more complicated and slower as it is unable to take advantage of performance gains that can be had by allowing memory operations to complete out-of-order."

The next section of the paper picks a number of different cores in the market today and looks at their specific architectural and application characteristics. Among these cores are a few DSP processors, a couple of general purpose mobile cores (focus is on low power consumption), an Nvidia high performance graphics core, and the Intel Core i7 general purpose core. Of the analysis done I took particular interest in the Core i7, mainly because it is Intel's latest high performance consumer processor. It was unsurprising the learn that the i7 is implemented with eight out-of-order , two-way symmetric multithreading cores. However, I was very surprised to learn that the i7 implements a broadcast cache-coherency memory system. Prior to reading this paper I would have expected the i7 to implement a directory based protocol for inter-core communication/memory coherence/management in order to save bus bandwidth and obtain higher throughput. Overall though, the i7 is reported as a chip which is highly capable in a variety of applications as long as power isn't a constraint. One other interesting note worth mentioning is a quote from the discussion on cache coherency – "It is not uncommon for multicore designs to omit cache coherence to reduce design and verification complexity." While I understand the challenges of designing cache coherent systems I find it somewhat surprising that some companies choose to ignore the issue all together. Because of the increased difficulty when programming for such a system I would assume that many designers steer clear of such architectures. I would be interested to see another paper comparing these architectural decisions with consumer price points and market response for various chips.