

Jumpers and Stuff

Signal Glossary

Connectors

Revision History

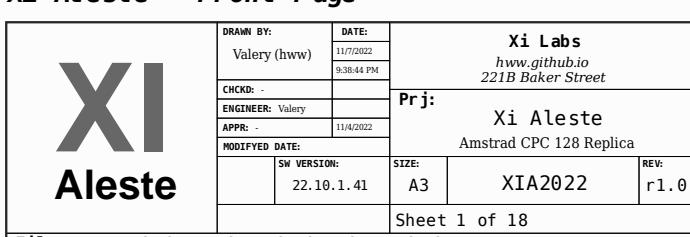
REF	DESCRIPTION	APPRV1	APPRV2	MANAGER

ECO Log

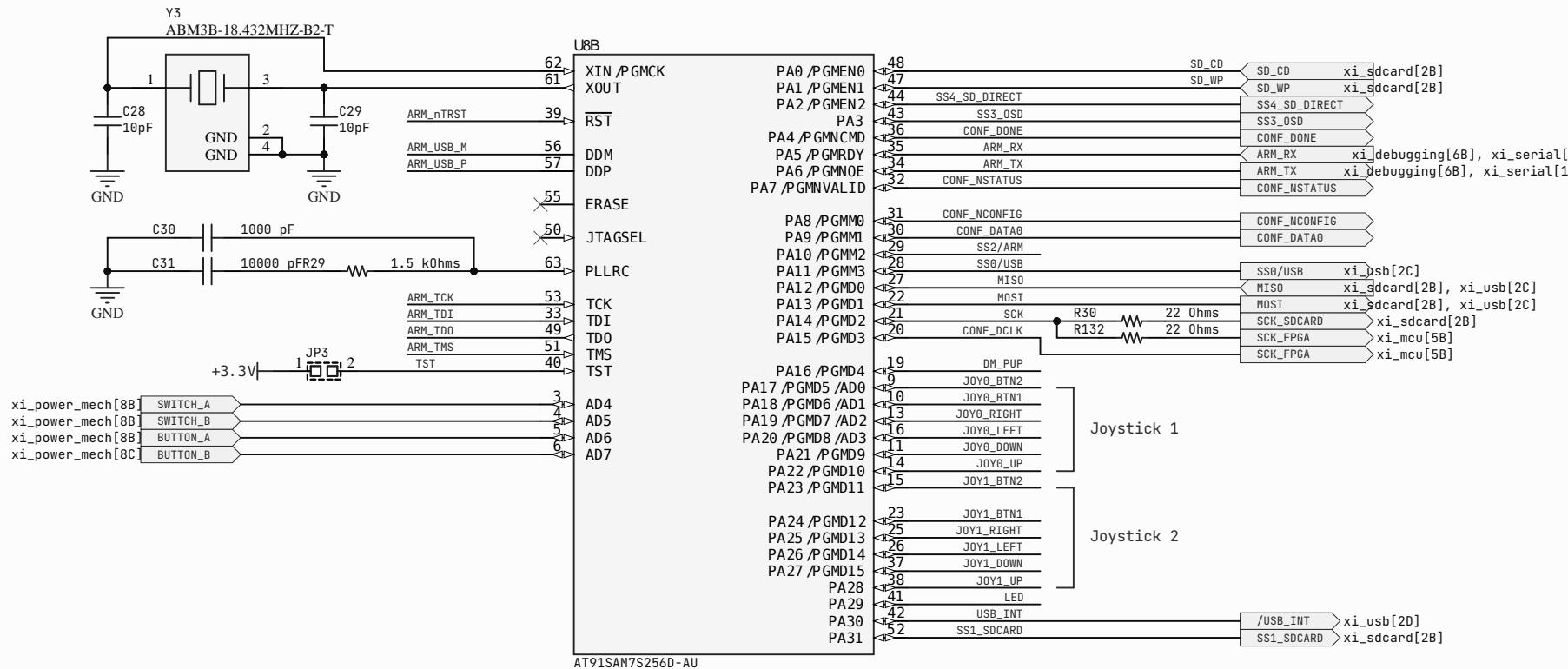
ECO NUMBER	DESCRIPTION	DATE

Key Components

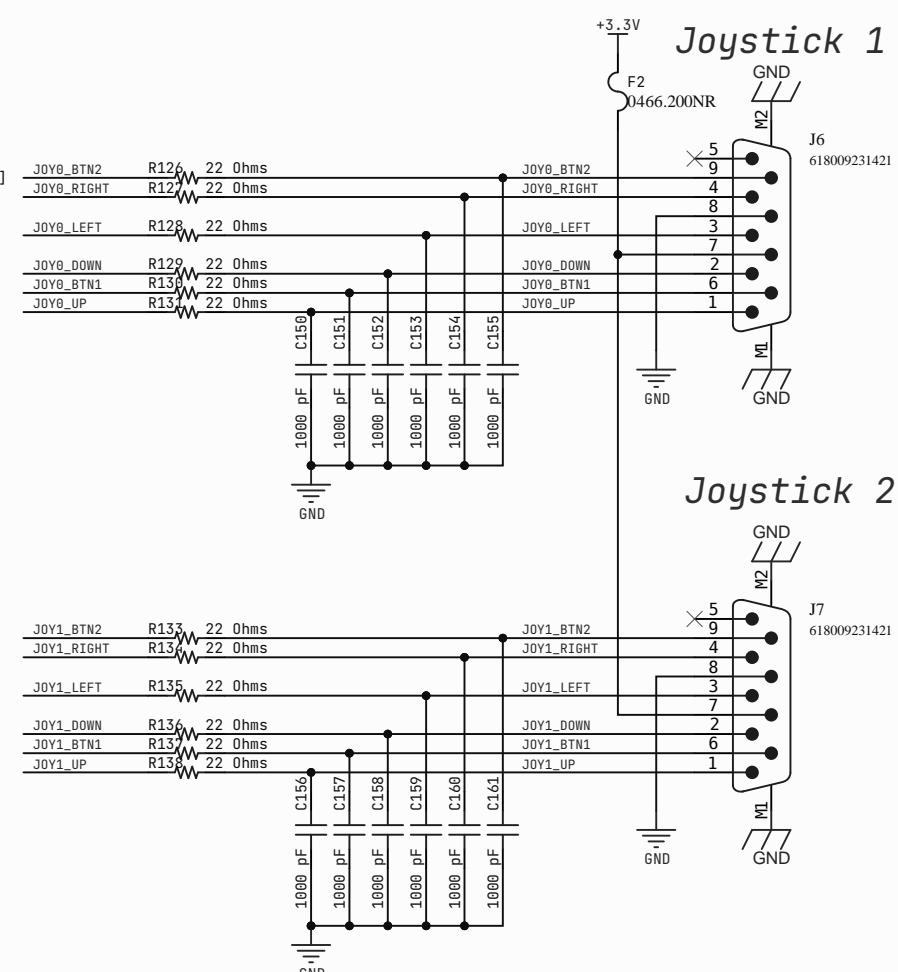
Xi Al este - Front Page



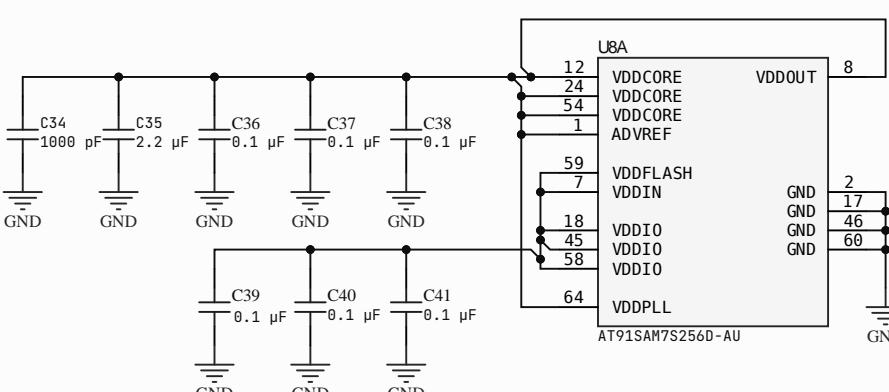
MICROCONTROLLER



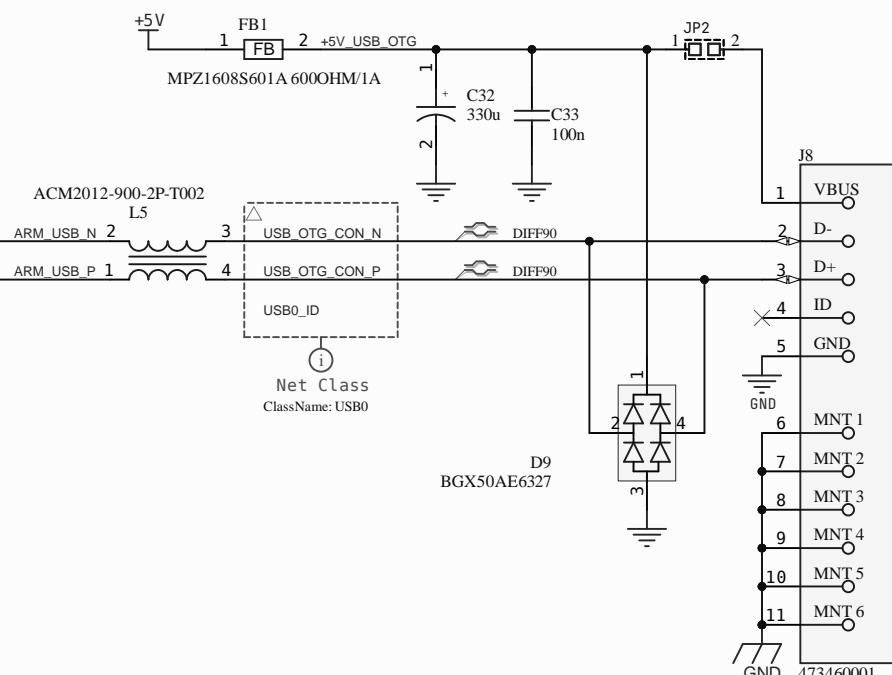
GAME CONTROLLERS



MCU DECOUPLING



MCU PROGRAMMING USB



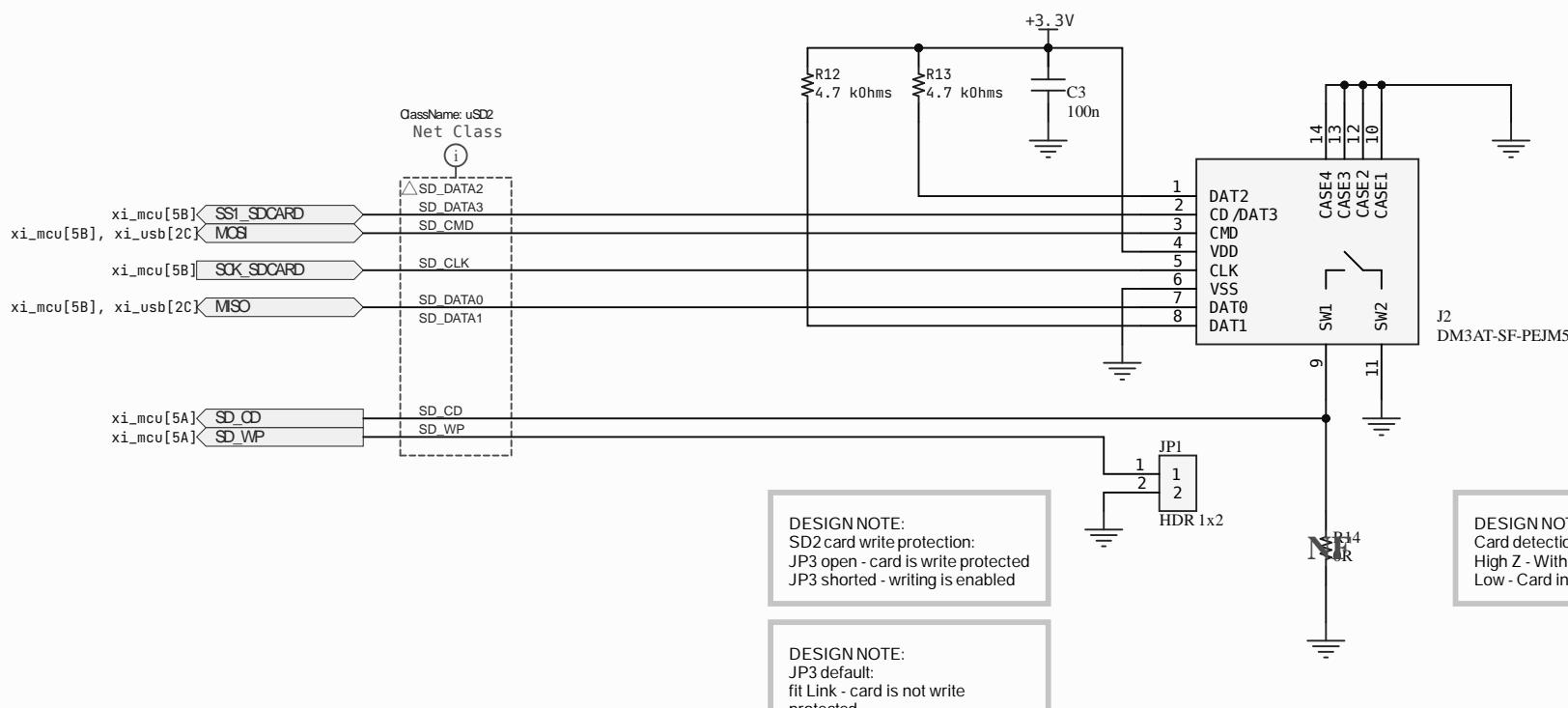
xi A este - Microcontroller



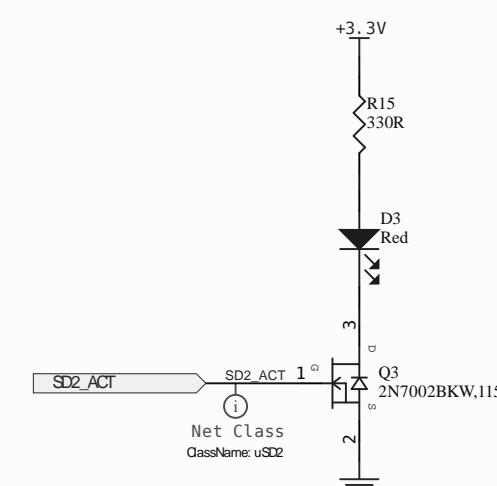
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	Valery (hwv)	11/7/2022	hwv.github.io		
		9:38:44 PM	221B Baker Street		
	CHKD:	-	Prj:	Xi Aleste	
	ENGINEER:	Valery			
	APPR:	-			
MODIFIED DATE:		11/7/2022	Amstrad CPC 128 Replica		
	SW VERSION:	SIZE:			REV:
	22.10.1.41	A3	XIA2022		r1.0
Sheet 2 of 18					

Xi Aleste - SD Card

Micro SD



Micro SD Activity LED



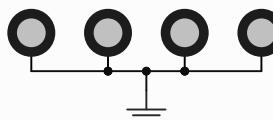
Xi Aleste - SD Card

XI Aleste	DRAWN BY: Valery (hww)	DATE: 11/7/2022 9:38:45 PM	Prj: Xi Aleste Amstrad CPC 128 Replica	Xi Labs hww.github.io 221B Baker Street	
	CHKD: -	ENGINEER: Valery		SIZE: A3	REV: r1.0
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				Git Hash: Version control disabled	Sheet 3 of 18

Mechanical

MOUNTING HOLES

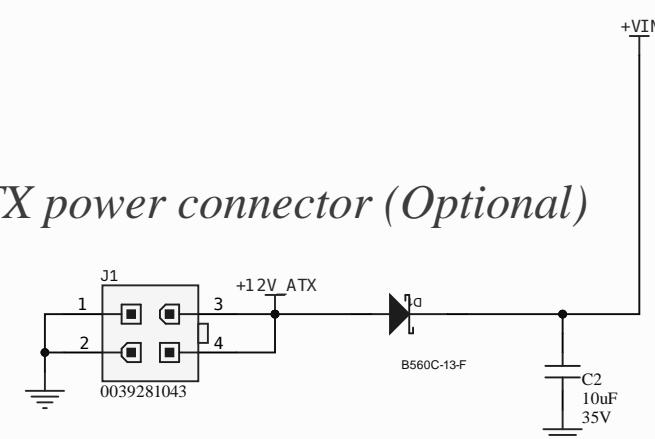
MH1 MH2 MH3 MH4



Mounting holes 7.4mm pad 3.2mm drill
BOARD MOUNTING HOLES
ONE IN EACH CORNER

POWER INPUT

ATX power connector (Optional)



DESIGN NOTE:
For automotive application use ATX connector. You can for example place all the required protections on a separate board (e.g. load dump protection) and then connect this baseboard.

DESIGN NOTE:
If ATX connector is used for supplying baseboard with power, fit D17 and C197. If it is used as power output then fit D20 and C197. Do not fit both diodes at once!

DESIGN NOTE:
If +12V is required by PCIe Card or LVDS Backlight inverter, use ATX connector to power the baseboard.

DESIGN NOTE:
Optional: A 2.5" hard drive can be supplied from this connector (requires only +5V power). Use standard SATA power cable and fit the correct ATX connector on the Baseboard.

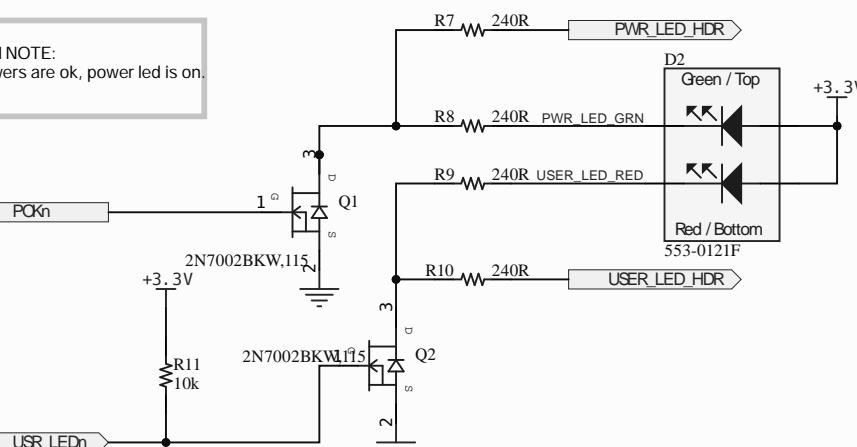
LEDs

Power & Use LEDs

GROUND TEST POINT

TPI
TP-25MILC

DESIGN NOTE:
If all powers are ok, power led is on.



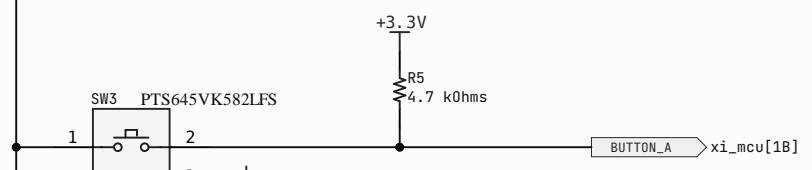
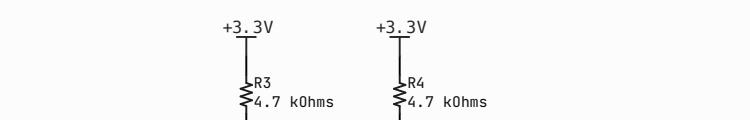
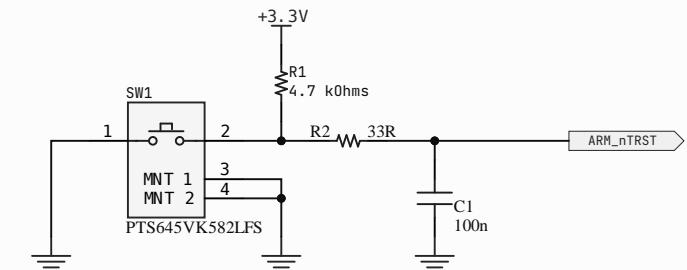
FIDUCIALS

FIDICLALS 4x TOP
FID1 FID2 FID3 FID4 FID5 FID6 FID7 FID8



BUTTONS

Reset Button



Xi Aleste - Power & Mechanics

	DRAWN BY: Valery (hww)	DATE: 11/7/2022 9:38:45 PM	Xi Labs hww.github.io 221B Baker Street
	CHKD: -	ENGINEER: Valery	
APPR: -	APPRAISAL DATE: 11/7/2022	MODIFIED DATE: 22.10.1.41	Prj: Xi Aleste Amstrad CPC 128 Replica
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A

B

C

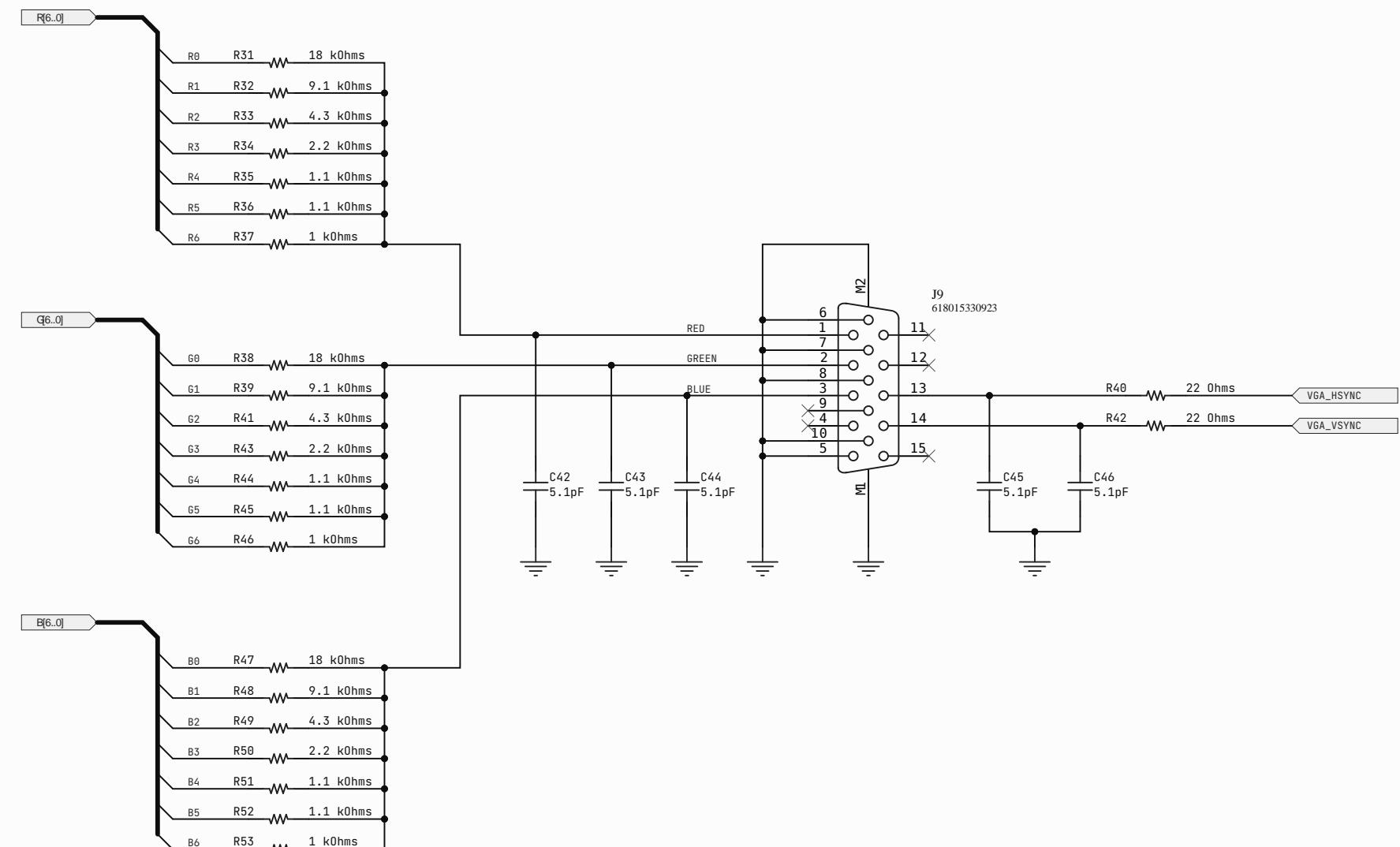
D

A

B

C

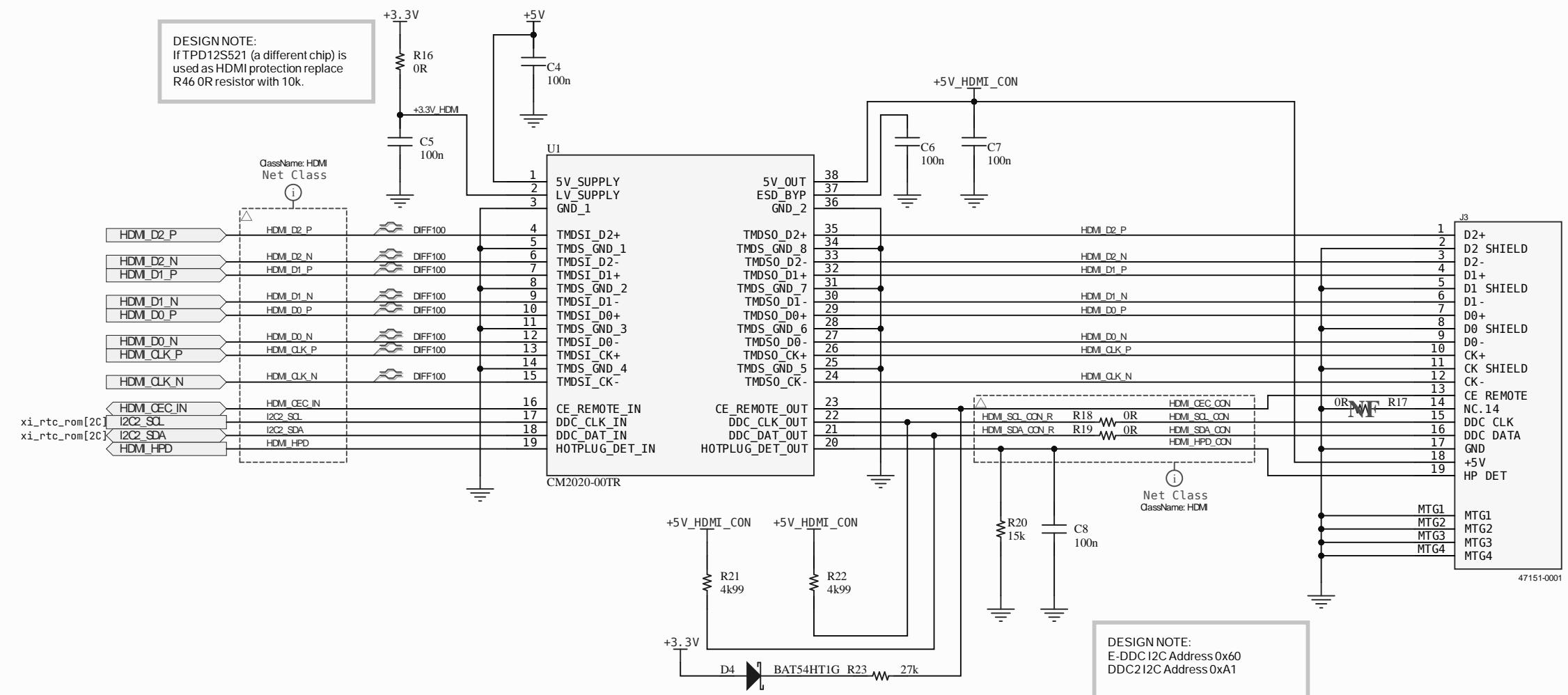
D



Xi Aleste - VGA Video output

	DRAWN BY: Valery (hww)	DATE: 11/7/2022 9:38:45 PM	Xi Labs hww.github.io 221B Baker Street			
Prj:	Xi Aleste Amstrad CPC 128 Replica					
CHKD:						
ENGINEER:	Valery					
APPR:	11/7/2022					
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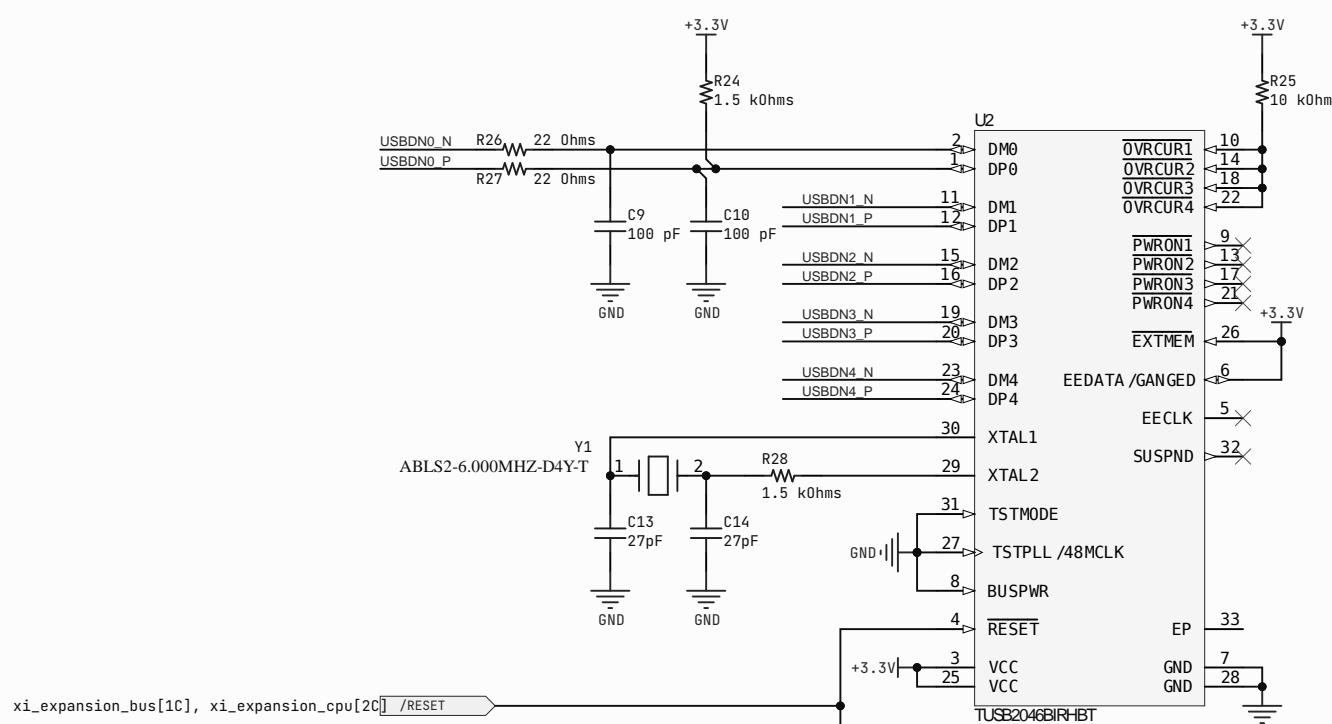
HDMI



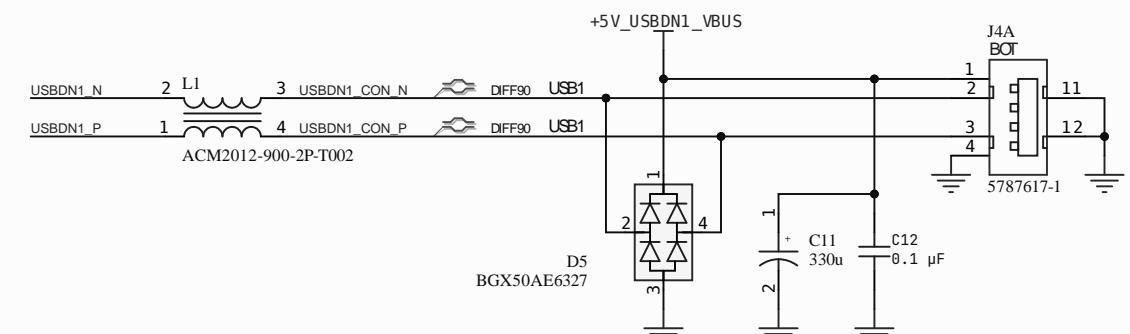
Xi Aleste - HDMI

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	CHKD: -	ENGINEER: Valery		SIZE: A3	REV: r1.0
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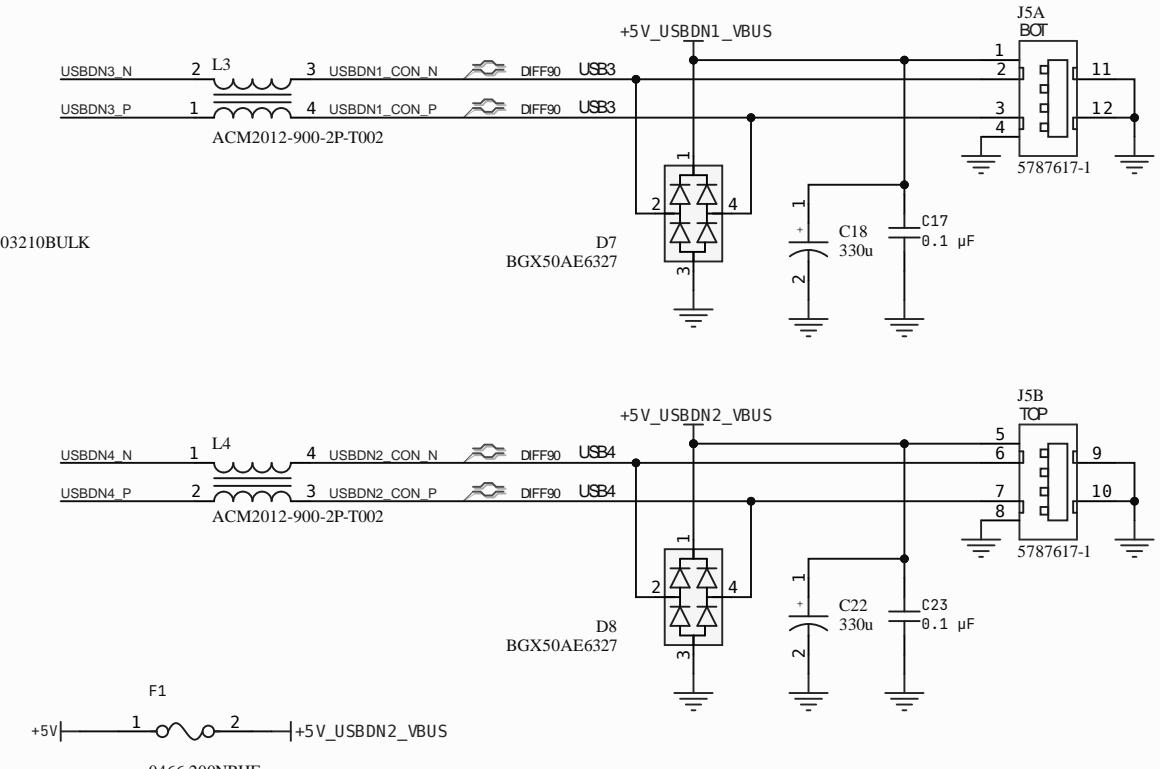
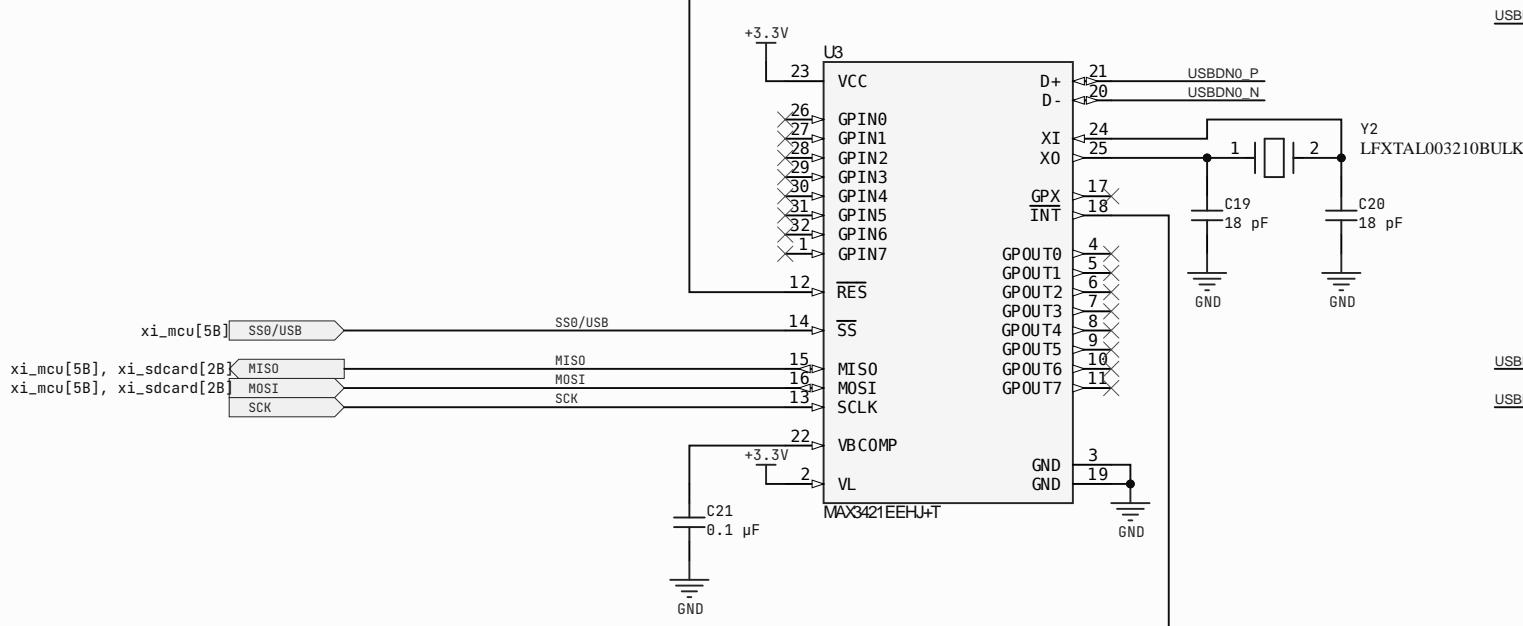
USB HUB



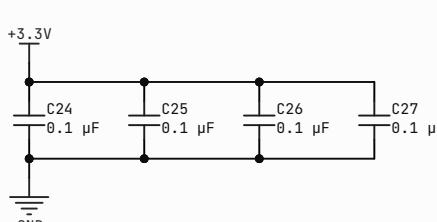
USBDN 1-4 FROM HUB



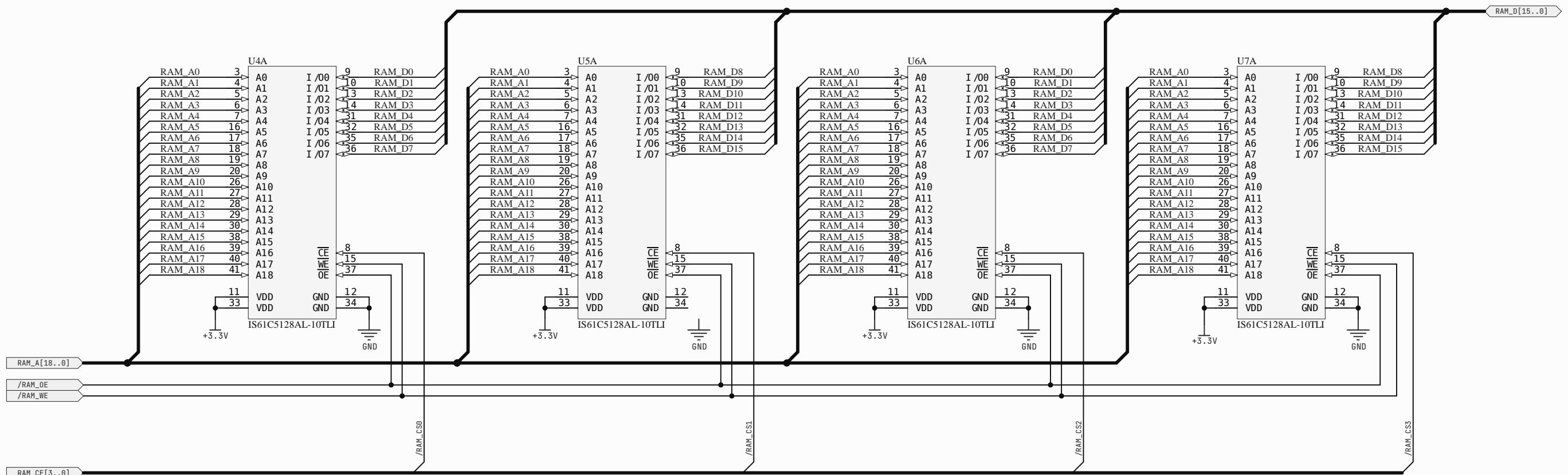
SPI 2 USB CONTROLLER



DECOUPLING



A



B

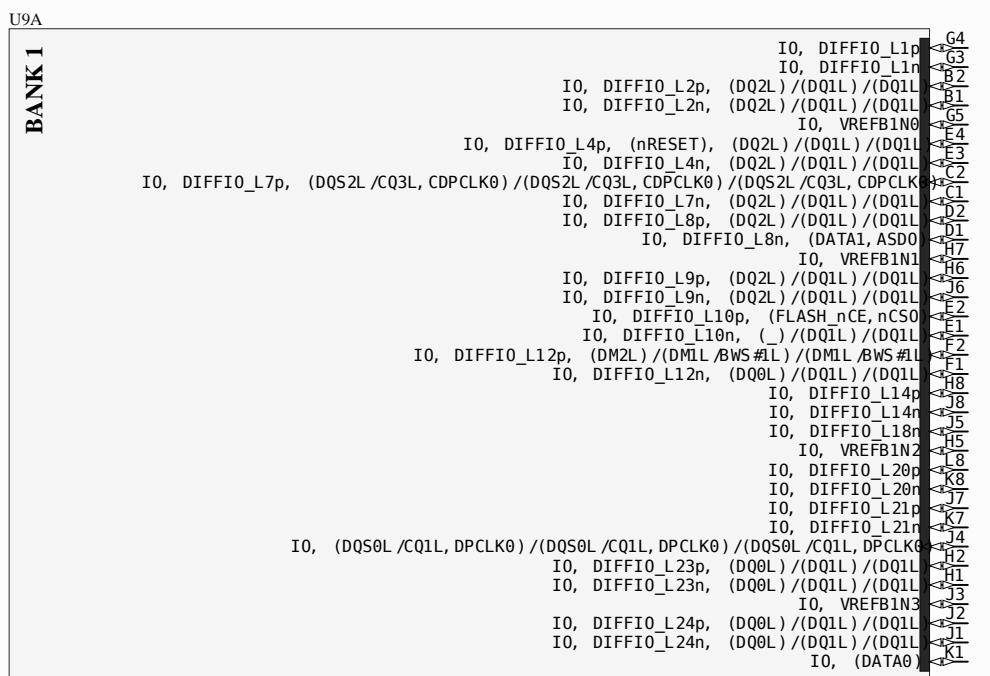
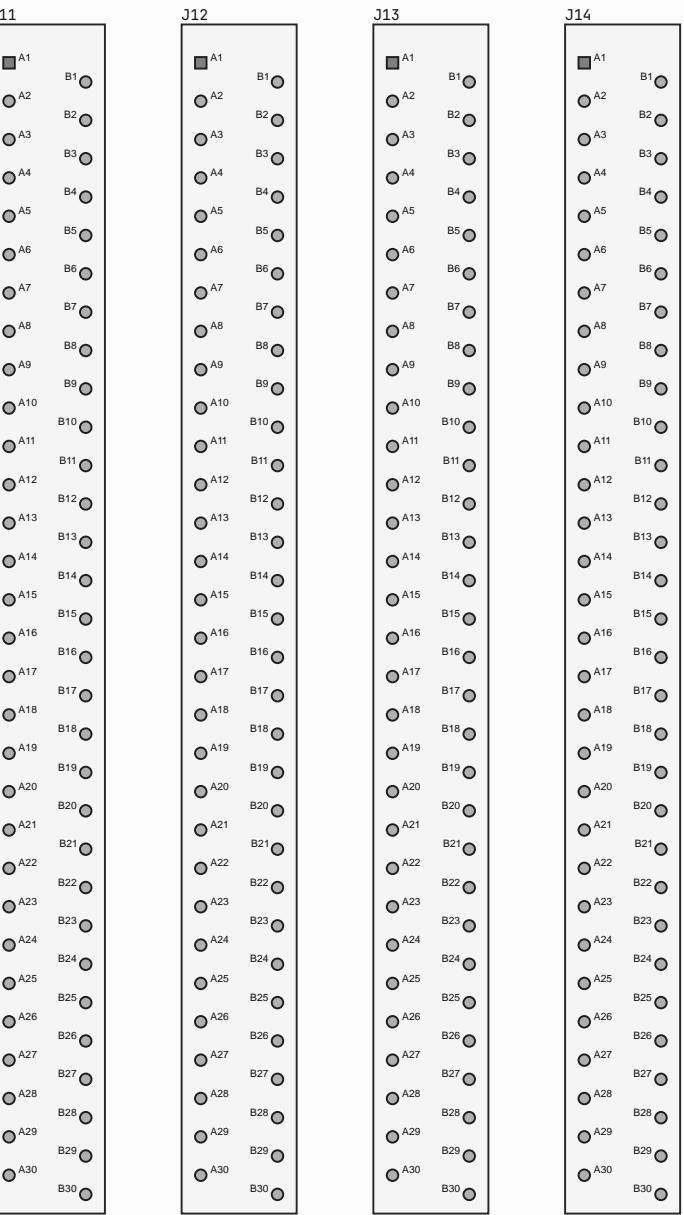
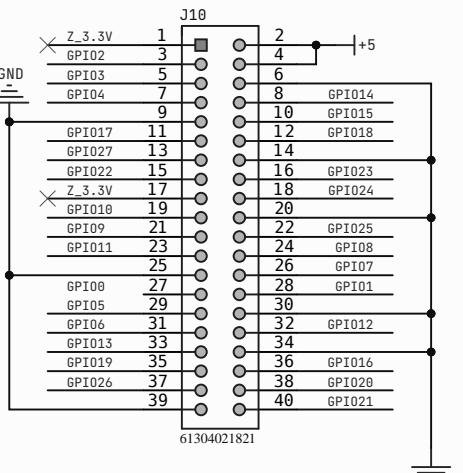
C

D

Xi Aleste - Memory

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CHKD: -	ENGINEER: Valery	APPR: -	
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Sheet 7 of 18			

RASPBERRY PI ZERO

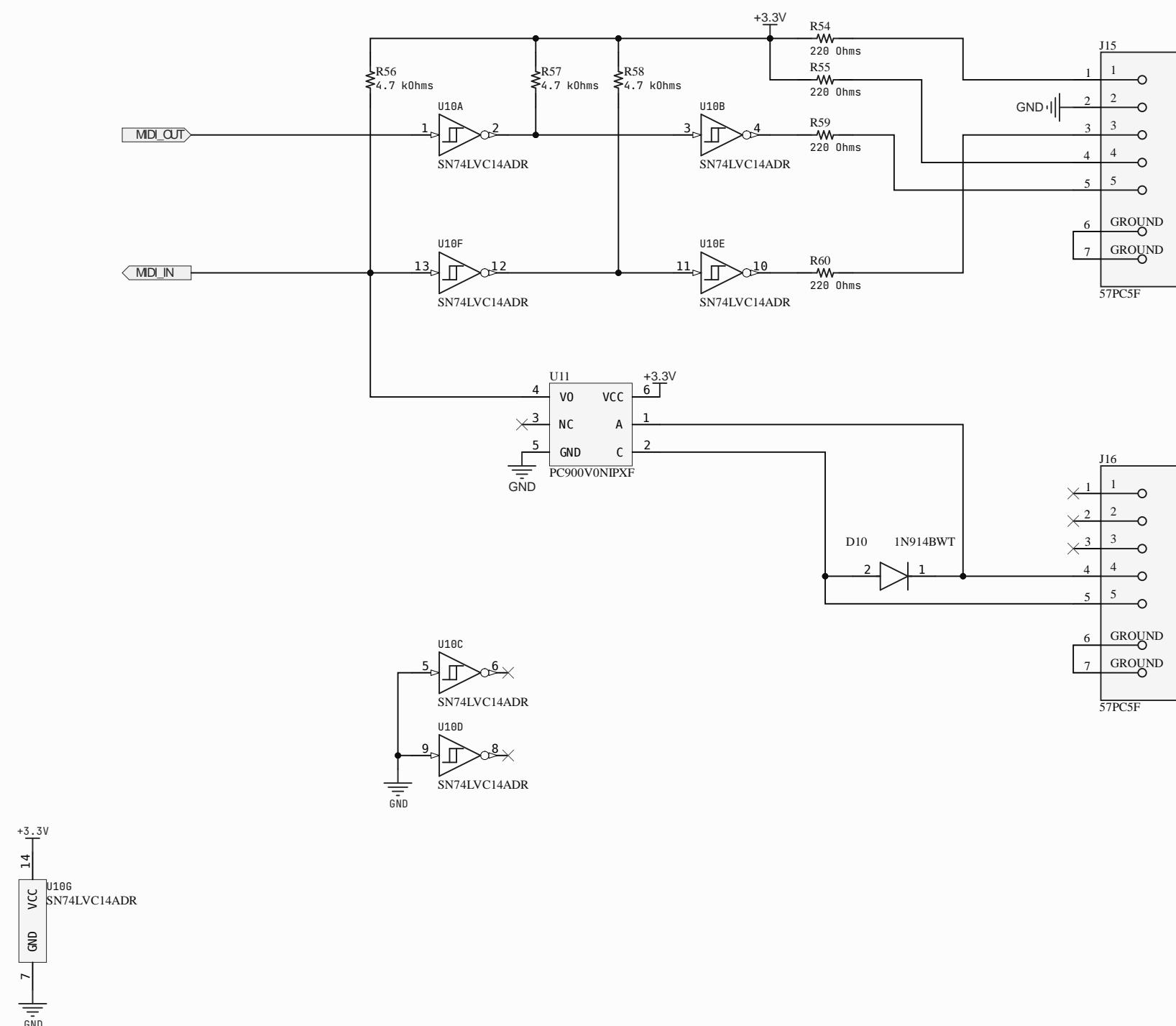


Xi Aleste - Field Gate Array 1

Xi Aleste	DRAWN BY:	DATE:	Xi Labs
	Valery (hww)	11/7/2022 9:38:46 PM	
CHKD: -	ENGINEER: Valery	APPR: -	Prj: Xi Aleste
MODIFIED DATE:	22.10.1.41	11/7/2022	Amstrad CPC 128 Replica
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A

MIDI INTERFACE CIRCUIT



Xi Aleste - MIDI Interface

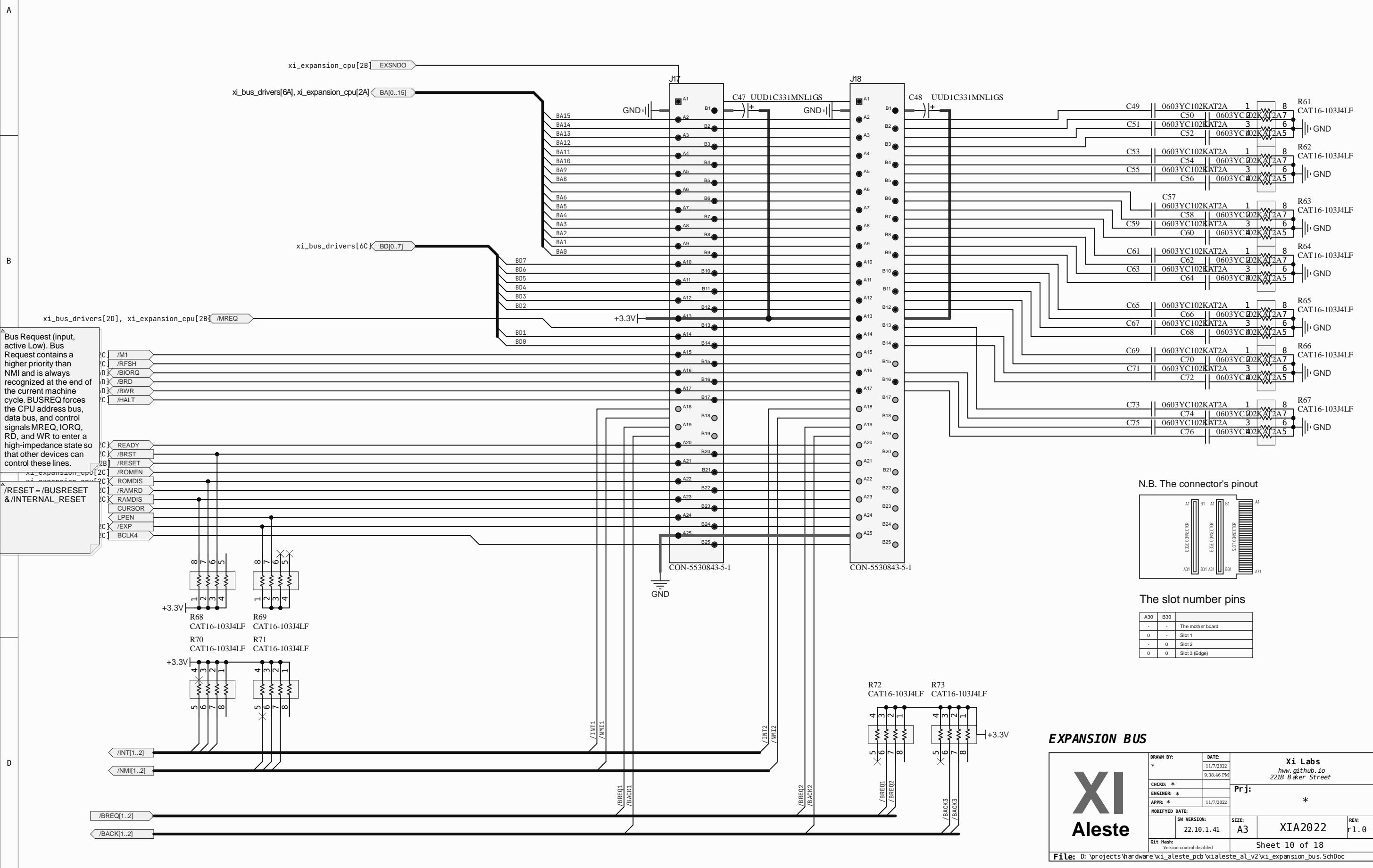
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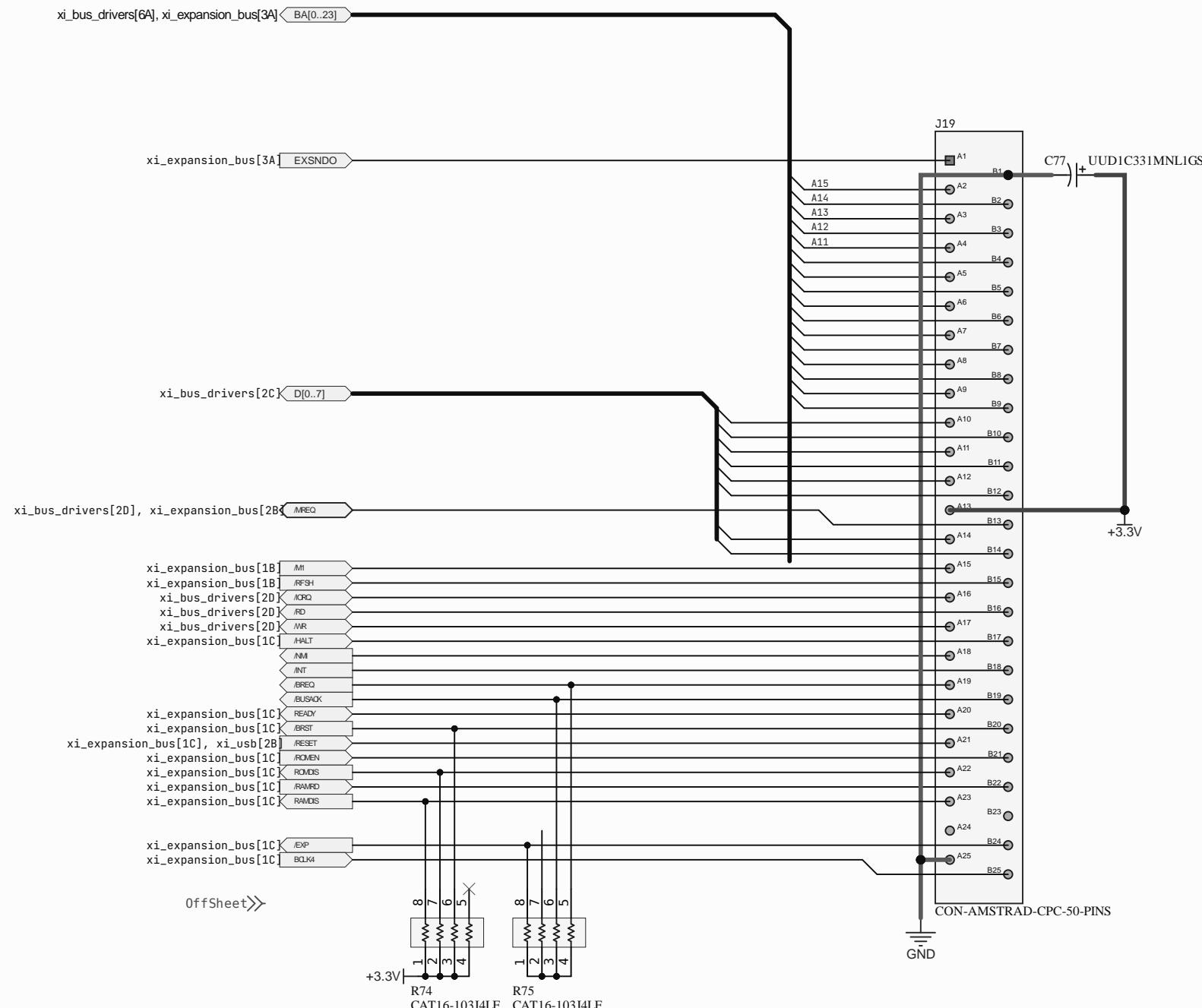
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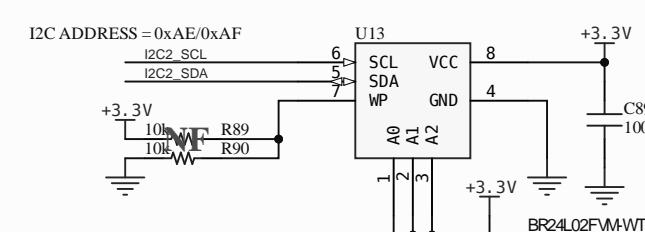
CPU Expansion



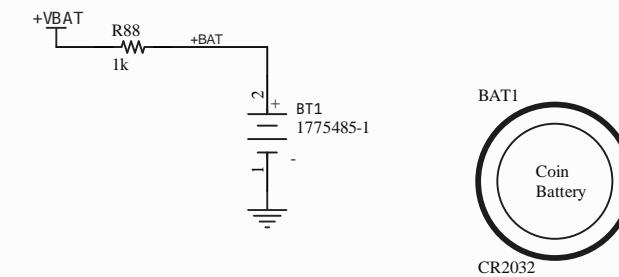
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A

EEPROM

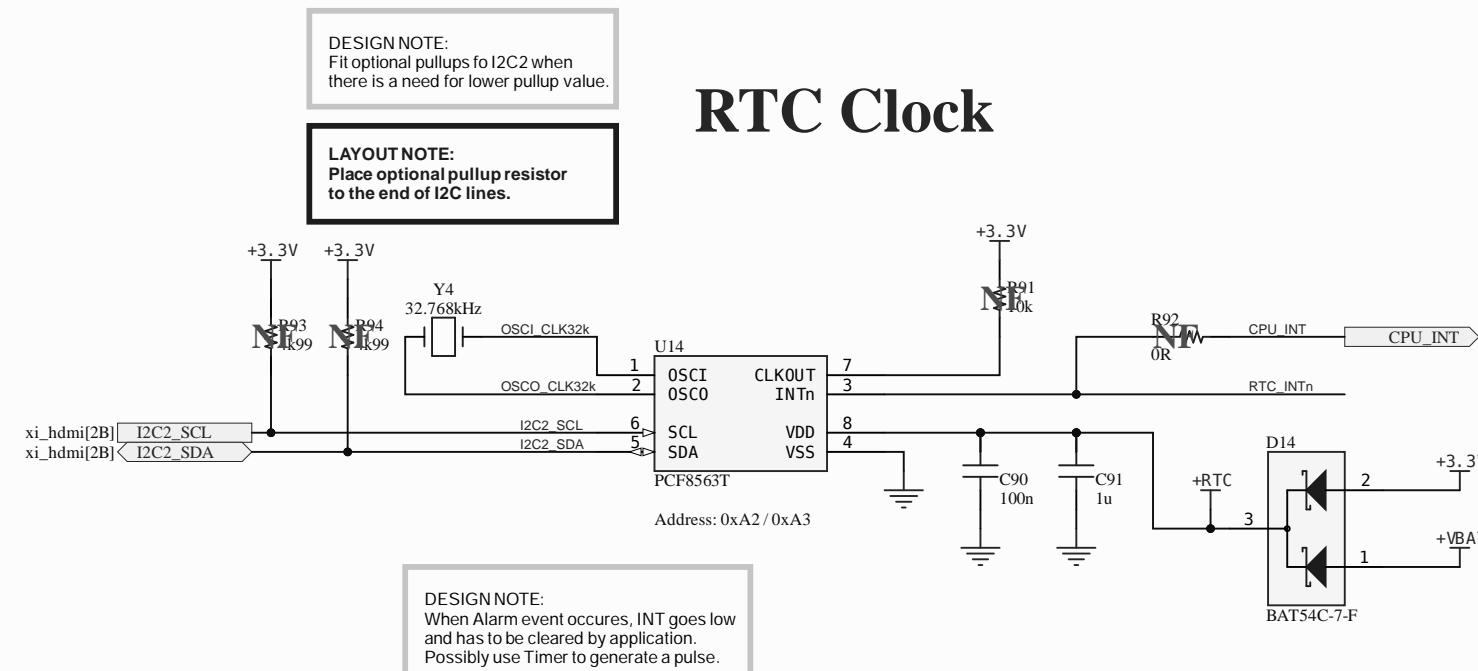


RTC Battery



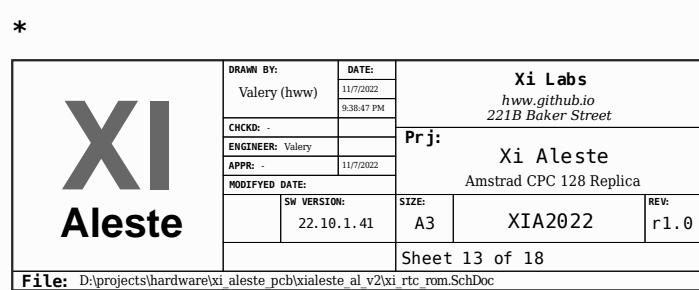
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RTC Clock

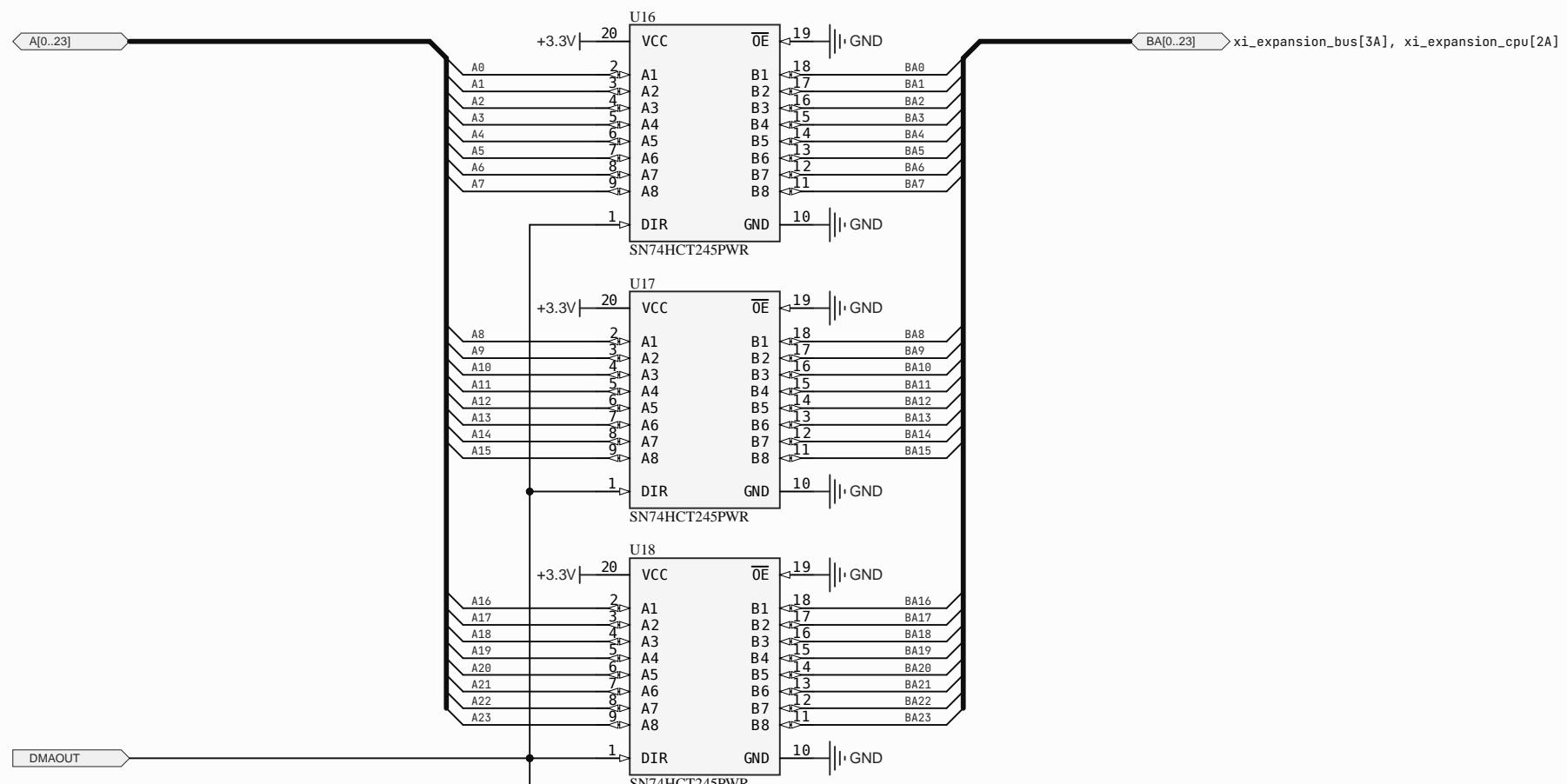


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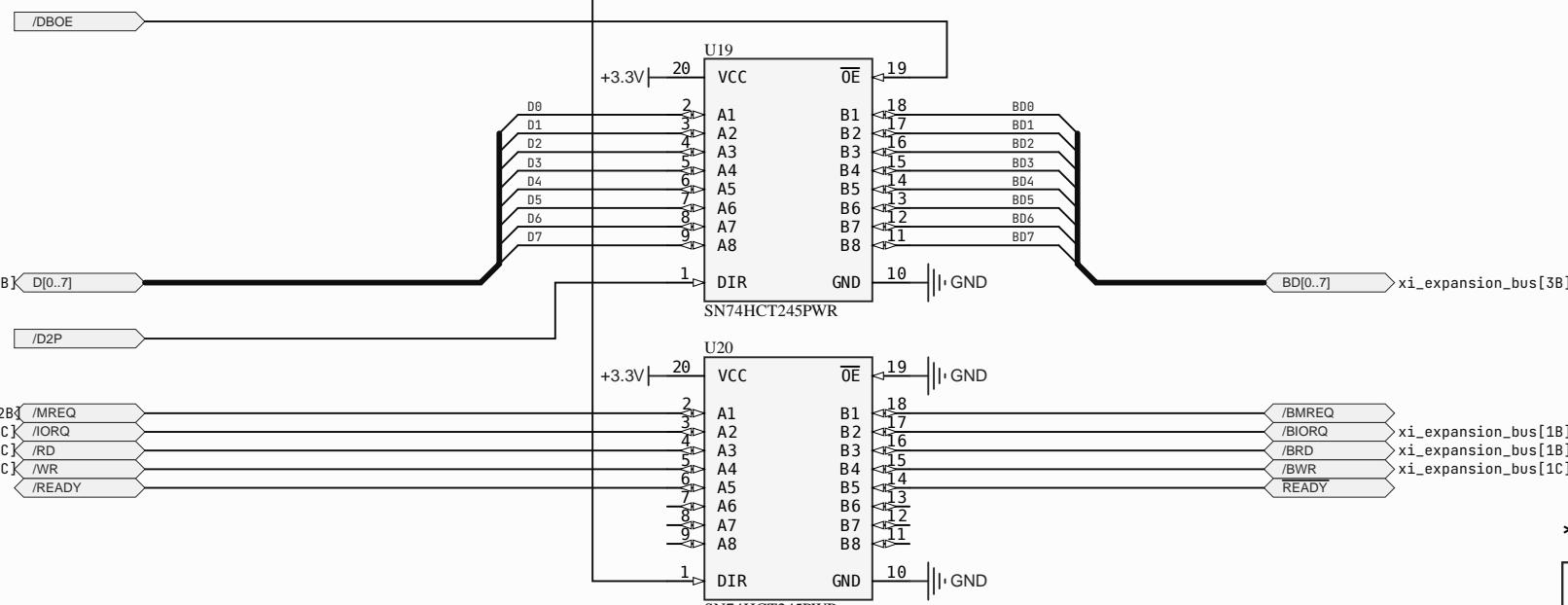
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A

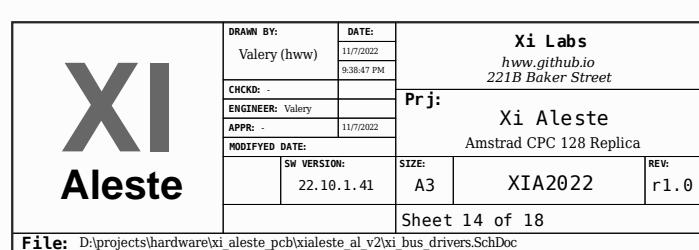


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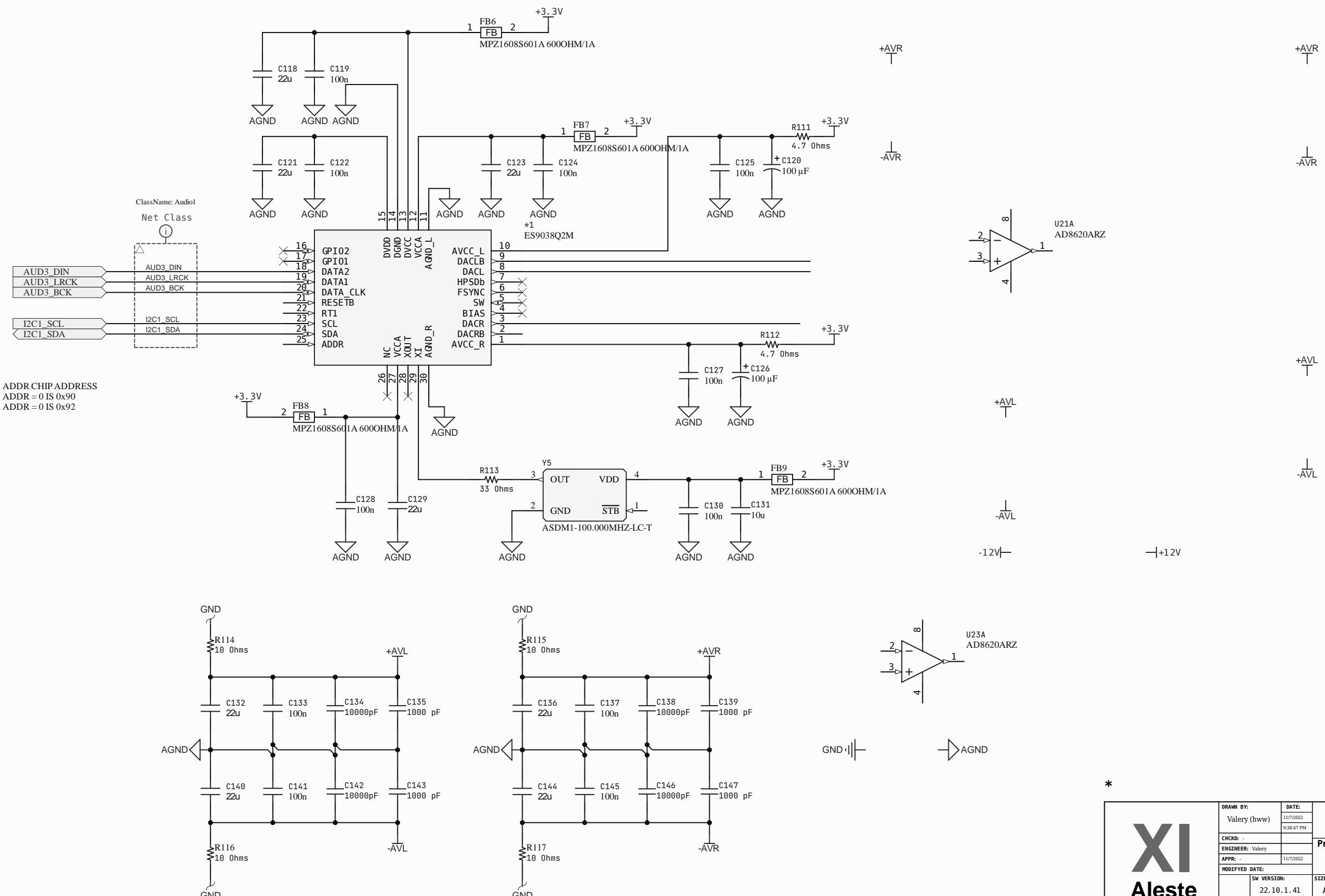


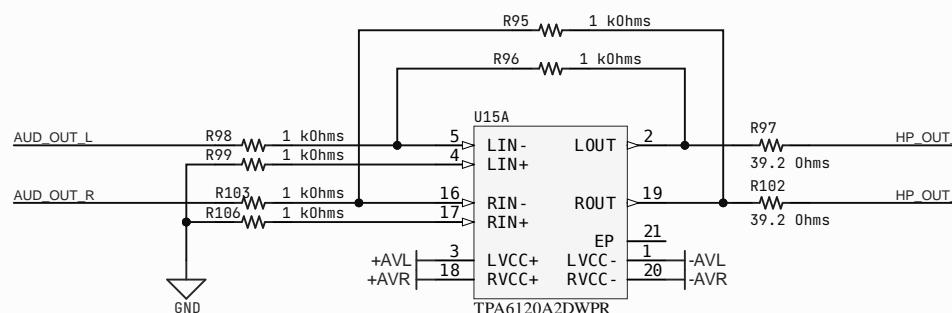
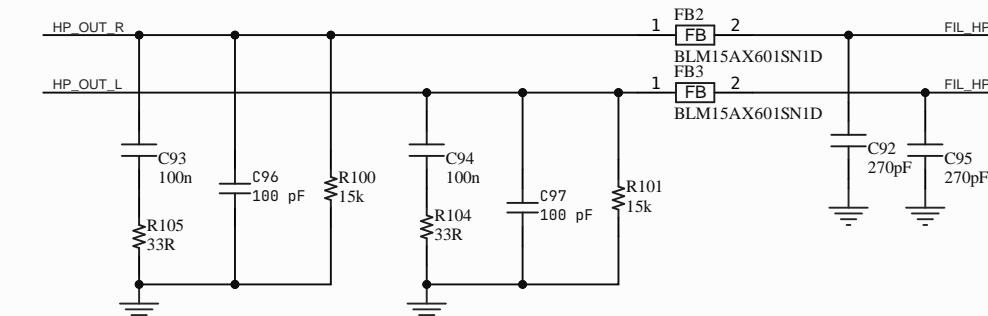
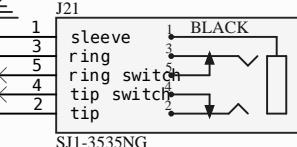
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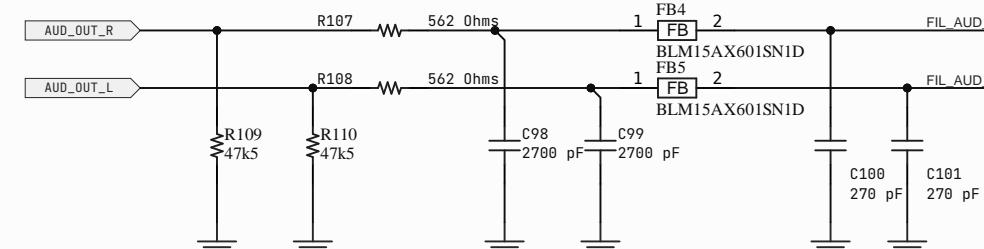
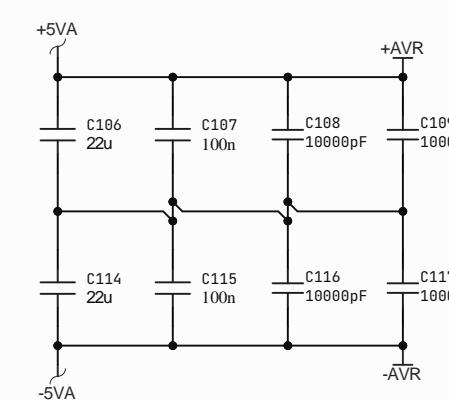
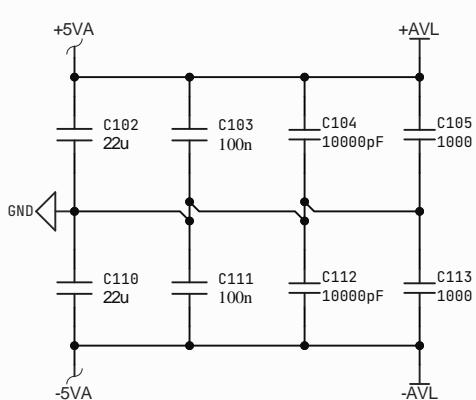
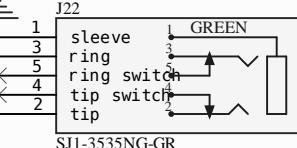


(System audio connected to CPU)



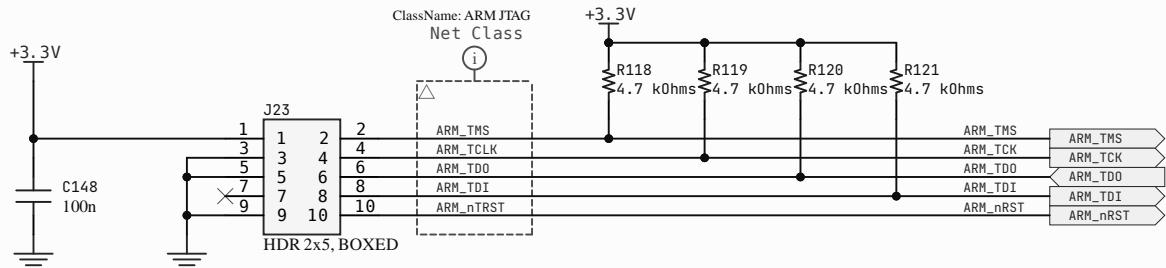
Headphones Amplifier**Headphones****Headphones (Black)**

DESIGN NOTE:
Source for the audio filters is http://www.cirrus.com/en/pubs/rdDatasheet/CDB4207_DB1.pdf

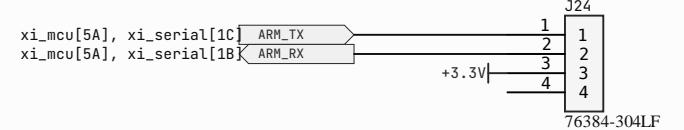
Line Out**Line Out (Green)**

A

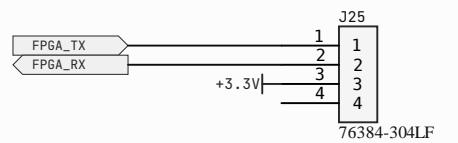
ARM JTAG INTERFACE



ARM SERIAL INTERFACE

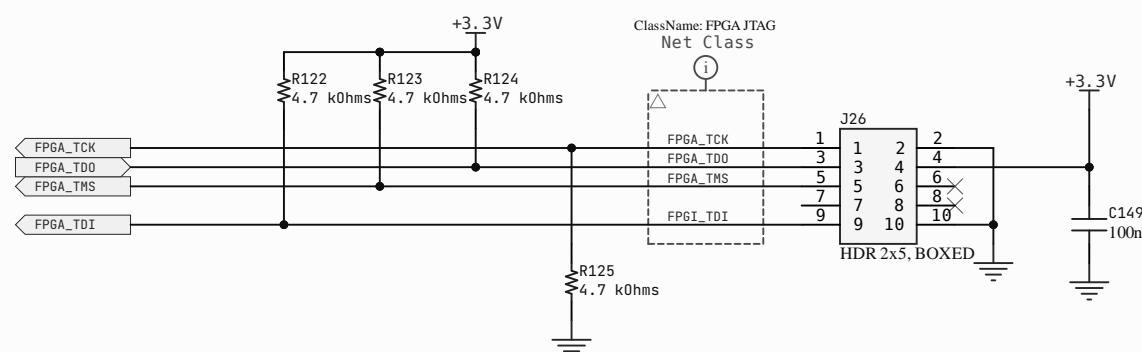


FPGA SERIAL INTERFACE



B

FPGA JTAG INTERFACE



C

D

Xi Aleste - Debugging Interfaces

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	Valery (hww)	11/7/2022 9:38:47 PM	
	CHKD:	-	
	ENGINEER:	Valery	
	APPR:	-	
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