CSE350

Digital Electronics and Pulse Techniques

Lab Report

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Section: CSE5

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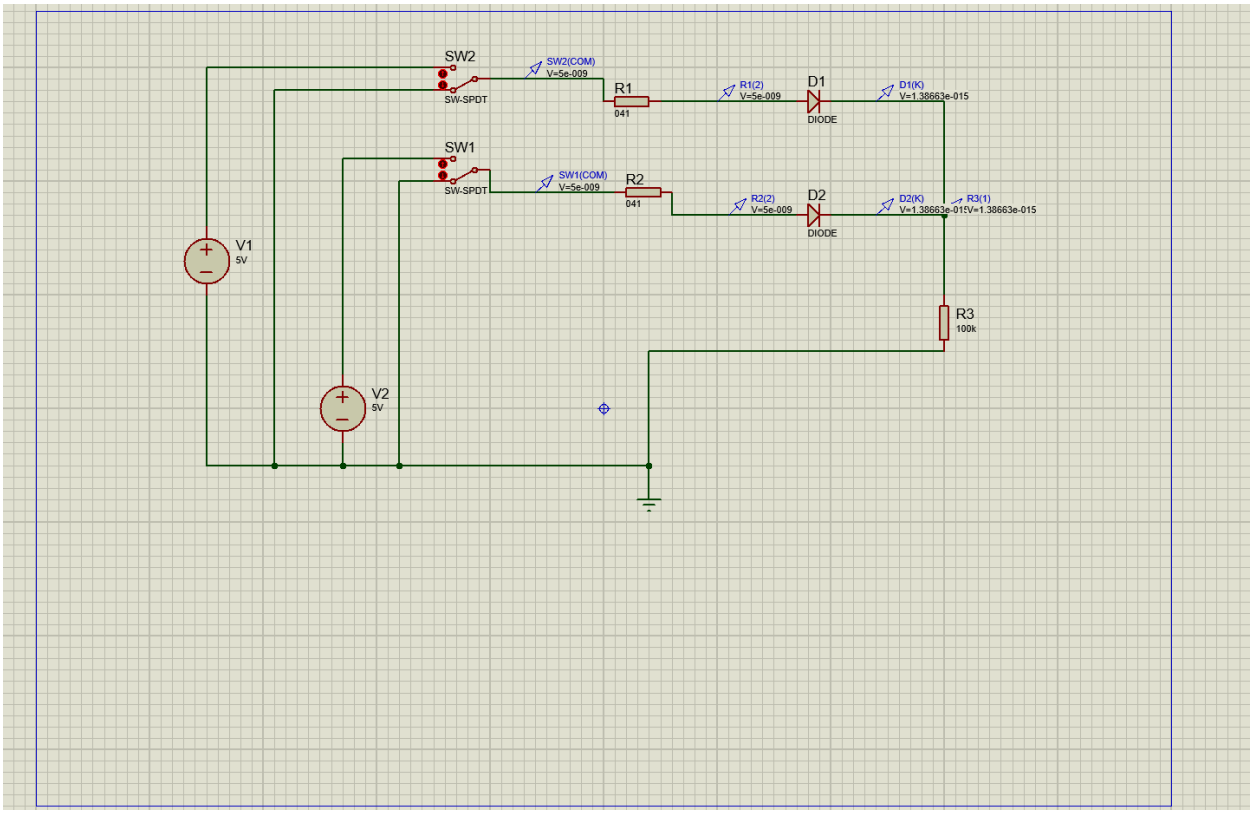

Figure: OR Gate

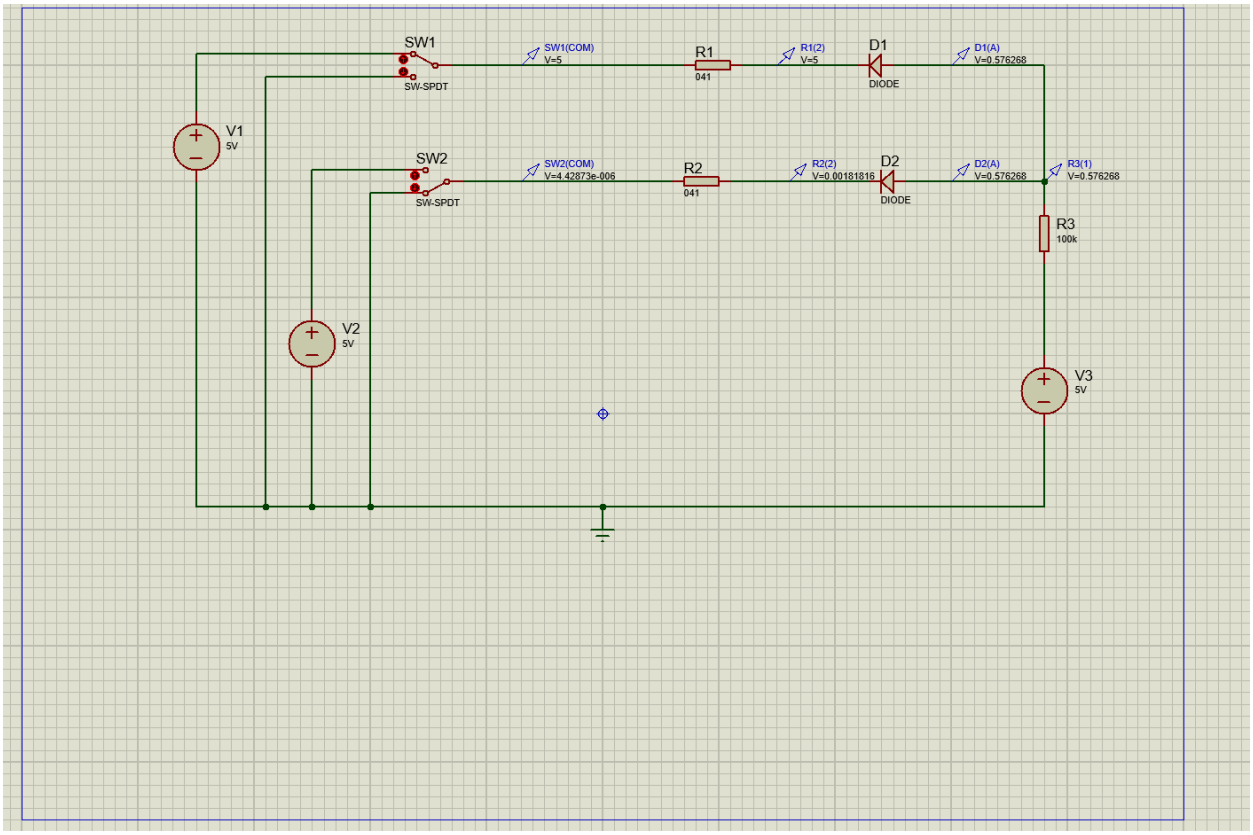

Figure: AND Gate

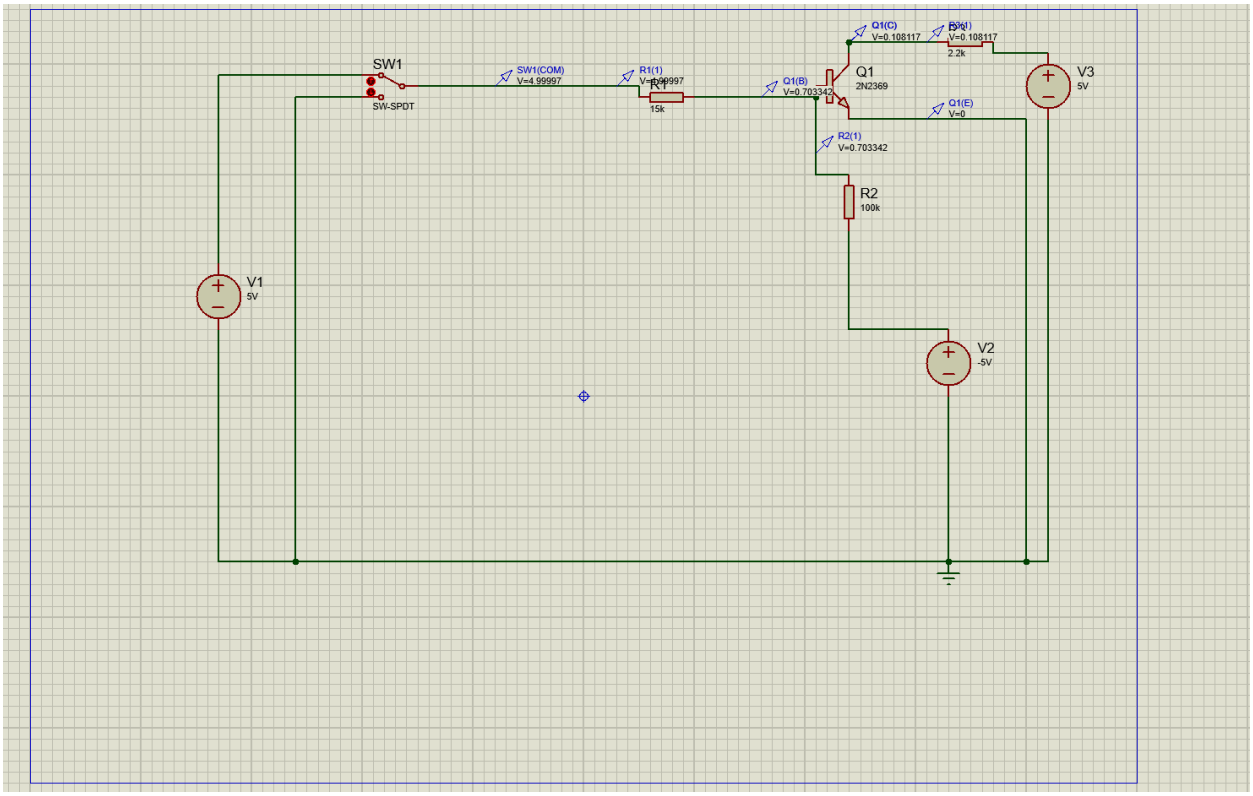

Figure: Inverter Gate

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V_A	V_B	V_{R_1}	V_{R_2}	I_{R_1}	I_{D_2}	$V_R = Y$
0	0	0	0	1.39×10^{-5}	1.39×10^{-15}	1.387×10^{-15}
0	5	1.8×10^{-3}	1.782×10^{-10}	4.9237	4.9237	4.9237
5	0	2×10^{-3}	1.78×10^{-10}	4.9237	4.9237	4.9237
5	5	0.01	0.01	4.99	4.99	4.99

OR Gate

V_A	V_B	V_{R_1}	V_{R_2}	I_{R_1}	I_{R_2}	$V_R = Y$
0	0	8.77×10^{-9}	8.9779×10^{-14}	0.5578	0.578	0.5576
5	0	0	1.8136×10^{-3}	0.576	0.576	0.576
0	5	1.813×10^{-3}	0	0.576	0.576	0.576
5	5	0	0	5	5	5

AND Gate

V_A	V_B	V_{R_1}	V_{R_2}	I_{R_1}	I_{R_2}	$V_R = Y$
0	0	0	0	1.387×10^{-5}	1..	
0	5					
5	0					
5	5					

1830104[illegible]

V_i	V_{R_1}	V_{R_2}	V_{R_C}	I_1	I_2	I_B	I_C	Y
0	0.65	4.35	0	4.3×10^{-5}	4.3×10^{-5}	-3×10^{-3}	1.72[illegible]3	5
5	4.3	5.7	4.9	0.002	5.7	0.00	0.00[illegible]	0.1

Report:

① If both input are logical zero or low. then diode will be on and output will be low. Then if input are logical high diode will be off and current will pass. If input is high, then diode will be on state and output will low.

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V_i	V_{R_1}	V_{R_2}	V_{R_4}	I_1	I_2	I_B	I_C	Y
5	0.6	4.0	0	0				
0								

(2) As $V_A > V_C$ both D_1 & D_2 will work (OR Logic)

As $V_C > V_A$; D_1 D_2 will work (AN Gate)

(3) R_2 at base of an inverter in the mentioned figure is used as pull up resistor. So it does not go into bias nature of input which can vary between 0 & 1.

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(a) Case 1; $I_1 = I_C = I_B = I_C = 0$

$V_B < 0.5$

Cut off mood.

Case 2; ($V_i = 5V$)

β forced $< \beta$

β forced $= \frac{I_C}{I_B}$

$= \frac{4.6122}{0.0622}$

$= 11$