CSE350

Digital Electronics and Pulse Techniques

Lab Report

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Section: CSE5

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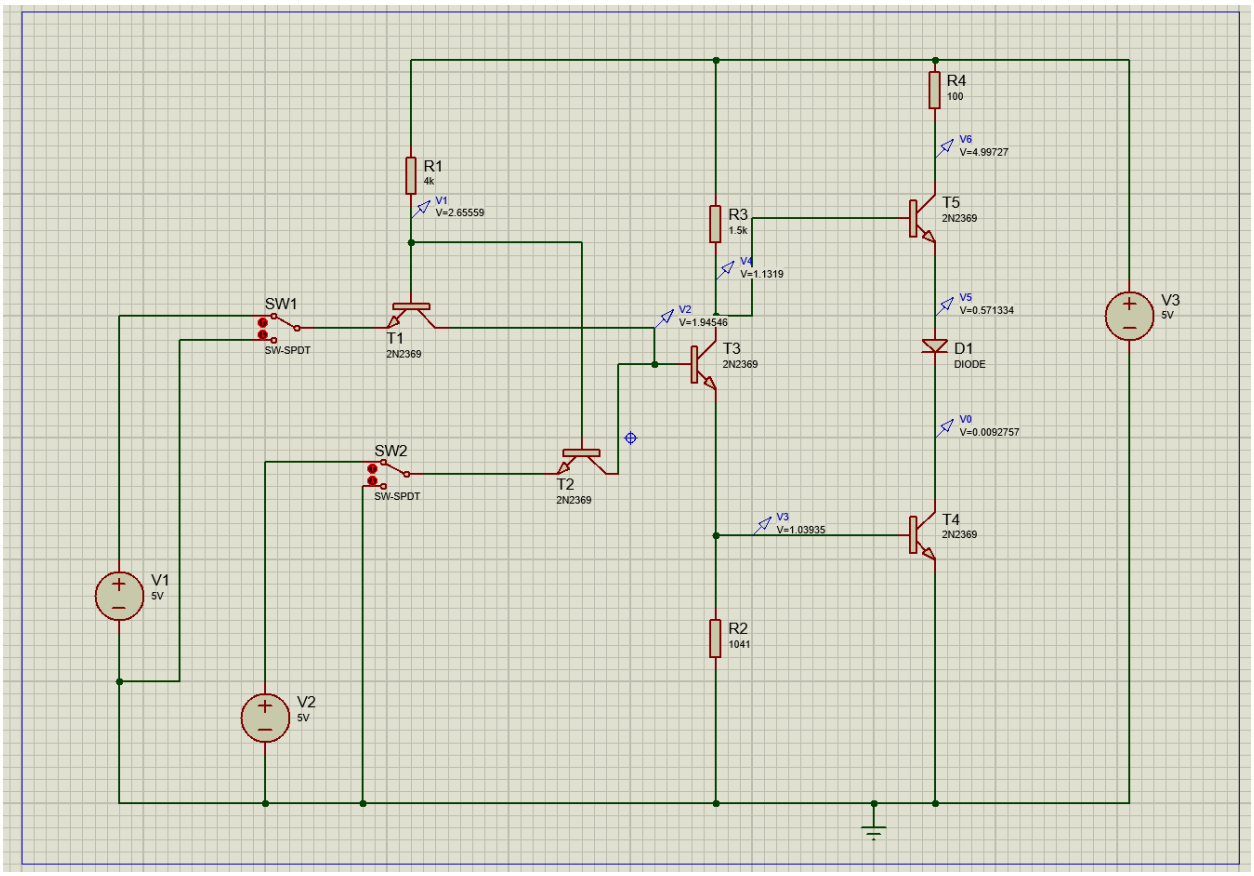

R4
100
V6
V=4.99727
R1
4k
V1
V=2.65559
R3
1.5k
T5
2N2369
V4
V=1.1319
V5
V=0.571334
V3
5V
SW1
SW-SPDT
T1
2N2369
V2
V=1.94546
T3
2N2369
D1
DIODE
V0
V=0.0092757
SW2
SW-SPDT
T2
2N2369
V3
V=1.03935
T4
2N2369
V1
5V
R2
1041
V2
5V

18301041

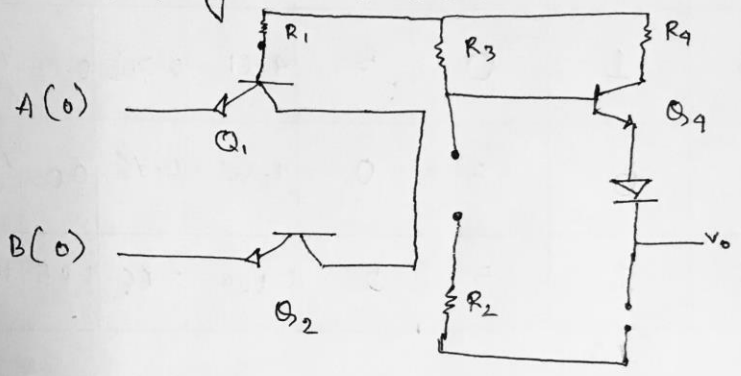
Input A	Input B	Input V_A	Input V_B	V_0	V_1	V_2	V_3	V_4	V_5	V_6
0	0	0	0	4.61	0.717	0.008	7.19×10^{-09}	5	4.8	5
0	1	0	5	4.61	0.755	0.05	7.25×10^{-09}	5	4.80	5
1	0	5	0	4.61	0.76	0.05	7.25×10^{-09}	5	4.8	5
1	1	5	5	0.009	2.66	1.95	1.09	1.13	0.57	4.997

1. In NAND Gate if one of the input is low or 0, the output will be high or 1. Also if both the input is 0, the output will be 1 and if both the inputs are 1, then the output will be 0.

In figure 1, if one of the input is low transistor T_1 and T_2 will be in saturation mood. So, the collector voltage of transistors will be 0.1v which is the base voltage of transistor T_3. Therefore, T_3 will be in cut-off mood as well as T_4 and T_5. So, the output will be close to V_{cc} which is logical high and thus work in the case of NAND Gate.

2. Totem pole stage also known as output section which has 2 complementary pair of transistors, each amplifying one another.

3.



4 T_3 is a phase spliftem for Q_4 and Q_5 which conduct in such way if one is in cut off the other will be on.

5 If Diode D_1 is not used, Q_3 would be in saturation mood which result such a way that pass excess current.

6. $V_6 = 5$ $V_5 = 4.8$ [From Proteus Data]

$V_6 - V_5 = 0.2$ which is V_{CE} for T_5

Therefore, T_5 is in forward Active Mode.

7.