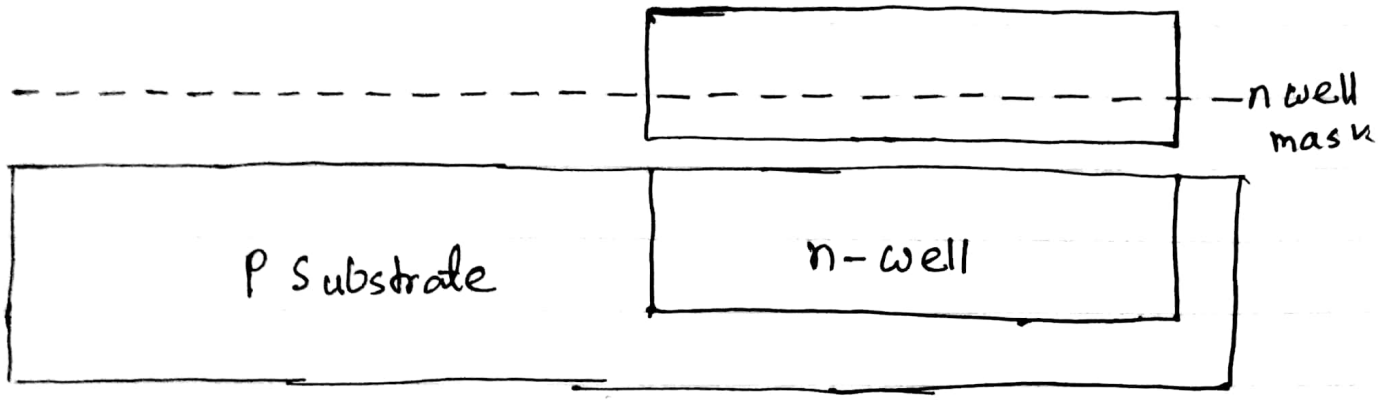
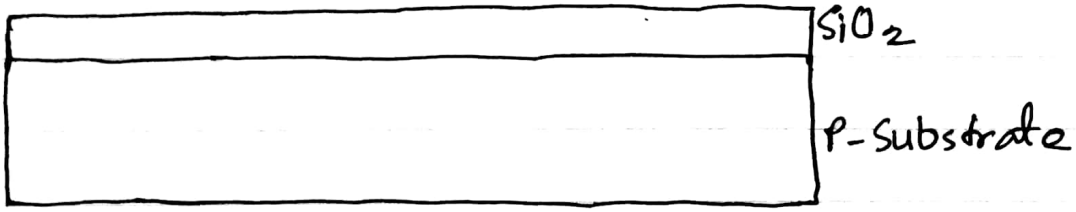
Date

1. @ n-well mask

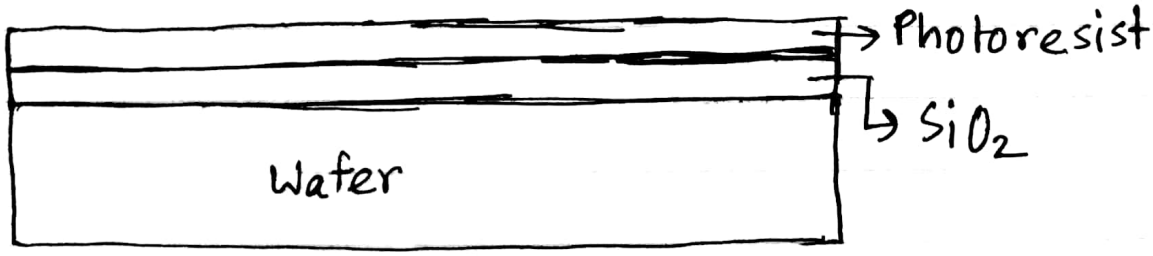


(b) Steps to fabricate n-well

① Oxidation : SiO_2 on the top of Si wafer / blank

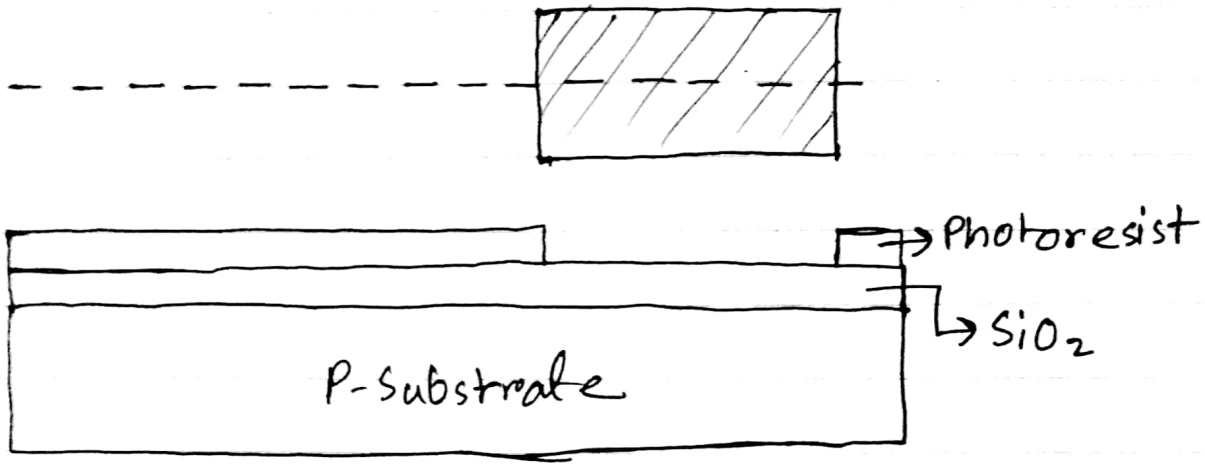


② Photoresist

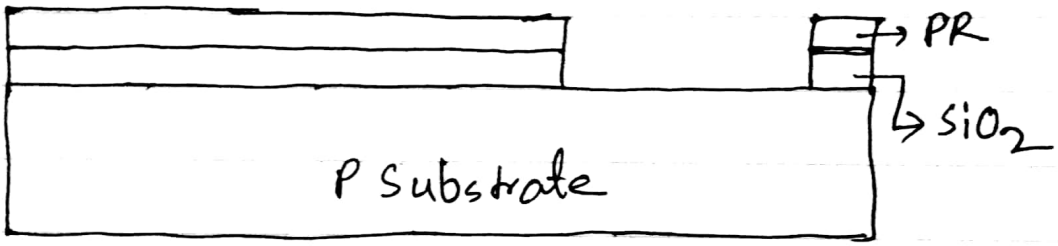


③ Lithography

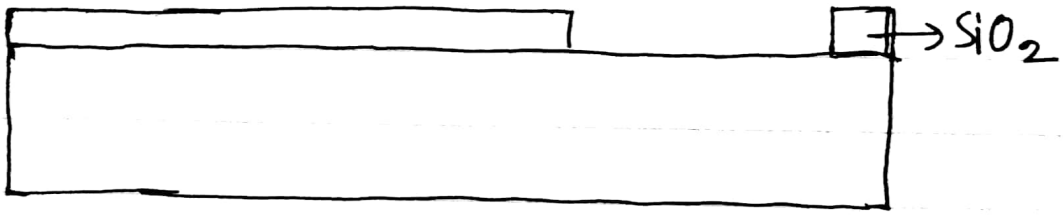
Expose photoresist through n-well mask



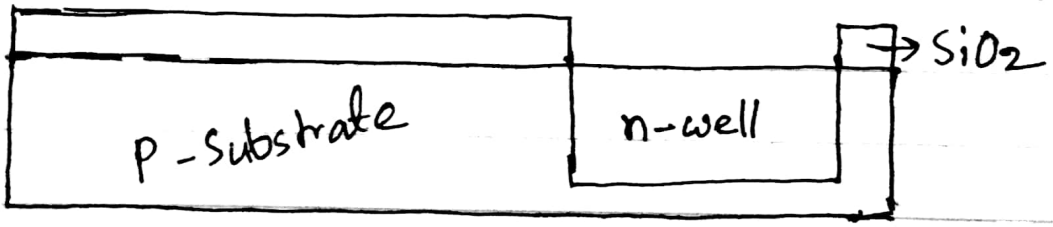
④ Etch



⑤ Strip Photoresist

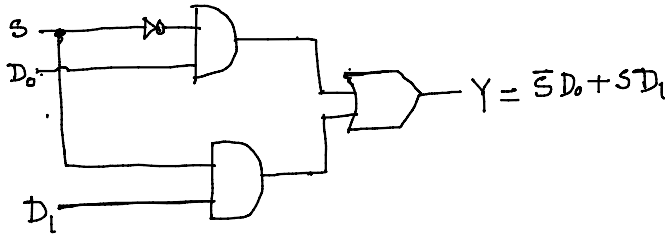


⑥ n-well : formed with diffusion or ion implantation



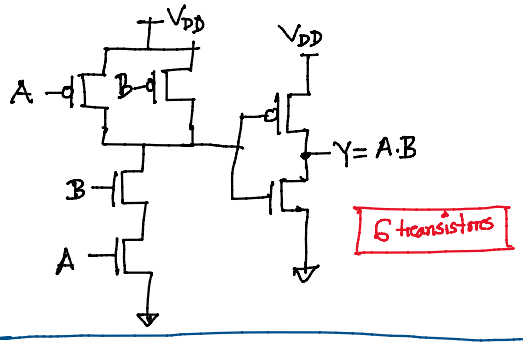
Saturday, March 12, 2022 9:35 PM

2. (a) 2-to-1 multiplexer using basic logic gates:

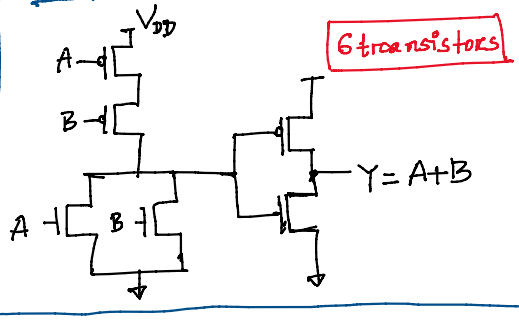


So, total number of transistors required
= 2 AND gates + 1 OR gate + 1 inverter
= 2 × 6 + 6 + 2
= 20

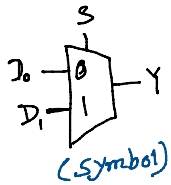
2-input AND gate



2-input OR Gate



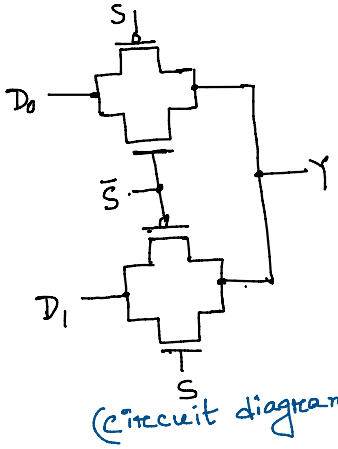
(b) 2-to-1 multiplexer design using transmission gates



(symbol)

S	Y
0	D_0
1	D_1

(truth table)

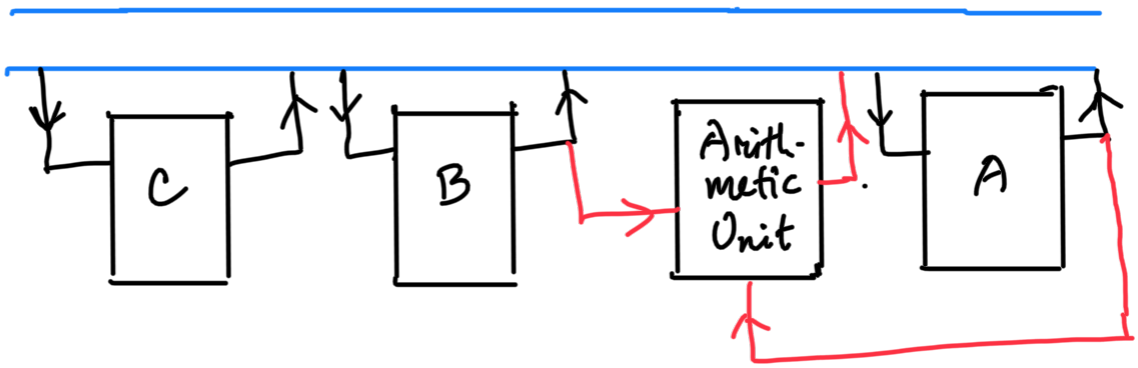


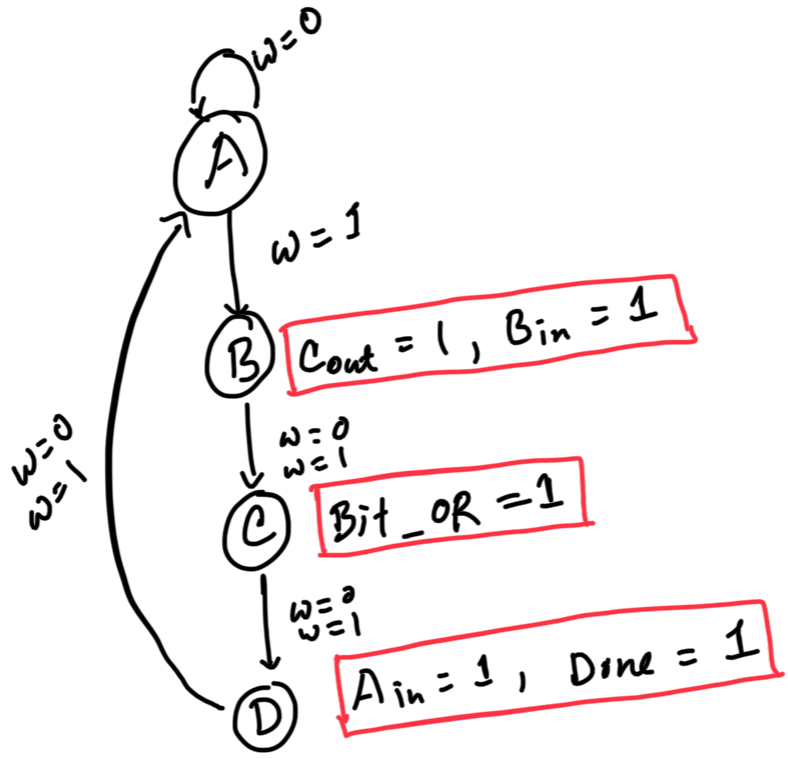
(circuit diagram)

So, total number of transistors required = 4

This design is non-restoring since any noise on the input line goes directly to the output

Mid Spring '22





Table

Present state $y_4y_3y_2y_1$	Next State $w=0$ $Y_4Y_3Y_2Y_1$	Next State $w=1$ $Y_4Y_3Y_2Y_1$	Output: Ain	Bin	Cout	Bit_OR	Done
A 0001	A 0001	B 0010	0	0	0	0	0
B 0010	C 0100	C 0100	0	1	1	0	0

C 0 100	D 1000	D 1000	0	0	0	1	0
D 1 000	A 0001	A 0001	1	0	0	0	1

$Y_1 = \bar{w} y_1 + y_4$

$Y_2 = w y_1$

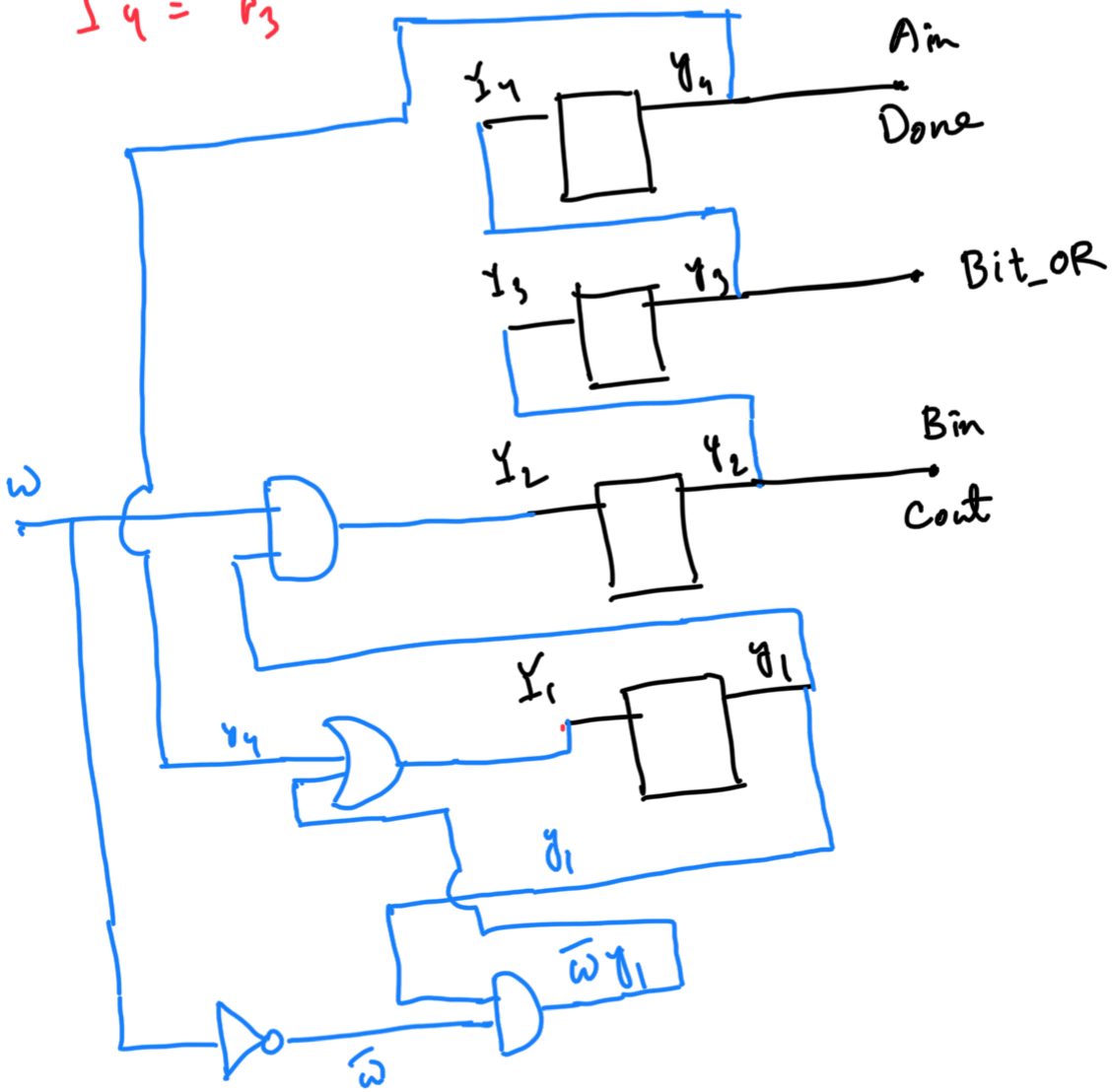
$Y_3 = y_2$

$Y_4 = y_3$

$B_{in} = C_{out} = y_2$

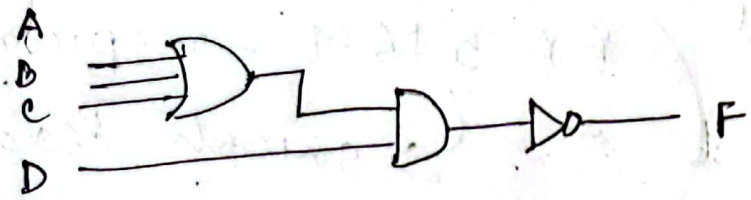
$Bit\_OR = y_3$

$A_{in} = Done = y_4$

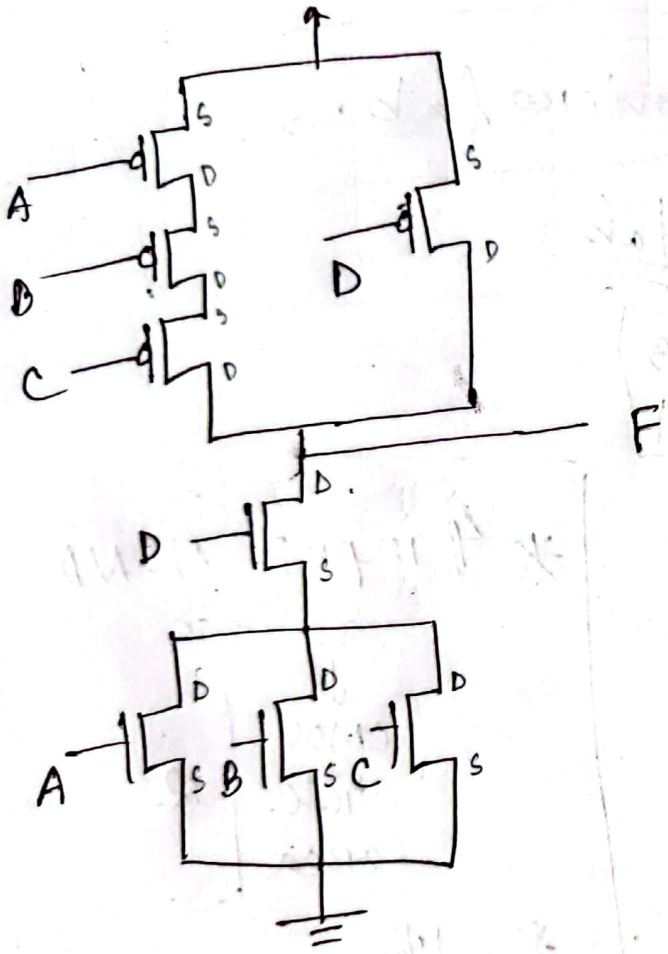


Part (a)

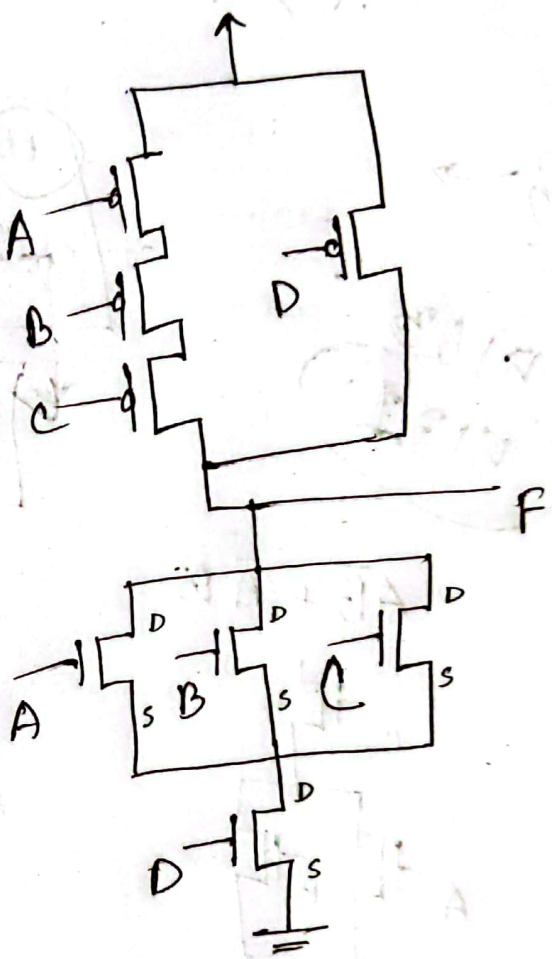
OAI 31 → CMOS → stick → area



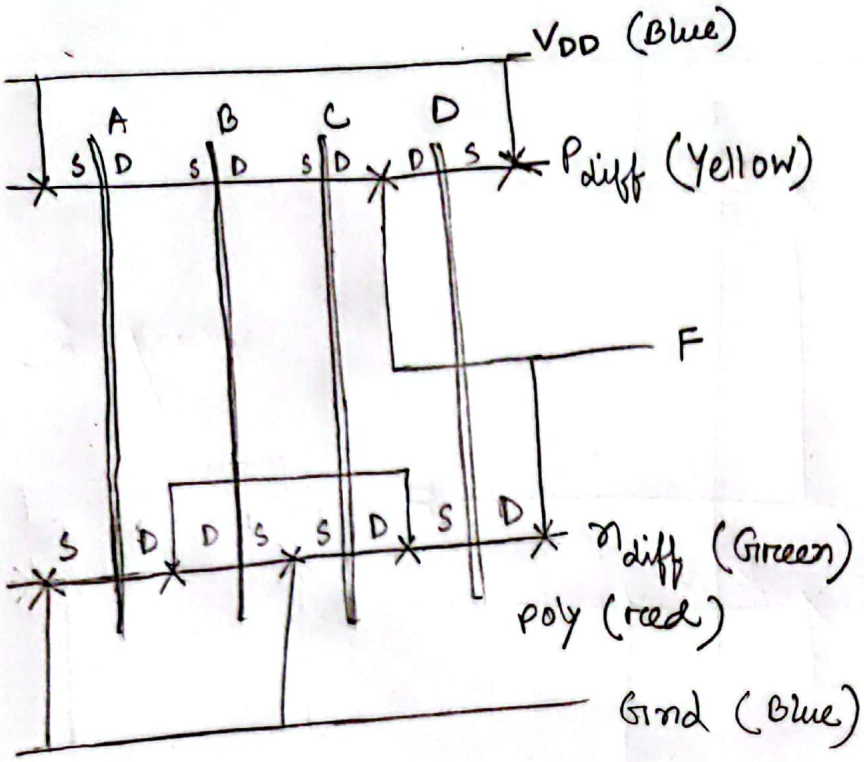
$F = \overline{(A+B+C)D}$



way 1



way 2



way 1

area : height : 6 tracks

$\therefore (6 \times 8)\lambda$

$= 48\lambda$

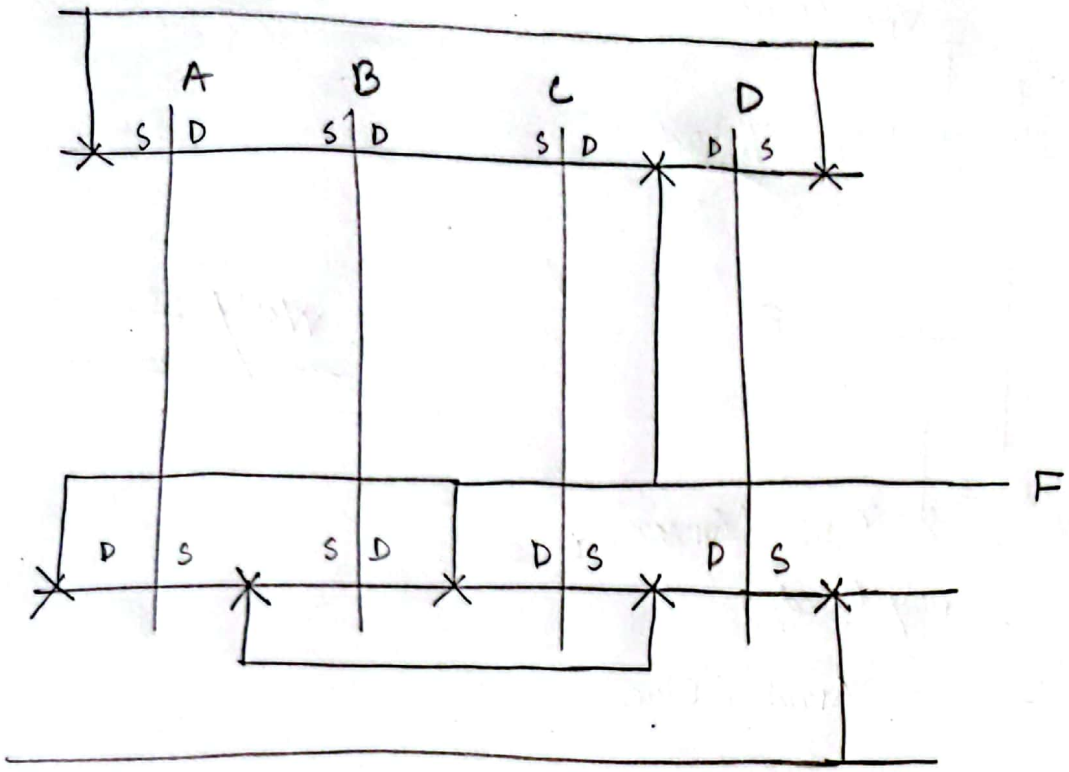
width : 5 tracks

$\therefore (5 \times 8)\lambda$

$= 40\lambda$

area $48 \times 40\ \lambda^2$

$= 1920\ \lambda^2$



way 2

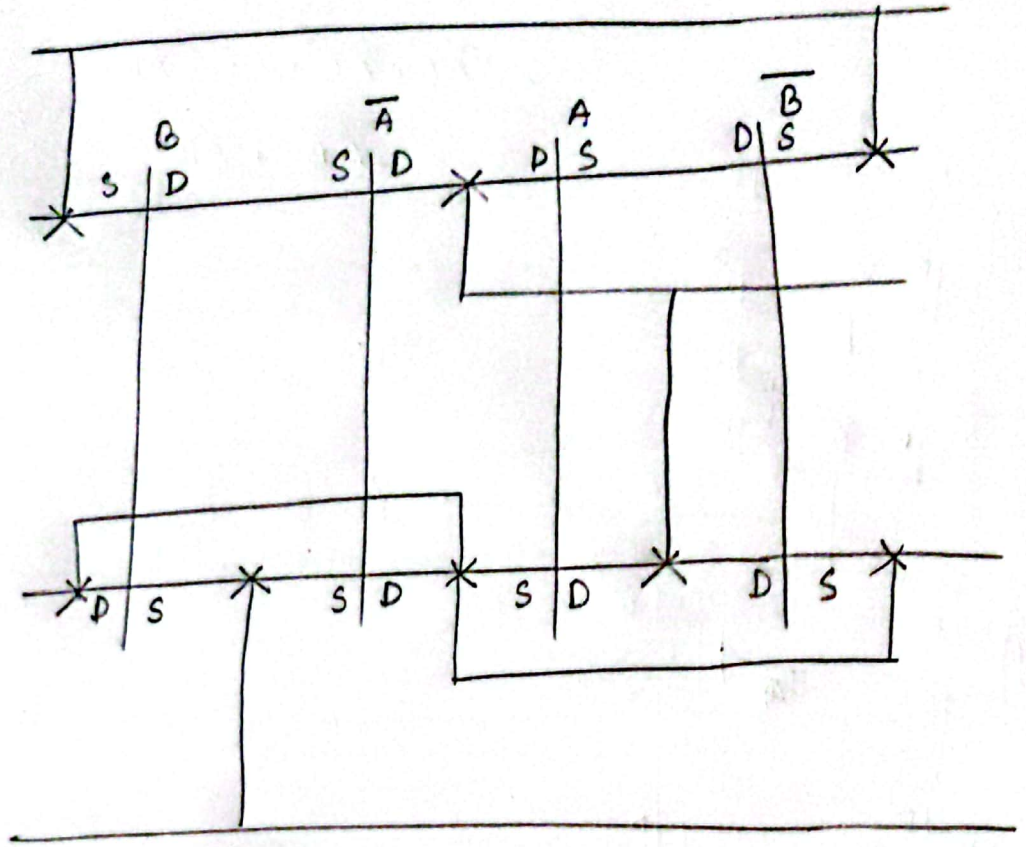
height : 48λ

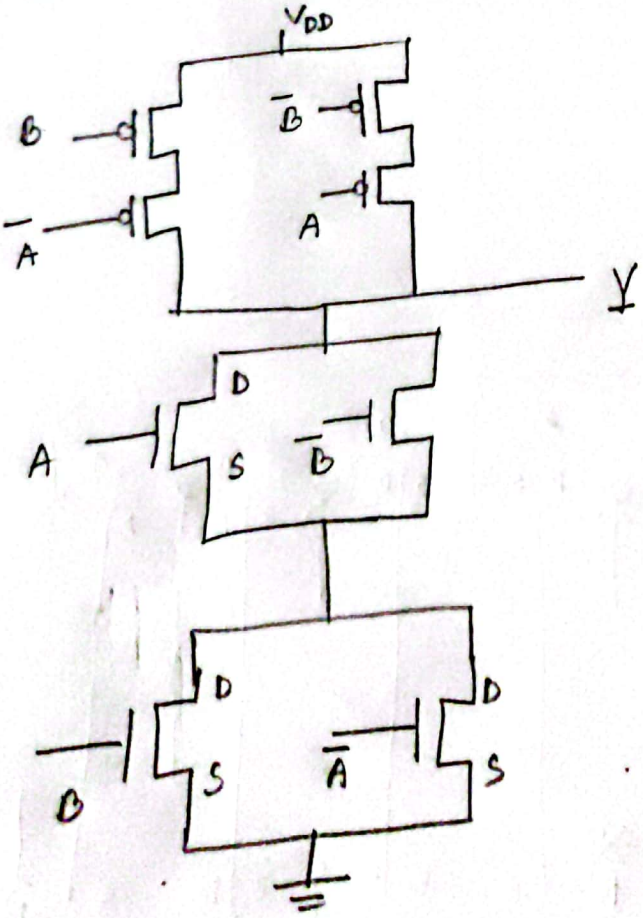
width : 40λ

area : $1920\lambda^2$

Question 2

Part (b)





$$Y = \overline{(\overline{A}+B)(A+\overline{B})}$$

$$= \overline{A\overline{A} + \overline{A}\,\overline{B} + AB + B\overline{B}}$$

$$= \overline{AB + \overline{A}\,\overline{B}}$$

$$= \overline{AB} \cdot \overline{\overline{A}\,\overline{B}}$$

$$= (\overline{A}+\overline{B})(A+B)$$

$$= A\overline{B} + A\overline{B}$$

XOR Gate

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

Area:

Height: $(7 \times 8\lambda) = 56\lambda$

width: $(5 \times 8\lambda) = 40\lambda$

$\therefore$ area = $2240\lambda^2$