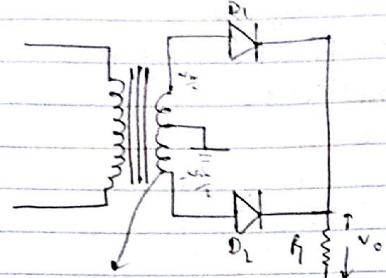
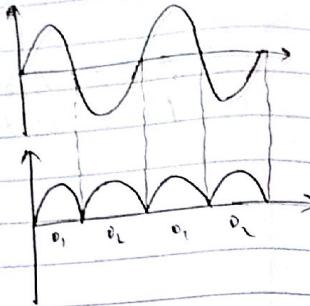


## # Full wave Rectifier

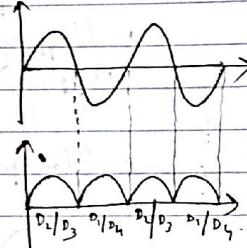
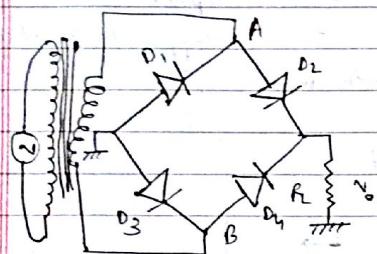


center tapped  
transformer



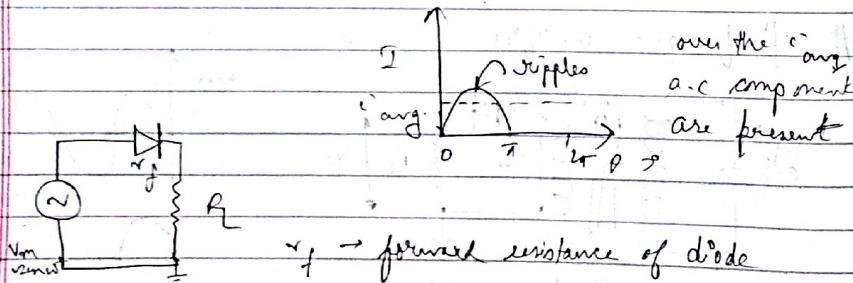
Transformer → necessary for FWR, unlike HWR

## # Bridge Rectifier



check

## # Efficiency of a half-wave rectifier



$r_f$  → forward resistance of diode

O/P → not a true d.c. → mag. not steady

$$i = i_{\text{m}} \sin \omega t = \frac{V_{\text{m}} \sin \omega t}{R_L + r_f}$$

$$\text{Avg current} = \frac{1}{T} \int i_{\text{m}} \sin \omega t dt = \frac{i_{\text{m}} [\cos \omega t]}{\pi} = \frac{i_{\text{m}}}{\pi}$$

$$= \frac{i_{\text{m}}}{2\pi} \times 2 = \frac{r_f}{R_L} \cdot \frac{i_{\text{m}}}{\pi}$$

$$\Rightarrow T_{\text{avg}} = \frac{I_{\text{m}}}{(n^2 I_{\text{d.c.}})}$$

$$\text{Efficiency } \eta = \frac{P_{\text{d.c.}}}{P_{\text{ac}}} = \frac{i_{\text{d.c.}}^2 R_L}{i_{\text{m}}^2 (r_f + R_L)}$$

$$(\text{Here } i_{\text{rms}} = \sqrt{i_{\text{dc}}^2 + i_{\text{ac}}^2}) \Rightarrow \eta = \frac{4}{\pi^2} \left( \frac{R_L}{R_L + r_f} \right)$$

$$i_{\text{rms}} = \frac{I_{\text{m}}}{2} \\ P_{\text{ac}} = i_{\text{rms}}^2 (r_f + R_L)$$

As  $r_f \ll R_L$   $\frac{R_L}{R_L + r_f} \approx 1$

$$\eta = \frac{4}{\pi^2} \quad \eta = 0.406$$

Gives  $\eta \approx 40.6\%$  for a half-wave rectifier

## Ripple Factor

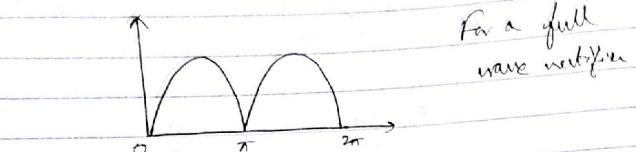
Amount of a.c. component of  $V$  for  $I$  at output of a rectifier  
Amount of d.c. component of  $V$  (or  $I$ )

$$I_{\text{rms}} = \sqrt{I_{\text{d.c.}}^2 + I_{\text{a.c.}}^2} \Rightarrow \frac{I_{\text{d.c.}}}{I_{\text{a.c.}}} = \sqrt{\frac{I_{\text{d.c.}}^2}{I_{\text{a.c.}}^2} - 1} \\ = \sqrt{\frac{I_{\text{m}}^2}{I_{\text{a.c.}}^2} - 1}$$

$$\Rightarrow \text{R.F.} \approx 1.21$$

$$\boxed{\text{R.F.} = 1.21}$$

## # Full Wave Rectifier



$$\bullet I_{dc} = \frac{2I_m}{\pi} \quad I_{rms} = \frac{I_m}{\sqrt{2}}$$

$$\eta = \frac{P_{dc}}{P_{ac}} = \frac{I_{dc} \cdot R_L}{I_{rms}^2 (R_L + r_f)}$$

$$= \frac{8}{\pi^2} \left( \frac{1}{1 + r_f/R_L} \right)$$

$r_f \ll R_L$

$$\boxed{\eta = \frac{8}{\pi^2} = 0.812}$$

$$\eta \cdot 1 = 81.2\%$$

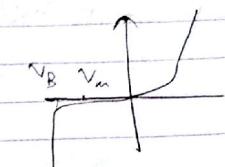
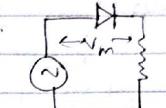
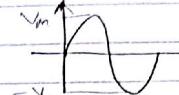
$$\frac{I_{ac}}{I_{dc}} = \sqrt{\frac{I_{rms}^2}{I_{dc}^2} - 1} = \sqrt{\frac{\pi^2}{8} - 1} \approx 0.48$$

$$\boxed{R.F = 0.48}$$

almost 1/3 of RF of Half Wave

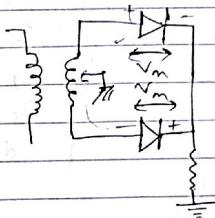
# Peak Inverse Voltage ( $PIV$ )  $\rightarrow$  max reverse  $V$  that a diode can withstand

• Half Wave



$V_m$  is very close to  $V_B$

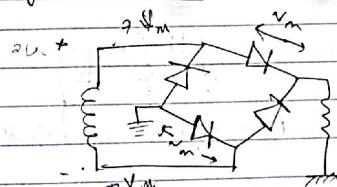
• Full Wave



at any instant, voltage across any diode =  $2V_m$

So higher rating  $2V_m$

• Bridge rectifier



In 1 half cycle

Rating Voltage across each diode =  $V_m$

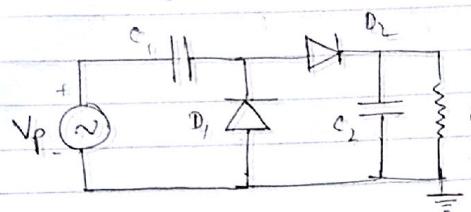
Rating =  $V_m$

# Comparison b/w diff rectifiers

Particulars	Half Wave	Full Wave	Bridge
No of <del>diodes</del> diodes	1	2	4
Need of transformer	No	Yes	No
Efficiency	40.6%	81.2%	81.2%
Ripple factor	1.21	0.48	0.48
$PIV$	$V_m$	$2V_m$	$V_m$

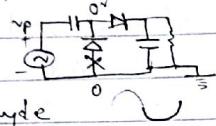
## 2. Voltage Multipliers

### (a) Voltage doubler

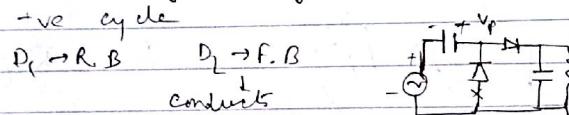


$R_L \rightarrow$  should be very high  
↓ con

1st half cycle  
 $\frac{V_p}{2}$  to cycle  
C will start charging, but cannot  
D<sub>1</sub> → reverse biased (unbiased)



-ve cycle  
D<sub>1</sub> → F.B. C →  $\frac{V_p}{2}$   
C charged gets discharged as D<sub>2</sub> conduction

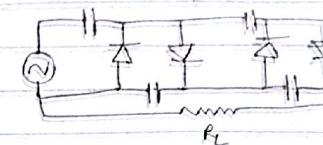


C<sub>2</sub> → charged ( $R_L \rightarrow$  high → negligible current through R<sub>L</sub>)

$$V_p + V_{p/2} = V_{out} \Rightarrow V_{out} = 2V_p$$

- (1) no (little) current should flow through R<sub>L</sub>
- (2) To prevent discharge of C<sub>2</sub> through R<sub>L</sub>, so the voltage ~~does~~ 2V<sub>p</sub> doesn't drop off

### (c) Voltage Quadriplifier

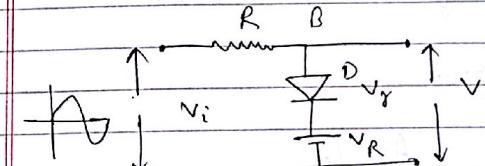


For higher multipliers, add a diode circuit and flip the pos of R<sub>L</sub> top/bottom.

### # Wave Shapers

#### Clipping circuit

##### Positive Clipping:



$V_p \rightarrow$  cut-in voltage

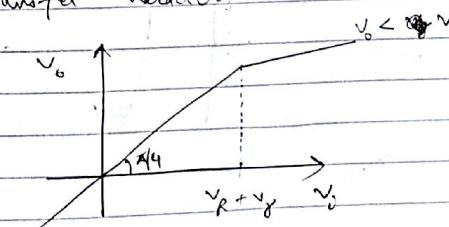
Whenever whenever  $V_B \geq V_R + V_d$ , diode will conduct

As long as  $V_i < V_R + V_d$   
 $V_o = V_i$

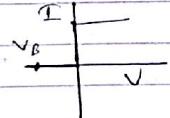
When  $V_i \geq V_p + V_d$

D → F.B., surely  $V_o < V_i$   
→ because of drop iR

#### • Transfer Characteristics



#### Ideal diode

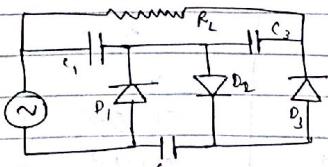


$V_d = 0$  for ideal diode

$R_f = 0$

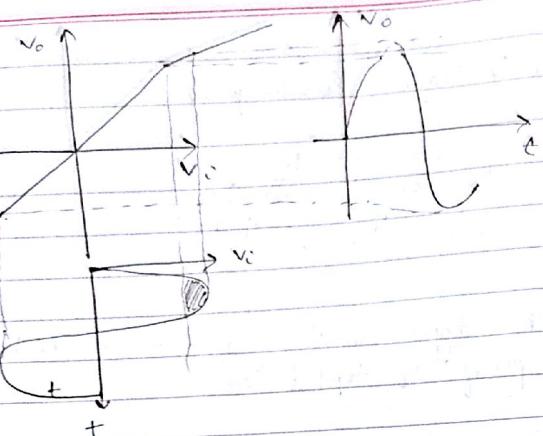
$R_{re} = \infty$

### (b) Voltage Tripler



$$= 0.2 \times 10^{-6} T^2 R_C$$

$$V_i - V_f - V_R = iR$$

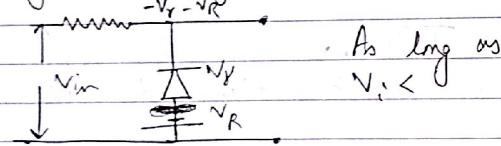


Also called slicing circuit, or amplitude limiter

$$V_i - (R + r_f)i = 0 \Rightarrow i = \frac{V_i}{R + r_f}$$

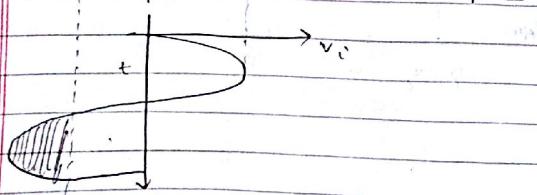
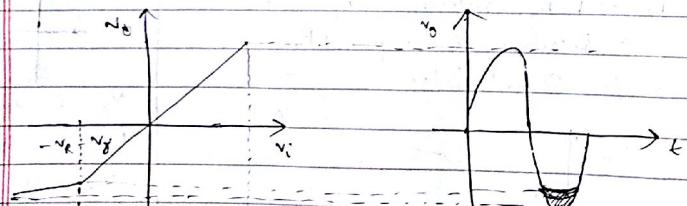
$$V_o = \frac{V_i + f_i}{R + r_f} \Rightarrow \frac{V_o}{V_i} = \frac{1}{R + r_f}$$

### # Negative Clipping Circuit

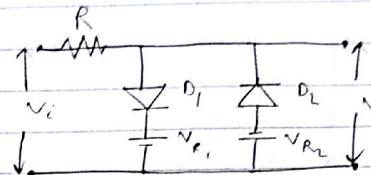


As long as  
 $V_i < -V_R - V_F$

for  $V_i < -V_R - V_F$ ,  $D \rightarrow F.B.$ , then  $V_o < V_i$   
else  $D \rightarrow R.B. \rightarrow V_o = V_i$



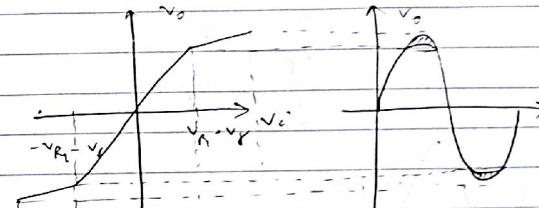
### # Clipping at 2 independent levels



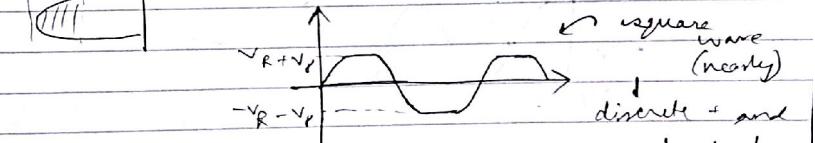
$$\text{For } V_i < -V_{R1} - V_F \rightarrow D_2 \rightarrow F.B. \quad V_o > V_i \\ D_1 \rightarrow R.B. \quad (\text{i.e. } V_o < V_i)$$

$$-V_{R1} - V_F < V_i < V_{R1} + V_F \rightarrow D_1, D_2 \rightarrow R.B. \Rightarrow V_o = V_i$$

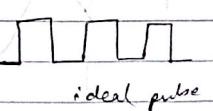
$$V_i > V_{R1} + V_F \rightarrow D_1 \rightarrow F.B. \quad D_2 \rightarrow R.B. \Rightarrow V_o < V_i$$



$$\text{If } V_{R1} = V_{R2} = V_R$$

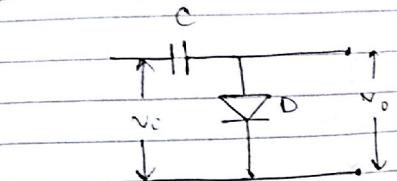


Hence, clipping at 2 independent levels  $\rightarrow$  also called the slicing circuit



ideal pulse

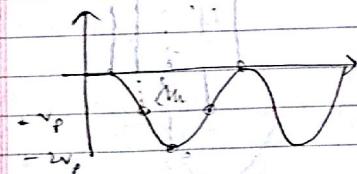
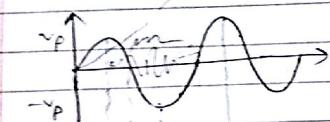
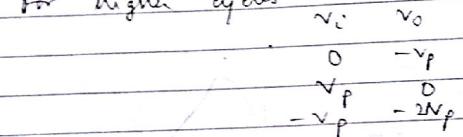
## # Clamping Circuit



+ve 1<sup>st</sup> cycle

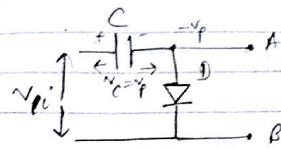
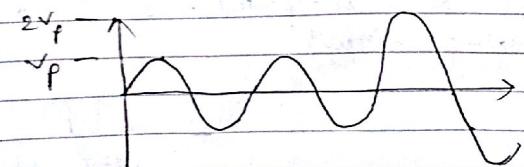
$D \rightarrow F.B$  and  $C$  starts charging  
 $C$  can charge max to  $V_c$ .  $V_c \approx V_i$  if  $V_f \rightarrow 0$

$V_o = V_i - V_c = V_i - V_p$   
 For first <sup>greatest</sup> cycle  $V_o = 0$ , as  $C \rightarrow$  uncharged  
 for higher cycles



### Drawbacks

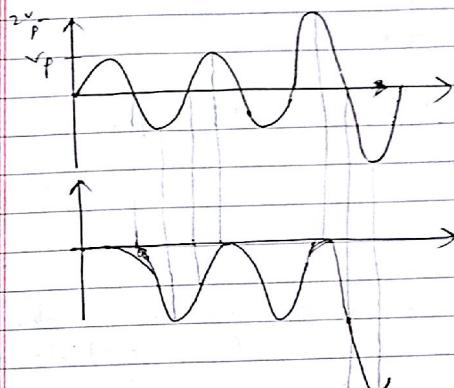
If input voltage fluctuates



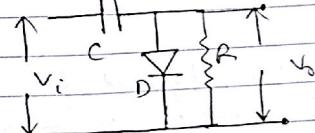
during ~~the~~ first 2 cycles (when  $V_p$  is steady),  $D$  can never be forward biased

When  $V_i = 2V_p$ ,  $D \rightarrow F.B \Rightarrow C$  starts charging  
 $C \rightarrow$  will be charged upto  $2V_p$

$$\therefore V_o = V_i - 2V_p$$

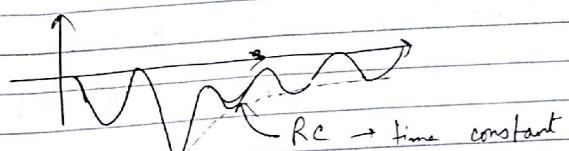


Now if the voltage returns to  $V_p$ , then  $D$  will never be forward biased

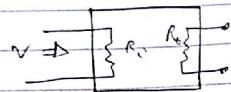
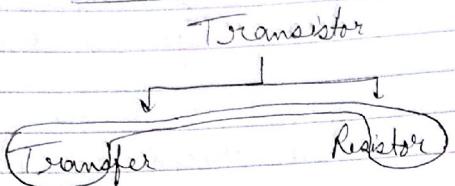


R should be chosen such that  
 $r_p < R < r_s$

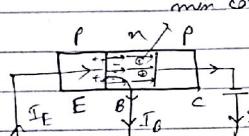
In this case if  $V_i$  goes from  $V_p$  to  $2V_p$  to  $V_p$



## Transistor



$p\ n\ p$  —  $n\ p\ n$  → 2 types  
electrical contact  
min curr



in B, some holes combine with  
 $e^-$  in B → constitute the base  
current. no of such holes  
(only few)

If B-C is F.B. →  
large current will flow through the B → may  
damage, and not reg. also.

B-C is R.B.

∴ E-B is F.B. → holes have diffused from E to B  
→ so holes in B is not only due to min curr in B, but also from E. Hence large amt of charge will flow through B-C under R.B.

At Node X → using KCL →

$$I_E = I_B + I_C$$

Intuitively, if  $I_B$  increases,

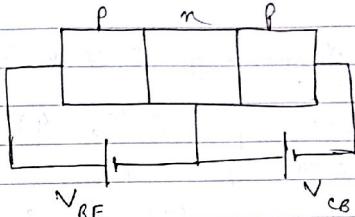
Biasing : Application of low d.c input voltage to a device so that a scaled voltage can appear across the device and a scaled current can flow through the device

$M_e > M_h \rightarrow$  electrons more mobile than holes

$$f = \frac{1}{T} \rightarrow \text{switching speed of device}$$

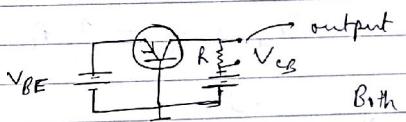
for high freq operation → use n-p-n

for low freq / audio freq operation → use p-n-p



### Modes of Operation -

- Common base (CB) mode



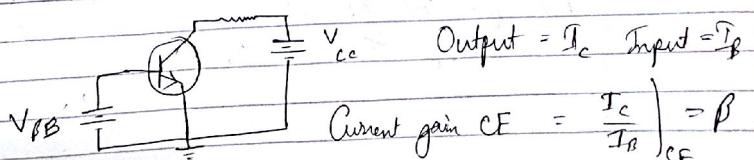
Both input & output has the  
base common

input current =  $I_E$

output current =  $I_C$

$$\text{Current gain at CB} = \frac{I_C}{I_E}_{CB} = \alpha < 1$$

- Common emitter mode (CE)



Output =  $I_C$  Input =  $I_B$

$$\text{Current gain CE} = \frac{I_C}{I_B}_{CE} = \beta$$

$$I_F = I_B + I_C$$

$$\Rightarrow \frac{I_F}{I_C} = \frac{I_B}{I_C} + 1$$

$$\Rightarrow \frac{1}{\alpha} = \frac{1}{\beta} + 1$$

$$\Rightarrow \alpha = \frac{\beta}{1+\beta}$$

$$\Rightarrow \beta = \frac{\alpha}{1-\alpha}$$

# for a transistor  $I_C < I_E$   
 $\Rightarrow \alpha < 1$

Now width of base is less and (is thinly doped)

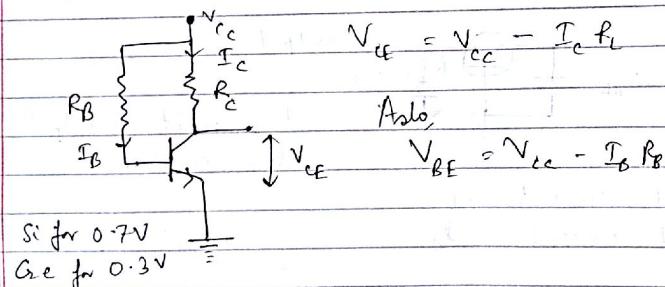
Value of  $\alpha$  generally 0.98 to 0.99

$$\text{Taking } \alpha = 0.98 \Rightarrow \beta = \frac{0.98}{1-0.98} = 49$$

$$\alpha = 0.99 \Rightarrow \beta = 99$$

Typically  $\beta$  ranges 6/16 to 50 to 100  
 $I_C, V_{CE} \rightarrow$  specifications of the device  
Methods of Biasing

# Base Resistor Method



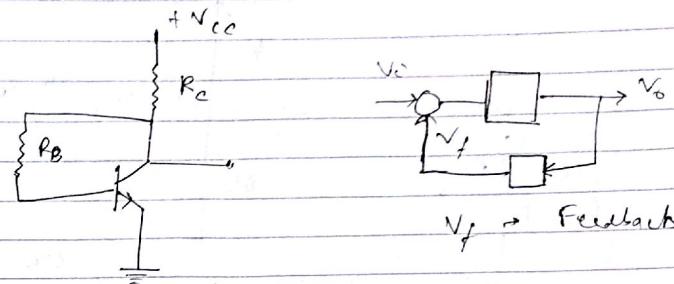
To make BE reverse biased

$$V_B > V_E \Rightarrow V_{BE} > 0$$

$$\Rightarrow R_B < \frac{V_{CC}}{I_B}$$

for practical transistors may si  
 $V_{BE} \geq 0.7V$

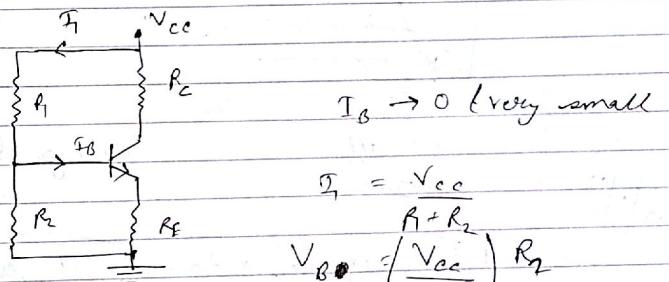
(2) Collector to base feedback method



$$V_{CC} = (I_C + I_E) R_C + V_{CE} \quad (1)$$

$$V_{CC} - (I_C + I_B) R_C - I_B R_B = V_{BE} \quad (2)$$

Voltage divider method of biasing



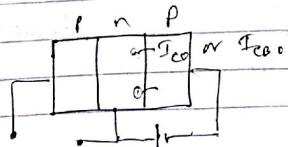
For operation,  $V_{BE} > 0$

$$I_C = f(\beta, I_{CO}, V_{BE})$$

$I_{CO} \rightarrow$  current due to minority carriers from B to C

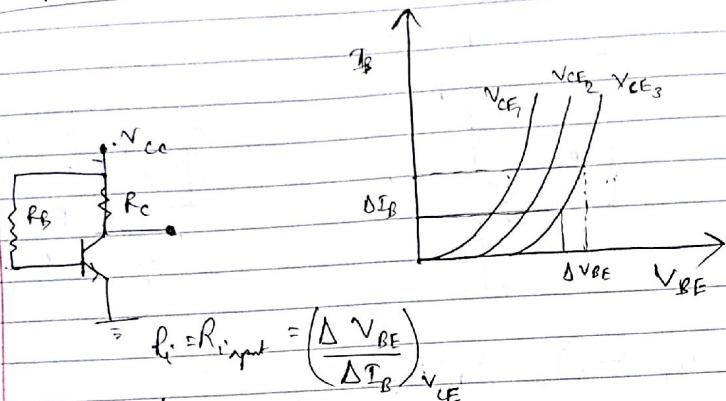
0 → stands for emitter open

Voltage divider method is the most stable method for biasing

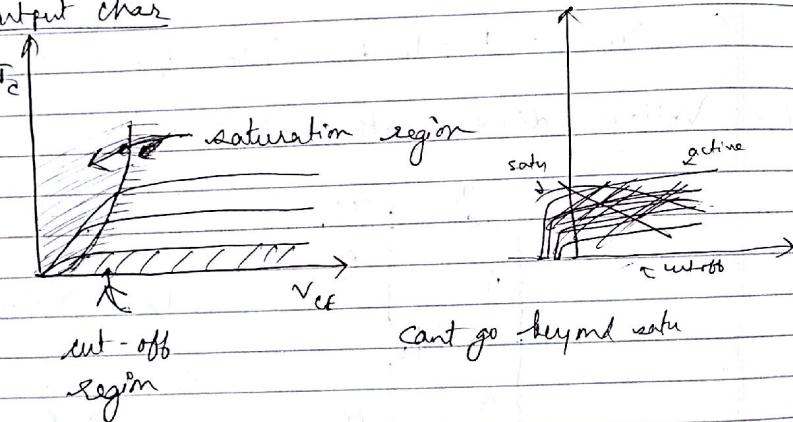


$$\beta =$$

## # Input ( $V-I$ ) Characteristics



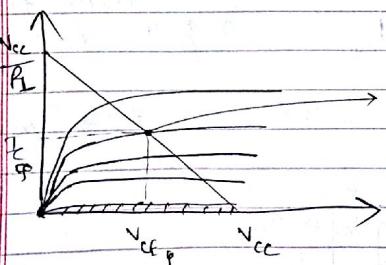
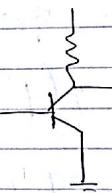
## # Output char



12/3/16

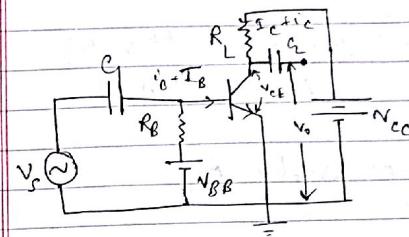
Never operate a transistor at cut-off, and very rarely to saturation

$$V_{CC} = I_C R_C + V_{CE}$$



## # Amplifier

An amplifier is a transistored circuit by which the amplitude of any a.c. signal in terms of its voltage or current can be increased



$$X_C = \frac{1}{\omega C}$$

$C$  = decouples the d.c. but couples the input a.c. signal to the base of the Transistor

### Common Emitter Amp

$i_b, i_c \rightarrow$  a.c. component of current  
 $I_b, I_c \rightarrow$  d.c. current in absence of  $V_c$

$V_{CC} = (I_c + i_c) R_L + V_{CE}$   
 $V_{CC} \rightarrow$  fixed  $\Rightarrow V_{CE} \rightarrow$  will change due to change in base current  $\Rightarrow$  collector current  $(I_c + i_c)$  will change

$C_L \rightarrow$  will block d.c. component of  $I_{C(\text{net})} \rightarrow$  allows  $i_c$  to flow

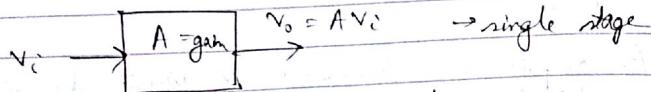
## # Classification of Amplifiers

1. Based on selection of operating point  
- Class A, Class B, Class AB, Class C

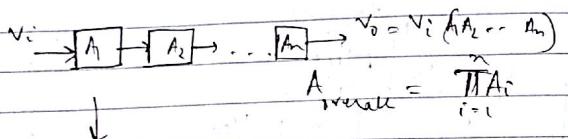
2. Based on frequency of operation  
(i) AF amplifier (20Hz - 20kHz)  
(ii) RF amplifier (above 20 kHz)

3. Based on the type of signal  
(i) Voltage amplifiers  
(ii) Current amplifiers

1, 2, 3 → called single stage amplifier



A - fixed for given amplifier



4. Multistage Amplifier or Coupled Amp

#### • Class A amplifier :

In class A operation of an amp, the operating point is set such that for the 100% of the i/p signal cycle, the transistor remains in the active region and can amplify the signal over the complete 1 cycle. In this mode of operation, the efficiency of the amplifier is only 25%. Voltage gain in class A op<sup>+</sup> is very high & at the same time, the noise present at the o/p of the amplifier is also high.

#### • Class B amplifier :

In class B op<sup>+</sup>, the operating point of the transistor is set such that for the 50% of the input signal cycle, the transistor will remain on and can amplify the signal. Efficiency of class B amp is 78.57%. Voltage gain is low and at the same time, the noise present at o/p of amp is also low.



half of it is in the cutoff region

#### • Class AB amplifier

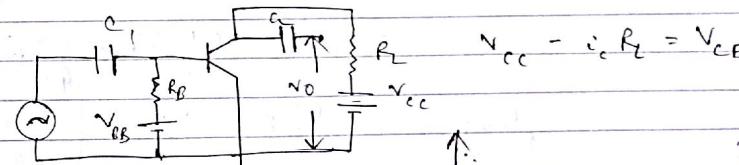
Class AB op<sup>+</sup> of an amp is not exactly same as class A or class B, but in b/w them, in this mode of amp the transistor will remain in the active region for the 75% of the input signal cycle and can amplify the signal. Here  $\eta_A < \eta_{AB} < \eta_B$ . Also voltage gain & noise at o/p is less than that of A, but more than that of B.

#### • Class C amplifier :

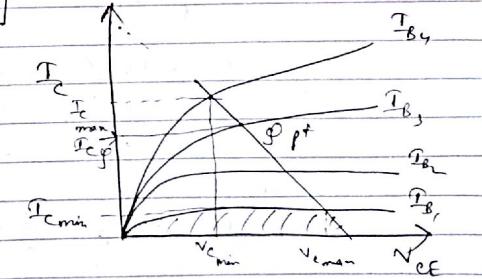
In class C amplifier, the operating point is set such that for the 25% of the i/p signal cycle, the transistor will remain active & can active.  $\eta_C \approx 90\%$ . Voltage gain is very low and also noise at o/p is low.

Thus class C amp is very popular as a low noise amp

#### Class A amplifier



When R\_L is set at its op pt, then  $v_{ce}$  and  $i_c$  will start to swing due to the application of a.c signal. The max value of collector current is  $i_{cmax}$  & corresponding collector voltage is  $v_{cmin}$  and at corresponding current is  $i_{cmin}$ , i.e. nearly at cut off.



The minimum collector voltage is  $V_{cmin}$  → corresponding current →  $I_{cmax}$  → nearly at saturation

As the operating pt swings equally about m either side of Q point, the amplitude of the a.c. collector current  $I_m$  is

$$V_m \rightarrow I_m = I_{max} - I_{min}$$

$$V_m = \frac{V_{max} - V_{min}}{2}$$

### Power Calculation

$$i_c(t) = I_m \sin \omega t + I_{cg}$$

operating point set by  
biasing d.c. value of current

$$V_{CE}(t) = V_c(t) = V_{cc} - i_c(t) R_L$$

$$= V_{cc} - (I_{cg} + I_m \sin \omega t) R_L$$

$$P \text{ dissipated across load } P_C = i_c^2(t) R_L$$

$$P_C(\text{avg}) = P_L(\text{avg}) = \int_0^T i_c^2(t) R_L dt$$

$$= \frac{R_L}{T} \left[ I_{cg}^2 T + 2 I_{cg} I_m \sin \omega t + I_m^2 \left( 1 - \frac{\cos \omega t}{2} \right) \right] dt$$

$$= \frac{R_L}{T} \left[ \frac{I_{cg}^2 T}{2} + I_m^2 T - \frac{I_m^2}{4} \left( \cos \omega t \right)_0 \right]$$

$$\boxed{P_C(\text{avg}) = I_{cg}^2 R_L + \frac{1}{2} I_m^2 R_L} \quad \text{--- (1)} \rightarrow \text{follows trivially}$$

Gain = Ratio of incremented value to peer value

$$= \frac{V_2}{V_1} \approx \frac{I_2}{I_1}$$

Now

$$P_{ac} \text{ at o/p} = \frac{1}{2} I_m^2 R_L = \frac{1}{2} I_m V_m = I_{avgm} V_{avgm}$$

• Avg power dissipated in transistor:

$$P_T = \frac{1}{2\pi} \int_0^{2\pi} i_c(t) V_c(t) d(\omega t) =$$

$$= V_{cc} I_{cg} - \frac{I_{cg}^2 R_L}{2} - \frac{1}{2} I_m^2 R_L \quad \text{--- (2)}$$

from (1) & (2)

$$\Rightarrow P_{total} = P_L + P_T \quad \text{at o/p}$$

$$= V_{cc} I_{cg}$$

- Device which doesn't lose power  $\rightarrow$  active device
- " " " " "  $\rightarrow$  passive device

$$V_{cc} I_{cg} \rightarrow P_s \text{ (supplied dc power)}$$

$$\eta = \frac{P_{ac}}{P_s} = \frac{\frac{1}{2} I_m V_m}{V_{cc} I_{cg}}$$

$$= \frac{1}{2} \times \frac{(I_{max} - I_{min})(V_{max} - V_{min})}{V_{cc} I_{cg}}$$

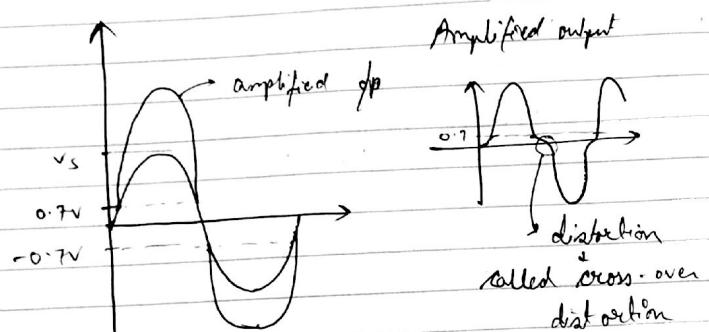
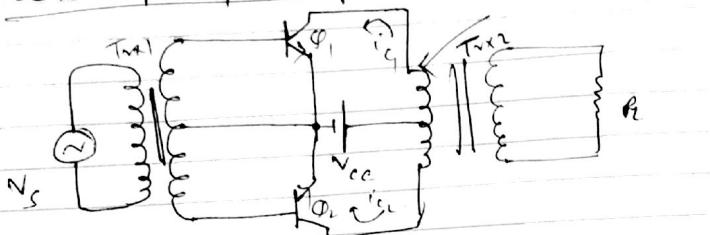
for an ideal transistor characteristics

$$V_{min} = 0 \quad I_{min} = 0$$

$$V_{max} = V_{cc} \quad I_{max} = 2 I_{cg} \quad (g \rightarrow \text{constant to be assumed})$$

$$(2)_{max} = \frac{1}{2} \times 2 = \frac{1}{4}$$

$$\Rightarrow \boxed{\eta_{max} = 25\%}$$

# Class B push-pull amplifier

B/W  $-0.7V$  and  $0.7V$  both transistors remain cut-off

So  $V_{op}$  is applied (minimum of  $0.7V$ ) to both emitter

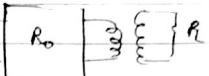
net current through primary =  $i_p$

(Push pull  $\rightarrow$  during one half  $\rightarrow$  one  $\oplus$  pushes the current & the other pulls the current)

Advantages:

- i)  $\eta \approx 78.5\%$  which is quite high
- ii) as transformer is a very good impedance matching device thus the i/p signal & output load can be connected with the Amplifier very easily

$$\boxed{R_o} \quad \boxed{R_L} \quad \text{for max power } R_o = R_L \rightarrow \text{but not always possible}$$



Let  $R_o = 50\Omega$ ,  $R_L = 10k\Omega$

Transformer can be adjusted such that power is max by making  $X \approx R_o$  and  $X \approx R_L$

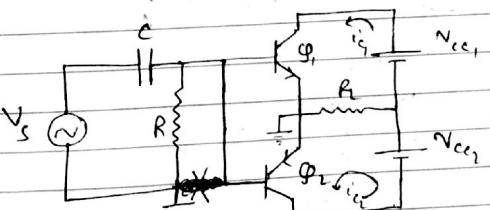
- iii) Keeping the emitter terminals of both the transistors at -ve potential one can overcome the problem of cross over distortion

Disadvantage

i) bulky large size & weight & thus it increase wt, volume & cost of the whole ckt

ii) At high freq operation the ~~core~~ cores of the txr will start to vibrate & produce some humming sound  
 $\rightarrow$  due to air gap b/w core sheet  
 $[\because \phi_B \propto f^{1.6 \text{ to } 2} \Rightarrow$  more flux  $\Rightarrow$  more loss due to eddy  $\rightarrow$  causes vibration (?)].

iii) Both transistors should be of same type, i.e. both have same gain and other parameters so that they can amplify both the halves asymmetrically so that no distortion results.

# Complementary symmetry class B push-pull Amplifier

When both n-p-n & p-n-p or n channel FET & p-channel FET used in same ckt

called complementary ckt

cross-over distortion can't be avoided

Efficiency

The collector current and voltage being half sinusoidal, the rms collector  $V_{ce}$  and rms collector  $I_{ce}$  are given by

$$V_{ce} = \frac{V_{cm}}{2}, \quad I_{ce} = \frac{I_m}{2} \quad (\text{mean value of } V/I)$$

a.c power o/p from one (R)

$$P_{ac} = V_{ce} I_{ce} = \frac{V_{cm} I_{cm}}{4}$$

Now  $V_{cm} = V_{cc}$  ( $\because$  max  $V_{ce}$  occurs when no drop)

$$\therefore P_{ac} = \frac{V_{cc}^2}{4R_L} \quad (R_L \rightarrow \text{resistance due to coil})$$

Total a.c power o/p

$$(P_{ac})_{\text{net}} = \frac{V_{cc}^2}{4R_L} \times 2 = \frac{V_{cc}^2}{2R_L}$$

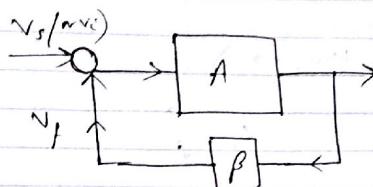
$$\text{Total d.c power supplied } (P_s)_{\text{net}} = 2V_{cc} I_{dc} = 2V_{cc} \left( \frac{I_m}{\pi} \right)$$

$$\eta = \frac{(P_{ac})_{\text{net}}}{(P_s)_{\text{net}}} = \frac{V_{cc}^2 / 2R_L}{2V_{cc} I_m / \pi}$$

$$\text{again } I_m = I_{em} = \frac{V_{cc}}{R_L}$$

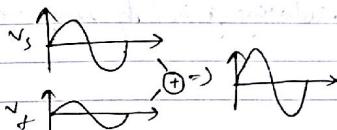
$$\therefore \eta = \frac{V_{cc}^2 / 2R_L}{2V_{cc}^2 / \pi R_L} = \frac{\pi}{4}$$

$$\Rightarrow \boxed{\eta = \frac{\pi}{4} = 0.785} \quad \boxed{\eta \% = 78.5\%}$$

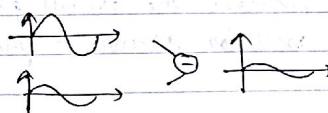
Feedback Amplifier

feedback network

When  $V_s$  and  $V_f$  are in the same phase  $\rightarrow$  +ve feedback  
 $\rightarrow$  addition



When  $V_s$ ,  $V_f$  opposite phase  $\rightarrow$  -ve feedback

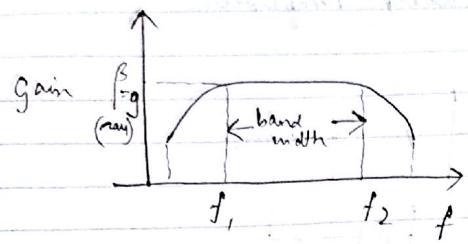


2 Types : • Positive feedback amplifier }  
• Negative feedback amplifier }  
Voltage Amp Current Amp

Can be either series or shunt

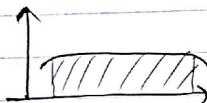
(\*) We use negative feedback to an amplifier because of :

- to reduce the gain of the overall amplifier
- to increase the bandwidth of an amplifier
- to increase the stability of an amplifier
- to increase the input impedance of an amplifier and to reduce the o/p impedance of an amplifier
- to reduce the distortion of the amplifier ckt
- to reduce the noise at the o/p of the amplifier

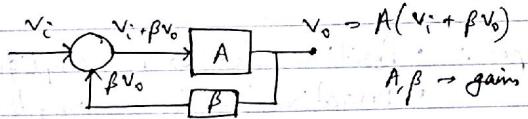


$$g(f_2 - f_1) = \text{gain} \times \text{BW} = GBW$$

For a given amplifier  $GBW$  is constant. By points 1 & 2, we can increase  $B/W$  by reducing gain (by using +ve feedback)



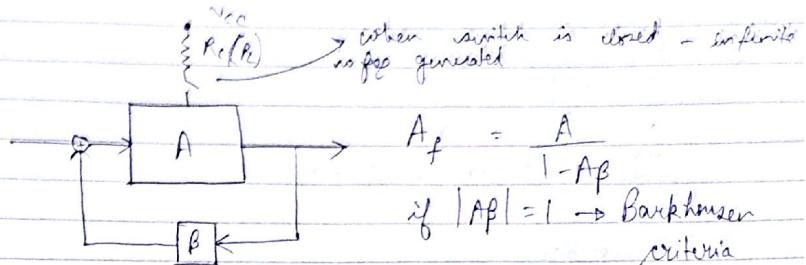
- ② Positive feedback increases the overall gain of the amplifier and used in the oscillator circuit to produce oscillation



$$\begin{aligned} V_o &= A(V_i + \beta V_o) \Rightarrow AV_i = V_o(1 - A\beta) \\ &\Rightarrow \frac{V_o}{V_i} = \frac{A}{1 - A\beta} = A_f \rightarrow \text{feedback gain} \end{aligned}$$

For +ve feedback

$$\begin{aligned} 1 - A\beta &< 1 & (\beta \text{ adjusted such that } \beta < \frac{1}{A}) \\ \Rightarrow A_f &> A \end{aligned}$$



### Conditions for oscillations

- There must be a +ve feedback
- Should satisfy Barkhausen criteria.  $|A\beta| = 1$

### Oscillators

Sinusoidal  
osc

Non-sinusoidal Osc  
or Relaxation type

Multivibrator



- Multivibrator  $\rightarrow$  Nonstable  
 $\rightarrow$  Bistable (e.g. flip flop)  
 $\rightarrow$  Astable (used as a clock)

#

Sinusoidal Osc -  
negative resistance type

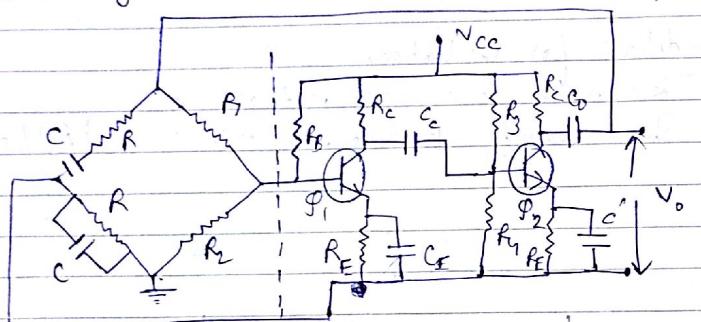
- +ve feedback type
  - RC osc
  - LC osc

## # RC Oscillators



Wien Bridge  
RC phase shift osc

## # Wienbridge Osc



~~RC osc part~~  
Feedback part

Bridge  $\rightarrow$  causes no phase change

2 amplifiers used  $\rightarrow$  2 CF causes net phase change of  $\pi + \pi = 2\pi$

So,  $V_{\text{feedback}}$  same phase as  $V_{\text{in}}$

# For the bridge on the left side:

$$\frac{R_f}{R_2} = \frac{R + \frac{1}{j\omega C}}{\frac{R(j\omega)}{R + \frac{1}{j\omega C}}}$$

$$\Rightarrow \frac{R_f}{R_2} = 2 + \frac{R^2 - 1/\omega^2 C^2}{R/j\omega C}$$

$$\Rightarrow j\omega(R^2 - 1/\omega^2 C^2) = 0 \Rightarrow \cancel{R^2 - 1/\omega^2 C^2}$$

Garg's  
Date \_\_\_\_\_  
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Acoustics  
Date \_\_\_\_\_  
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$$\Rightarrow \omega = \frac{1}{RC} \Rightarrow f = \frac{1}{2\pi RC}$$

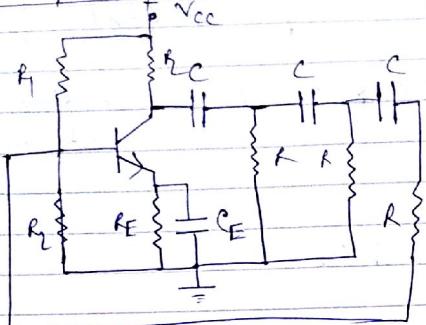
$$\frac{R_f}{R_2} = 2 \Rightarrow R_f = 2R_2 \quad \text{- Condition for sustaining oscillation}$$

## # Advantages of Wienbridge:

- i) Overall gain is high since a 2 stage amplifier is used
- ii) The circuit gives a very good sine wave off
- iii) Frequency stability is also good
- iv) Frequency of oscillation can be easily varied (by varying  $R$  &  $C$ )
- v) If the resistance  $R_f$  is replaced by a thermistor which has a -ve temperature coeff of resistance, the amp of osc is stabilised against the variation caused by the other resistor  $R_2$  due to temperature

## # Disadvantage

- i) Large no of components are needed for a 2 stage amp
- ii) One cannot generate very high frequency using this oscillator

# RC phase shift oscillator

$$\varphi = \varphi_0 (1 - e^{-t/T_C})$$

$$\varphi = \varphi_0 e^{t/T_C}$$

freq of osc:  $f = \frac{1}{2\pi\sqrt{6} CR}$

Condition for sustaining osc  $\left| h_{fe} \right| = 56$

# Negative feedback amp → effects  
introduces following modifications -

- i) The gain is reduced & stabilized w.r.t. the variations in  $(\beta)$  parameters.
- ii) The non-linear distortion is less so that the signal handling capacity of the amplifier increases.
- iii) The input impedance can be changed by suitably combining the feedback.
- iv) The band-width of the Amp increases.
- v) Phase distortion is reduced.
- vi) Noise level is lower.

$$A_f = \frac{V_o}{V_i} = \frac{A}{1 + A\beta}$$

(i) Stability of gain

gain should be stable, shouldn't vary with any parameters of the  $(\beta)$  Amp

$$A_f = \frac{A}{1 + A\beta}$$

$$dA_f = \frac{(1 + A\beta)dA - A\beta dA}{(1 + A\beta)^2} = \frac{dA}{(1 + A\beta)^2}$$

$$\Rightarrow dA_f = \frac{dA}{1 + A\beta} \frac{A_f}{A}$$

$$\Rightarrow \frac{dA_f}{A_f} = \frac{1}{1 + A\beta} \frac{dA}{A}$$

$$S = \frac{dA_f}{A_f} / \frac{dA}{A} = \frac{1}{1 + A\beta} \rightarrow \text{sensitivity of the transfer gain}$$

Dessensitizing  $D = \frac{1}{S}$

As  $|D| > 1$ , then for -ve feedback, the percentage change in  $A_f$  is less than that in  $A$ . Thus the overall gain stability is much better.

(ii) Decrease in non-linear distortion

If  $V_s$  is the applied i/p voltage, then o/p voltage of the amplifier without feedback =  $A V_s = V_{os}$

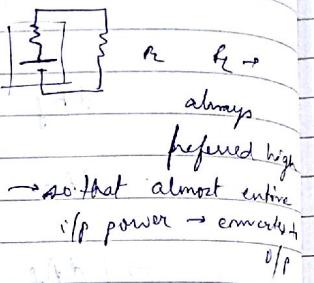
If  $V_D$  is introduced due to non-linearity of device, then it is assumed that the effective distortion voltage is  $V_D/A$  at the i/p of amp of gain  $A$ . In presence of -ve feedback both  $V_{os}$  and  $V_D$  will diminish. To keep  $V_{os}$  constant at its prev value, the i/p signal amplitude should be increased from  $V_s$  to  $V'_s = V_s (1 + A\beta)$ . When -ve feedback is applied

$V_{op}$  = distortion voltage with feedback → distortion component of o/p voltage. As the overall gain with -ve

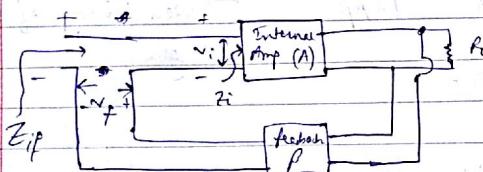
feedback is  $A/(1+A\beta)$  & i/p distortion voltage =  $V_o/A$

$$V_{df} = \frac{V_o}{A} \times \frac{A}{(1+A\beta)} = \frac{V_o}{1+A\beta}$$

$$\Rightarrow V_{df} < V_o$$



### (iii) Increase of i/p impedance



$$Z_i \text{ without feedback} = \frac{V_o}{I_i}$$

$Z_{if}$  (i/p impedance of Amp with feedback)

$$Z_{if} = \frac{V_i}{I_i}$$

$I_i \rightarrow$  nearly const

$$V_s = V_i + V_f = V_i + \beta V_o = (1 + A\beta) V_i$$

$$Z_{if} = \frac{V_i (1 + A\beta)}{I_i} = Z_i (1 + A\beta)$$

$$\Rightarrow Z_{if} = Z_i (1 + A\beta) \\ > Z_i$$

### (iv) Lowering of i/p noise

Undesired freq signal

$V_n \rightarrow$  noise voltage at i/p of Amp of gain A in abs of feedback.  $V_{on} \rightarrow$  o/p will be  $\frac{V_n}{1+A\beta} = V_{on} = A V_n$

In presence of feedback gain of the Amp reduces to  $\frac{A}{1+A\beta}$  also that o/p noise voltage becomes

$$V_{omp} = \frac{A}{1+A\beta} V_{on} = \frac{AV_n}{1+A\beta} = \frac{V_n}{1+A\beta}$$

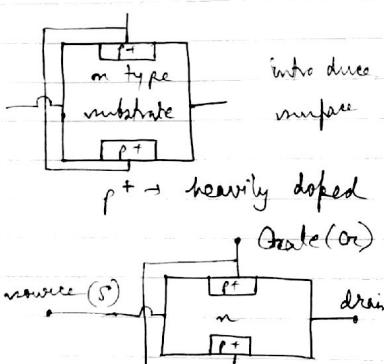
$$\Rightarrow V_{omp} < V_{on} \text{ as } 1 + A\beta > 1$$

# Field Effect Transistor (FET)

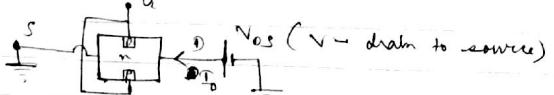
Junction field effect transistor (JFET)  
 p-channel n-channel

Metal Oxide Semiconductor Field Effect Transistor (MOSFET)

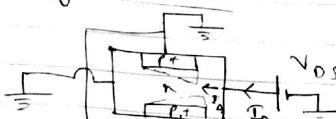
Unbiased Gate FET ( $I_{DSS}$ )  
 Depletion type MOSFET (D-MOS)      Enhancement type MOSFET (E-MOS)  
 p-channel n-channel p-channel n-channel



n-channel FET

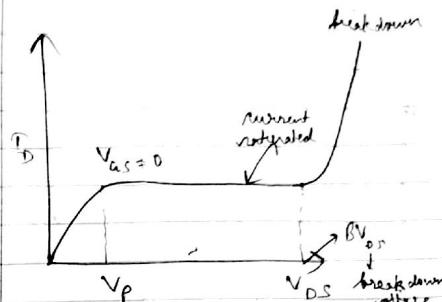


# Grounded Gate Condition



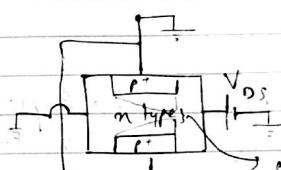
p  $\rightarrow$  highly doped  
 $\rightarrow$  width of depletion region  $\rightarrow$  very big

depletion region not horizontal because reverse bias decreases from right to left



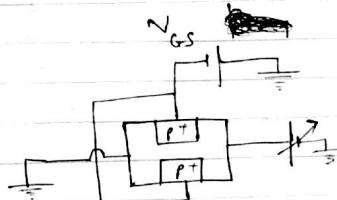
$V_p \rightarrow$  pinch-off voltage

\* physically depletion region will never touch a fixed current will flow (repulsion)



constant gap will be maintained

# Gate connected to -ve voltage

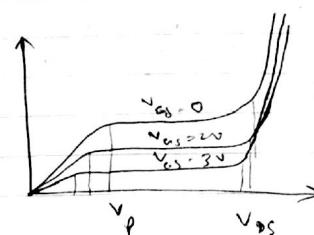


$$\text{Across } j^2 : \\ V_{\text{effective}} = V_{DS} - (-V_{GS}) \\ = V_{DS} + V_{GS}$$

$V_p$  and  $V_{\text{breakdown}}$  remain same

Now, for pinchoff carrier  $V_{DS} = V_p - V_{GS} \Rightarrow$  pinchoff occurs

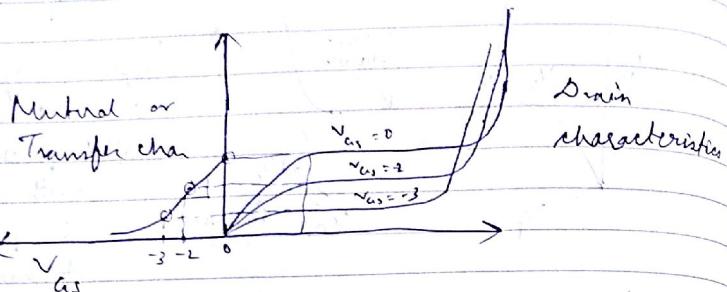
Drain characteristics of JFET



(Breakdown occurs earlier for  $V_{GS} > 0$ )

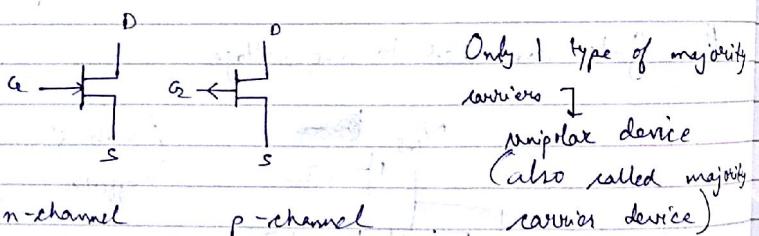
$$\frac{\Delta V_{DS}}{\Delta I_D} \rightarrow \text{drain resistance or channel resistance}$$

$$I_D = f(V_{DS}, V_{GS})$$



$$g_m = \frac{\Delta I_D}{\Delta V_{GS}} \rightarrow \text{mutual conductance}$$

$$r_d \times g_m = \frac{\Delta V_{DS}}{\Delta V_{GS}} = M \rightarrow \text{Amplification factor of the JFET}$$



#### # Comparison b/w BJT & FET

##### BJT

i) As both types of charge carriers flow through the device, hence it is a bipolar device

##### FET

i) Only 1 type of carrier that flows through the channel, and that depends on the type of the channel, & hence it is unipolar device

- ii) It is a current controlled device
- iii) As both the type of charge carrier flow through the device, thus a large amount of noise gets produced by the device due to recombination of these charges
- iv) As there is no recombination, thus lifetime problem is encountered
- v) I/p impedance of BJT is of the order of few 10s of kΩ, which is much lower than that of FET
- vi) BJT is very much sensitive to temperature and thus thermal runaway occurs for a BJT
- vii) As BJT is very large in size, thus we cannot use it in LSI
- viii) As more no of processing steps are involved in the fabrication of BJT, hence the fabrication procedure is complex & costly
- ix) It is a voltage controlled device
- x) As only 1 type of charge carriers are flowing through the device, hence no question of recombination. Thus FET is less noisy
- xi) As there is no recombination, so lifetime problem is not there in FET
- xii) I/p impedance  $\gg$  to channel region, because of reverse bias p-n junction, it is more than  $20 \text{ M}\Omega$  & thus higher than that of BJT
- xiii) Less temperature sensitive because FET can control its own current
- xiv) Because of very small size & low power consumption FET is very much suitable for LSI and especially in VLSI circuits

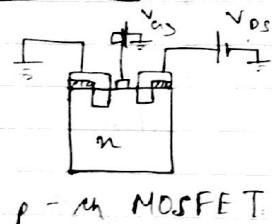
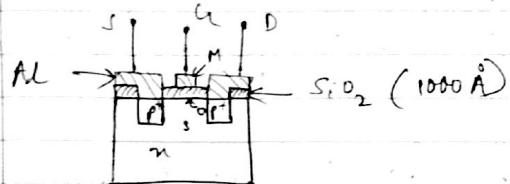
xv) As very less no of process steps are there in the fabrication of FET, hence FET is very costly

(ii) Because of very high gain & large bandwidth, BJT is very popular as an Amp.

(iii) Because of lower gain BJT, FET is not as popular as an Amp.

#

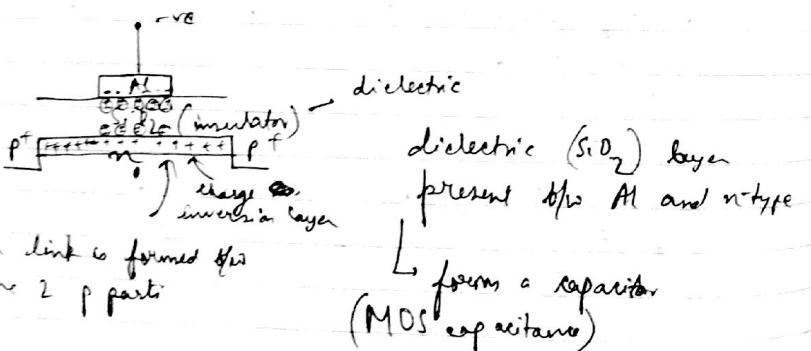
## MOSFET



$$V_G = 0$$

$\rightarrow$  no bias at the n-p junction  
 $\rightarrow$  no current

p-n MOSFET



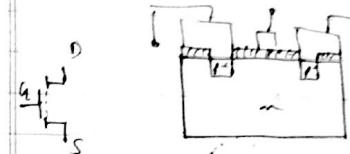
With increase in  $V_{DS}$ , the current will increase  
 $\rightarrow$  enhancement mode

$$\text{length of channel} = L = 25 \mu\text{m}$$

Time taken by charge carriers to move from D to S

$$t = \frac{L}{v_d} \propto \frac{1}{v_d}$$

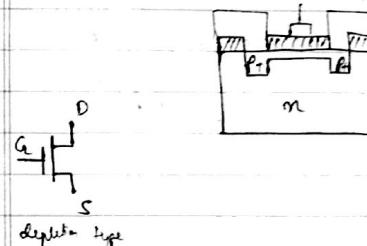
### Enhancement type



Grounded gate  $\rightarrow$  no current  
When  $V_G$  voltage applied across gate  $\rightarrow$  induced charge  
 $\rightarrow$  conduct

Initially no charge. On applying  $V_G$   $\rightarrow$  conduct  $\rightarrow$  current enhances

### Depletion type



Very similar to JFET

n  $\rightarrow$  used to absorb static charge developed (lightning friction)

### JFET

i) Gate directly connected with the channel

ii) JFET can operate only in depletion mode

iii) Input impedance of JFET is of order of few  $10^5$  to  $10^6$  M $\Omega$

iv) The current that flows from channel to gate is of  $10^{-6}$  to  $10^{-9}$  A

### MOSFET

i) Gate is insulated from the substrate or channel

ii) MOSFET can operate in depletion as well as enhancement mode

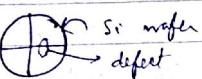
iii) Because of  $\text{SiO}_2$  layer b/w Gate & channel, the ip impedance of MOSFET is few  $100$  M $\Omega$

iv) Due to the presence of insulating  $\text{SiO}_2$  layer, the current that flows

9/4/13

~~Size of channel is negligibly small.~~

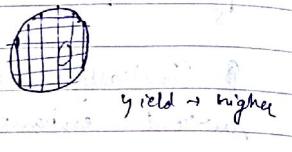
v) Because of low packing density, yield is low

 Si wafer  
defect

4 sectors, 2 pFET JFETs  
 $yield = \frac{2}{4}$

vi) Because of large size JFETs are not much used in the digital ICs

vii) Because of smaller size & low power consumption, MOSFETs are very much popular in LSI & VLSI ICs



b/w gate and channel is negligibly small.

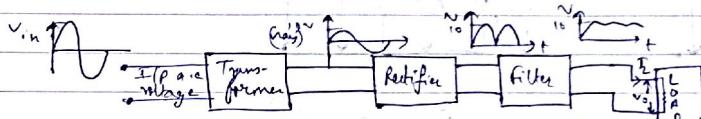
viii) Because of higher packing density, yield is more

## ④ Advantages of CMOS

i) In CMOS circuit, always 1 transistor out of 2 is on & thus the power dissipation is half

## D.C Power Supply

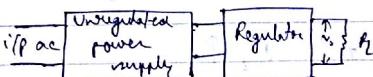
To run different semi-conductor devices like diode, transistors or ICs, a low voltage d.c is required



$\frac{dV_o}{dV_i}$  = Line regulation.  $V_{in} \rightarrow$  fluctuates  
 $\frac{dV_o}{dI}$  = Load regulation

I ideally  $\frac{dV_o}{dV_i} = 0\%$   
Load regulation =  $\frac{dV_o}{dI} = 0\%$  (ideally)

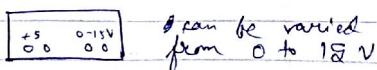
Thus, (Transformer  $\rightarrow$  Rectifier  $\rightarrow$  Filter)  $\rightarrow$  forms unregulated power supply because fluctuation of  $V_{in}$  will be reflected in  $V_o$



## # Voltage Regulator

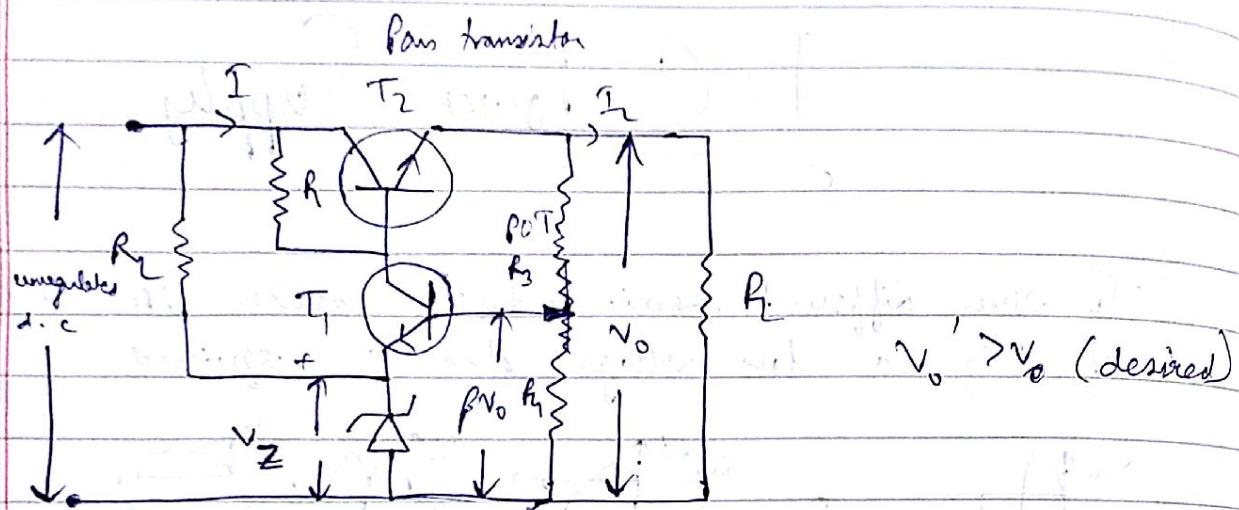
i) Fixed voltage regulator  $T_{-ve}$

ii) Variable voltage regulator



### iii) Uninterrupted Power Supply (UPS)

#### iv) Switching Mode power supply (SMPS)



$$i_{\text{POT}} = \frac{V_0}{R_3 + R_4}$$

$$(V_T)_{\text{Base}} = \frac{(V_0) R_4}{R_3 + R_4} = \beta V_0 \quad \beta = \frac{R_3}{R_3 + R_4}$$

$$\begin{aligned} \beta V_0 - V_z &\geq 0.7 \\ &= 0.7 \quad (\text{min for Si } \textcircled{K}) \end{aligned}$$

When  $V_0$  becomes  $V'_0$ :  $\beta V'_0 - V_z > 0.7$

$\beta \cdot F \rightarrow$  more  $F \cdot B \rightarrow I_E$  and  $I_L$  increases,  
current through  $T_1$ , current through  $T_2 \downarrow \rightarrow I_L \downarrow$

If  $\beta V_0 - V_z < 0.7 \quad I_L \uparrow$

② Main drawback: If load is shorted, large current flows through  $T_2 \rightarrow$  burns due to excessive heating