SinePi

Low jitter sine to square wave converter for FifoPi

By IanCanada Aug. 28, 2021 Ver. 0.9b

A. Introduction

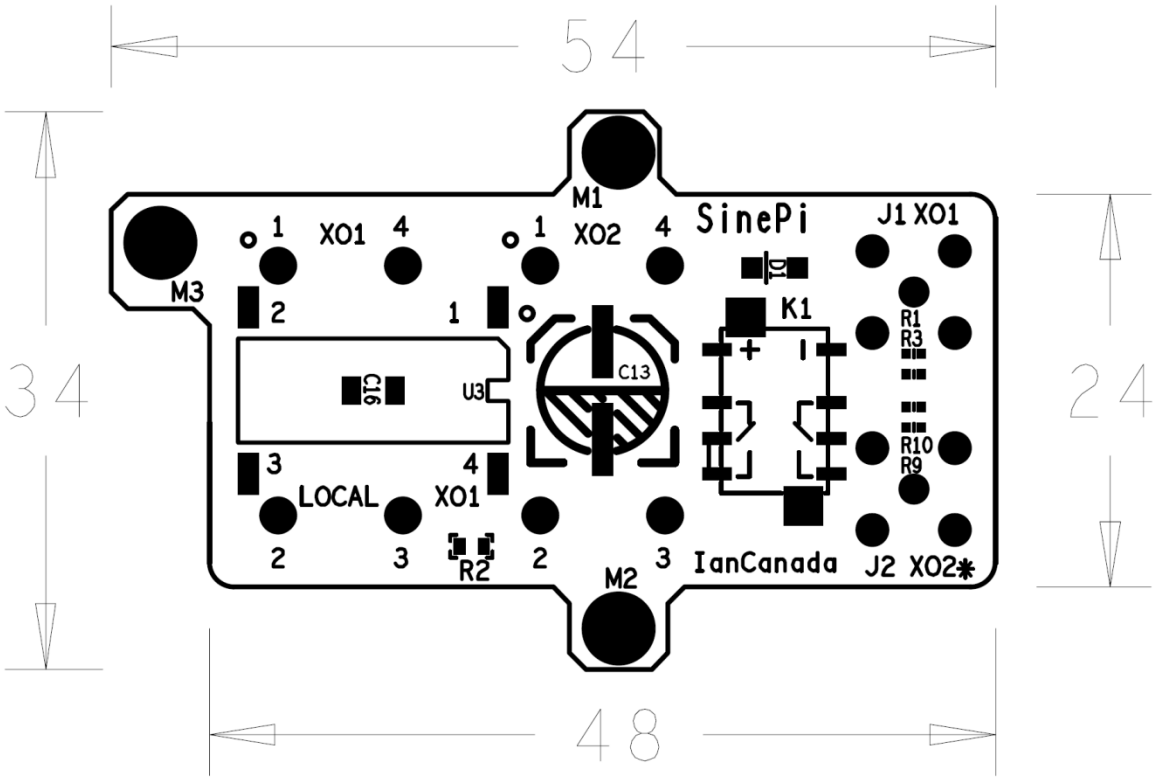
SinePi is a dual input low jitter sine to square wave converter board to adapt external high performance sine clock oscillators with FifoPi. It uses a specially designed architecture and topology to achieve best possible signal integrity and ultra-low additive jitter performance. A unified sine to square converter was implemented to eliminate the interference between two active converters. It also performs full signal isolation between SinePi and the unselected input channel to reduce both common mode and differential mode RF crosstalk.

With the optimized mechanical mounting scheme, SinePi can be firmly installed on top of a FifoPi.

B. Highlighted Features and Specifications

- One piece PCB architecture with full 8 pins connecting to the FifoPi XO sockets
- Unified sine to square converter to achieve best possible low jitter performance and signal quality
- Support both full sine mode with two external sine inputs and half sine mode with one local clock and one external sine input
- Flawlessly works with FifoPi Q1, Q2 and Q3
- Can disconnect both clock signal and ground from the unselected input channel by the on-board relay for a best possible clock isolation
- Enhanced NP0 and organic polymer capacitor power supply decoupling networks to ensure lowest possible power supply noise even under the mechanical vibration by addressing the piezoelectric effect
- Right angle SMA RF input connectors for a better system integration
- Metal film 0.1% tolerance resistors for the best possible low noise performance
- RF optimized four layers double side mounted PCB design to reduce ground impedance of the RF returning path and to control the matching impedance of the signal routes. The two additional inner ground plates can also provide a better shield for components between top and bottom side of the SinePi PCB
- Three specially designed standoff mounting holes for more reliable mechanical supports
- Input clock amplitude range: 0.5V - 5V Vpp (with 50 ohm termination)
- Input clock frequency range： 1-150MHz (sine or square wave)

C. Layout and Dimensions (in mm)

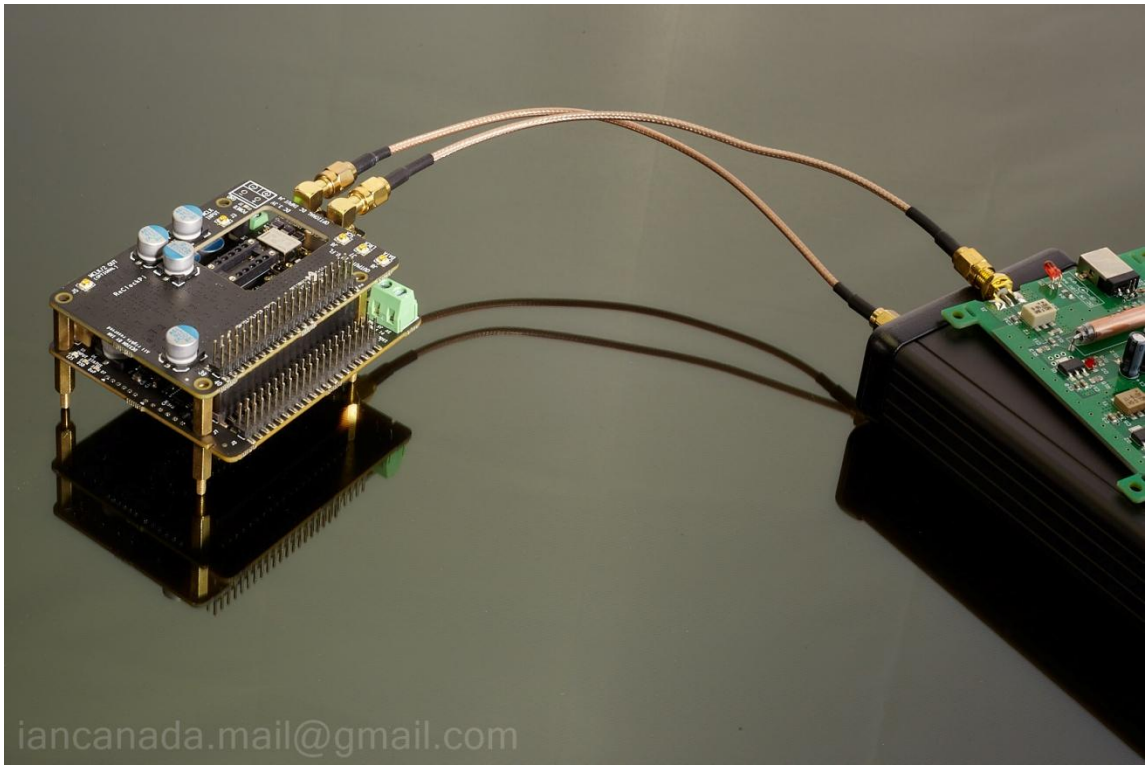


D. Getting start

1. Install the SinePi into the XO sockets on a FifoPi and make sure all the 8 pins are fully settled.
2. Install a ReClockPi or a ShieldPi on top of the FifoPi with standoffs, as well as the rest of the system.
3. Use SMA coaxial cables to connect two (into J1 and J2) or just one (into J1 or J2) external sine oscillators with the SinePi. The order doesn't matter.
4. Make sure the external sine oscillators are powered on and working properly.
5. Turn on the power of the whole system.
6. Enjoy the music.


SinePi
FifoPi Q3
ULTIMATE
LOCAL
iancanada.mail@gmail.com


OUTPUTS IN U.FL
DATA
LRCK
SCK
OPTIONAL DC INPUT J4
DC 3.3V
POWER
GND
iancanada.mail@gmail.com



E. Application notes

1. How to set up the half sine mode for one external sine clock and one local XO configuration?

Half sine mode can make use of only one good external sine clock for the most important music frequency family and the local XO for the rest. To do so, you will need the following steps:

A. Disassemble R2 on the top side of SinePi PCB by a soldering iron.
B. Install a local XO into XO1 socket on the SinePi. The local XO doesn't need an OE control pin if you use FifoPi Q3 or higher. Double check to make sure the local XO orientation is correct.
C. Connect the external sine clock into the XO2 SMA connector J2.

2. How critical is the SinePi power supply?

SinePi sine to square converter board can be considered as a high gain amplifier. In this case, AM noise could be easily modulated into time jitter. So, the power supply will be very critical to the final square wave signal quality. SinePi power supply quality differences were confirmed to be audible.

So far, the top three recommended power supply solutions are:
No.1: UcPure 3.3V with two 3000F ultra capacitors.
No.2: UcConcitioner3.3V with the LifePO4 Mini 3.3V two battery configuration.
No.3: LifePO4 Mini 3.3V in two battery cells parallel configuration.

By default, FifoPi shares the clean side power supply with SinePi. In this case, FifoPi clean side power supply will be the SinePi power supply.

3. **Can I use an independent power supply for SinePi?**

   By default, SinePi takes 3.3V power rail from the XO sockets on a FifoPi. So, normally you don't need an independent power supply for it. It's not recommended but if you really want, you can still do it. It will need the following steps:

   A. Use a side cutter to cut both the PIN4 (Vcc pin) of XO1 and XO2 at the bottom side of the SinePi PCB.

   B. Connect a dedicated 3.3V SinePi power supply to both the GND pad and the 3.3V VCC pad on the bottom side of the SinePi PCB. Please be very careful not to short the circuit.

4. **How long does it take to break-in a SinePi?**

   SinePi is an ultra-low noise application. New capacitors and other components really need time to get more stable and improve after power up. A New SinePi can be used right away without any problem. But for serious listening, I would suggest powering it for more than three days before you get started.

5. **Is a RF relay better than a non-RF relay?**

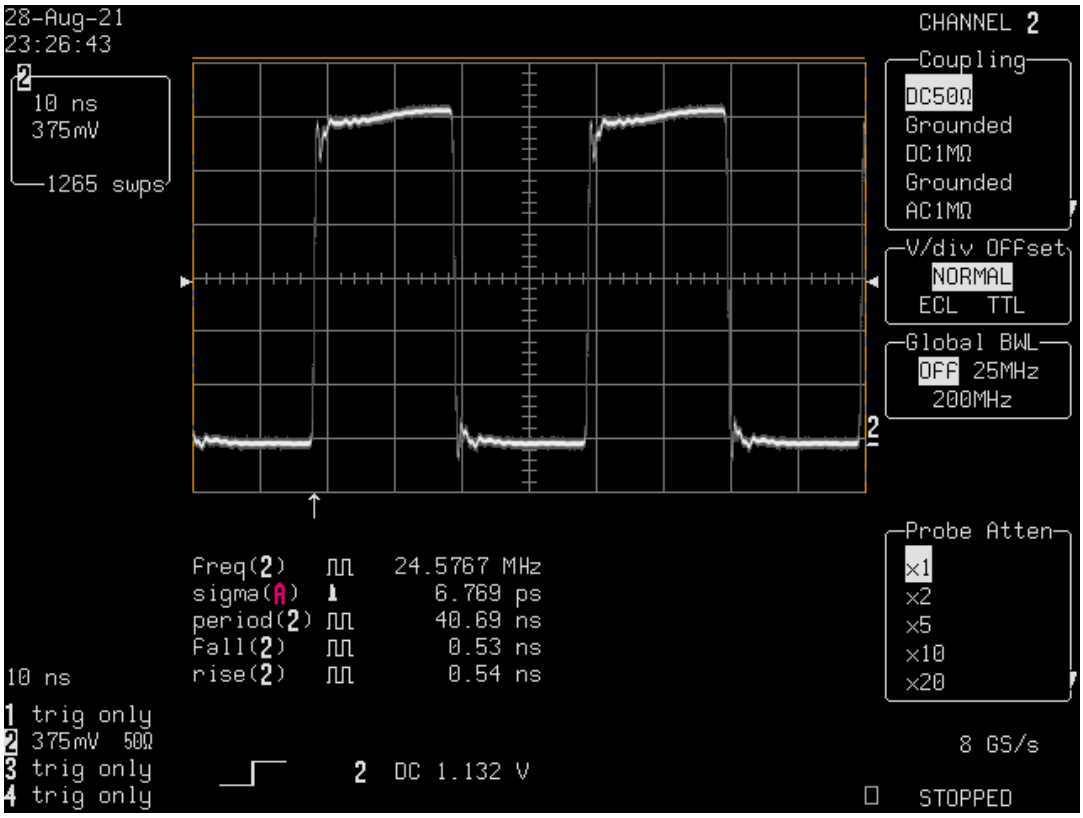
   RF relays are optimized to RF signals, normally they will have better signal isolation, impedance matching and high frequency performance than the non-RF relays. So theoretically, the answer will be yes. However, in the real listening experience, it may not really make as big a difference as we expected. It will be highly up to the actual system. And also, RF relays can be much more expensive than non-RF relays.

   The P/N of the RF relay for SinePi:
   6K-2F-RF-DC3
   or
   G6K-2F-RF-TR03 DC3.

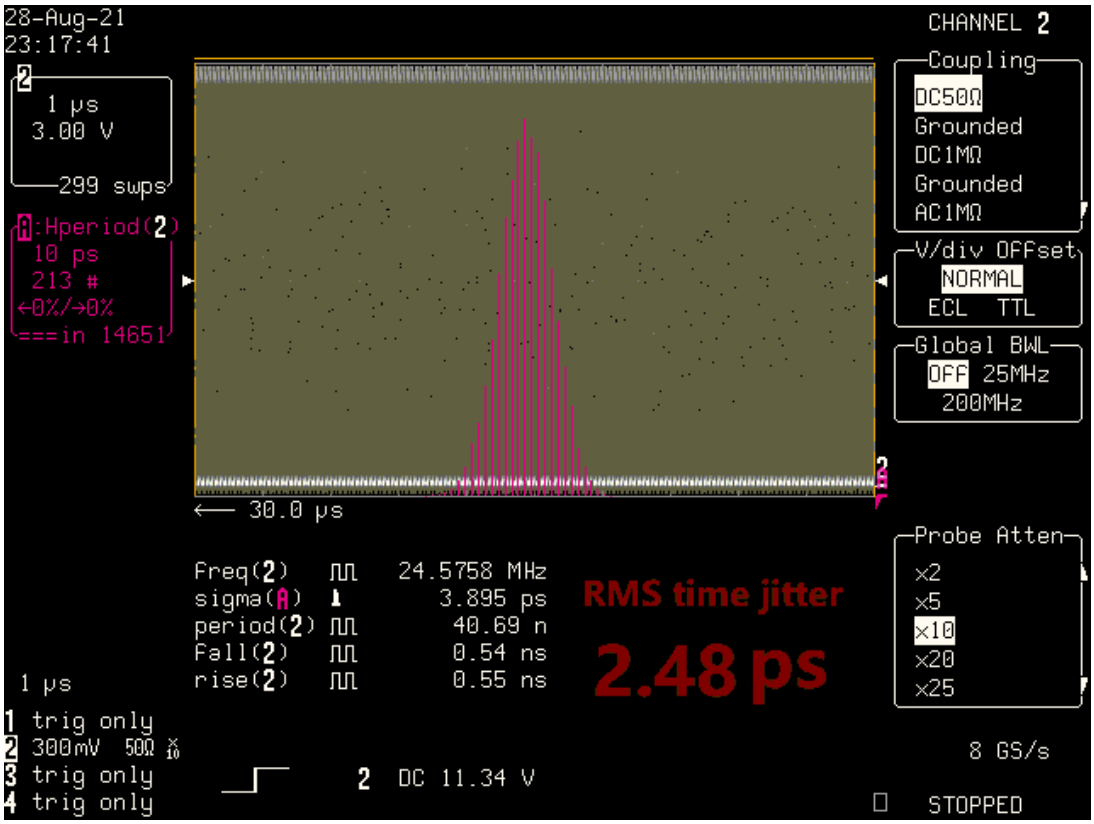
F. Measurement results

Testing conditions:

- LeCroy LC584AXL 1GHz Oscilloscope with jitter measurement package
- Time base 10ns/div
- Run at 8 GS/s sampling with 1GHz bandwidth fully opened
- 4 inches 50 ohm terminated coaxial cable input.
- TWTMC-DRIXO power supply: 13.2V LifePO4
- SinePi power supply: pure 3000F ultracapacitor package precharged to 3.3V
- Sine clock oscillator: TWTMS-DRIXO with 22.5792 MHz SC-CUT crystal
- Dual 80°C oven heating elements were installed
- DUT: SinePi V8.0



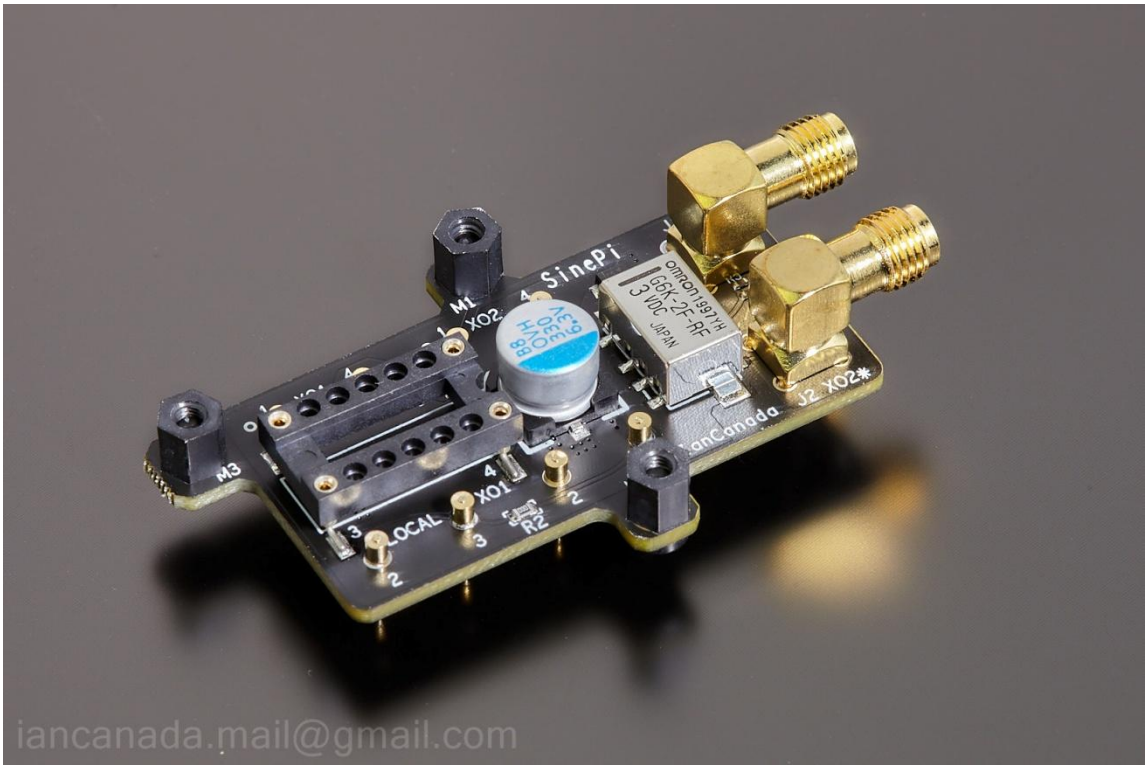
SinePi V8.0 square wave output waveforms



Time jitter of a SinePi V8.0 square wave output (DRIXO SC-CUT 24.5760MHz with oven)

G. Pictures

Fully assembled SinePi V8.0 with a RF relay



H. Links

https://www.diyaudio.com/forums/digital-line-level/192465-asynchronous-i2s-fifo-project-ultimate-weapon-fight-jitter-682.html#post6704886

https://www.diyaudio.com/forums/digital-line-level/192465-asynchronous-i2s-fifo-project-ultimate-weapon-fight-jitter-687.html#post6718041

https://www.diyaudio.com/forums/digital-line-level/192465-asynchronous-i2s-fifo-project-ultimate-weapon-fight-jitter-694.html#post6741950

I. History of revising

Aug. 28, 2021 V0.9b released