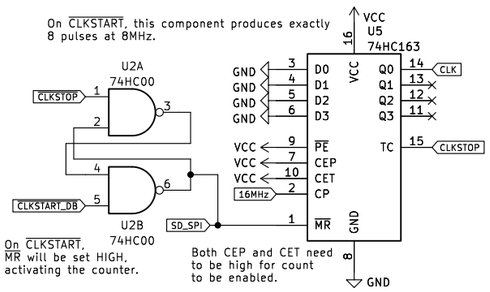
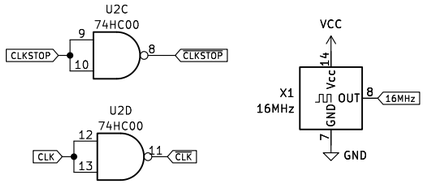
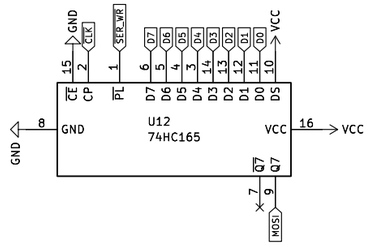
CLOCK COMPONENT

On $\overline{\text{CLKSTART}}$, this component produces exactly 8 pulses at 8MHz.

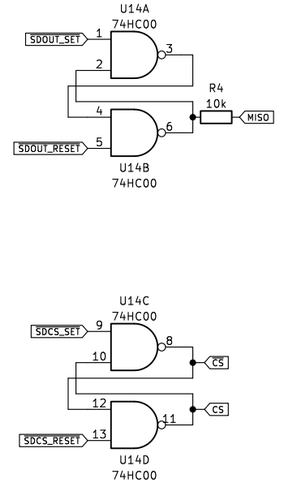




SHIFT REGISTER Z80 –> SD OUT REGISTER



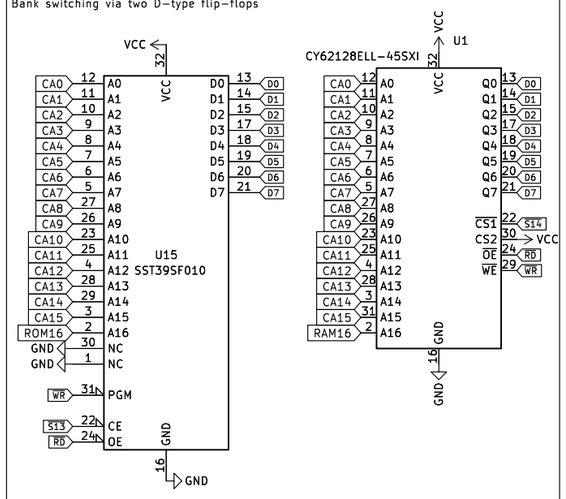
SD CARD S/R LATCHES



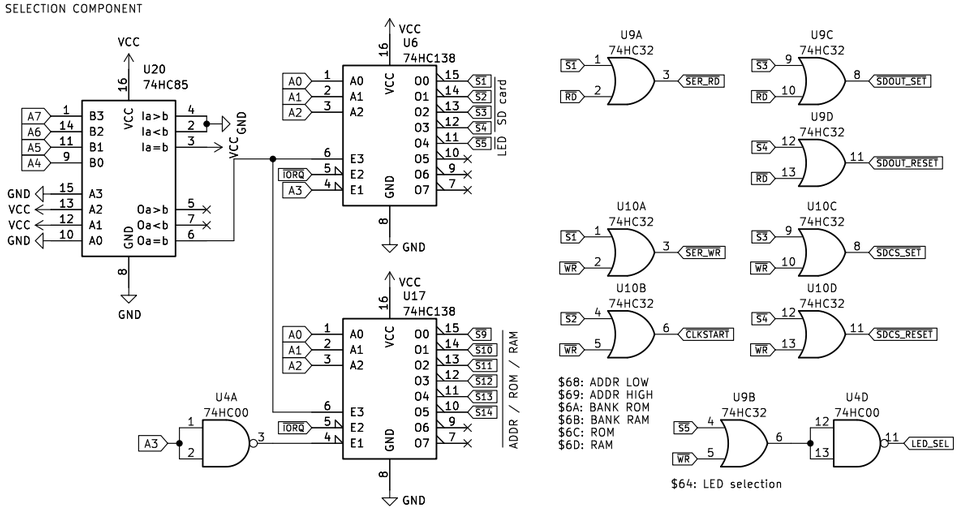
ROM and RAM chips

Expose 2x64kb of memory via bank switching

Addresses are set via two 74HC273 buffers
Bank switching via two D-type flip-flops



SELECTION COMPONENT

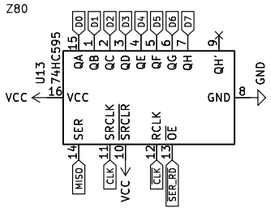


out $60: $\overline{\text{SER\_WR}}$ is pulled low, loading the values on the data bus into the out register.
out $61: $\overline{\text{CLKSTART}}$ is pulled low, starting the counter circuit and pushing a byte into the SD card while simultaneously reading a byte.
out $62: $\overline{\text{SDCS\_SET}}$ is pulled low, pulling $\overline{\text{CS}}$ high, deactivating the SD card.
out $63: $\overline{\text{SDCS\_RESET}}$ is pulled low, pulling $\overline{\text{CS}}$ low, activating the SD card.

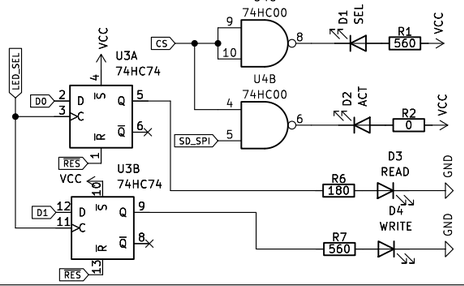
in $60: $\overline{\text{SER\_RD}}$ is pulled low, reading from the in register.
in $61: Does nothing
in $62: $\overline{\text{SDOUT\_SET}}$ is pulled low, pulling MISO low via a 10k resistor.
in $63: $\overline{\text{SDOUT\_RESET}}$ is pulled low, pulling MISO high via a 10k resistor.

When no card is present, the output of the SD card will follow the output of the SET/RESET latch, however if a card is present, though unresponsive, it will not follow and the same (high) output will be received.

SHIFT REGISTER SD –> Z80 IN REGISTER



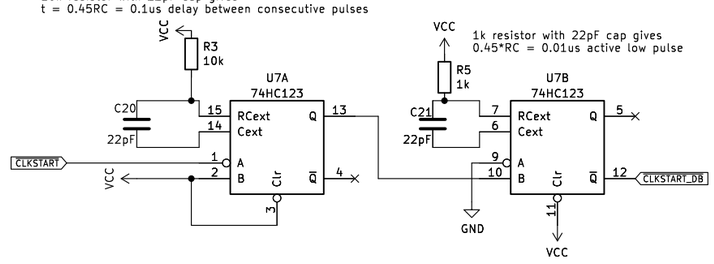
Two LEDS show whether the SD card is selected via the CS line and whether signals are sent to the SD card. Another two leds show I/O on the RAM and ROM chips.



MULTIVIBRATOR DELAY COMPONENT

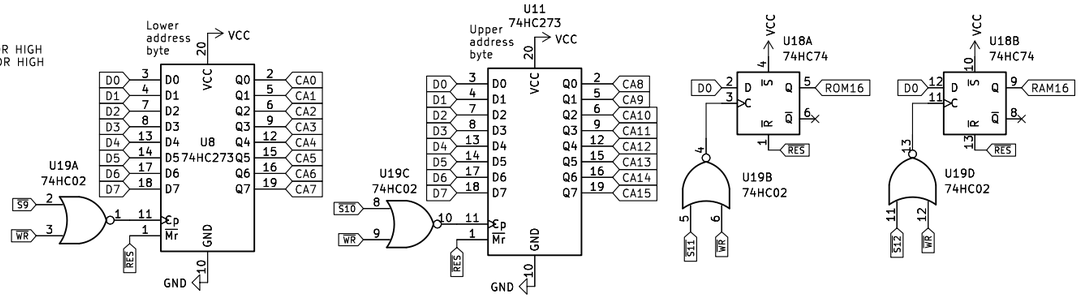
10k resistor with 22pF cap gives
t = 0.45RC = 0.1us delay between consecutive pulses

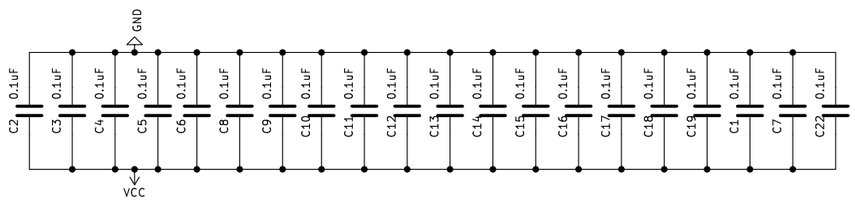
1k resistor with 22pF cap gives
0.45*RC = 0.01us active low pulse

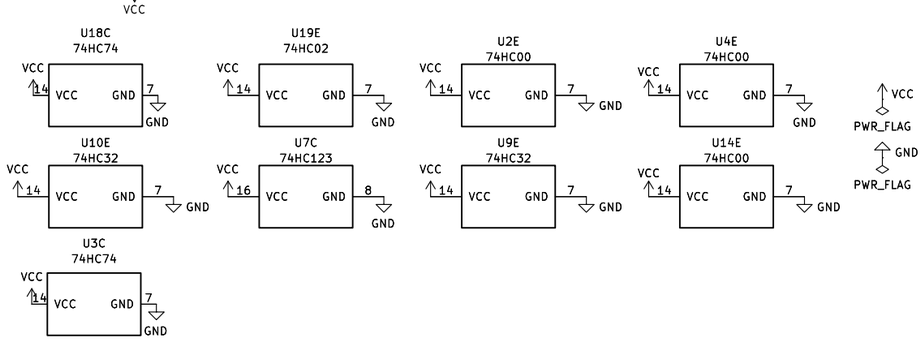


Set 16 bit address for the ROM and RAM chips. The logic circuitry for the CP signal uses the remaining gates on the 74HC04, 74HC00 and 74HC21 chips.

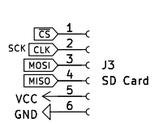
* $\overline{\text{S5}}$ and $\overline{\text{WR}}$ both LOW, CP for lower byte ADDR HIGH
* $\overline{\text{S6}}$ and $\overline{\text{WR}}$ both LOW, CP for upper byte ADDR HIGH



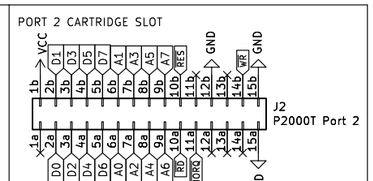




SD CARD



PORT 2 CARTRIDGE SLOT



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Size: A3	Date: 2024-04-09	**Rev: rev4**
KiCad E.D.A. 8.0.2		Id: 1/1