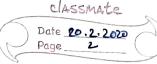
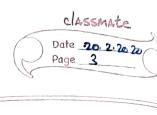
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SYNCHROHIZATION THE BASICS synchronization mechanisms are typically with with ver-level software, but we have got hardware supplied histractions, and part by sound we have low contention situations high contention situations. of the state of the three of in high contention situations, performance may be come a bottleneck, we have a set of basic hardware primitives meghanions mas enothernous metaline - metaline estas atomic exchange. contents of mem loc, and reg. are exchanged without any interruption, - test and set chstructions (PDP-11) betch and increment. - a pair of instructions Cloud result (load locked)) Cotone conditional) -> 0 of 2 inst. exec. atomically Leckit ; branch if lock was not



er try: mov x3, x4 ; move exchange value er neg exi , load result word the planget on homewhat mem addrage, Scor 143,0(x1) of store conditional. bnez x3 try ; branch if storefails. mov x4, x2 lace extension setuctions en try; lr x2, x1 200 load result O(x1) ns, no, 1; increment sc 43 o(a) store conditional bnez x3 try 6 +22 s; branch of store feeds. Only register- regulater chatrochions can reafely ber temic exchange. permitted or the of now loc. and my one exchanged it how an reption. ex addi no Ro #1 lockit: Excel ne, o(n) , atomic exchanges bnez nz, lockit forter construction - a par of instructions lockit; lab 22 6 (24) m load of look bnez lockito .. () mot available - spin , load locked value addi xz Ro, #1 ne, o(21) EXCH swap ; branch if lock was not be lonez nz lockit

Date 20. 2. 2020
Page

en lockit: le 22, o(21); load reserved. (penathness ke dockit som; not available - spin. moment to as adding m2, Ro, #10 on eyolocked gratues to SC X2, O(X1); Store bnez x2, lockit megobranich if netore fails. upolated has appointed and estated and a precessor checo the chia cytes of anther processor what our read most be enforced among read and write to different locations by different propertions write must some exception sequential assesses. most straightforward model for memory considering a rated squential consistency. Clastre lamport). regult of any execution be the same as though memory accesses assecuted by each processor kept in order and excelled among adifferent movestors are relationely interloaved.