FUNDAMENTALS OF QUANTITATIVE DESIGN AND ANALYSIS

- introduction
- classes of computers
- define computer architecture
- trends in technology
- power and energy
- cost
- dependability
- performance
- principles of computer design.

MEMORY HIERARCHY DESIGN

- introduction
- optimization of cache performance
- memory technology and optimization
- protection

INSTRUCTION LEVEL PARALLELISM (ILP) AND ITS EXPLOITATION

- ILP concepts and challenges.
- basic compiler techniques for exploiting ILP.
- reduced branch costs with advanced branch pred.
- overcoming data hazards with dynamic scheduling.
- dynamic scheduling examples & algorithms.
- hardware based speculation.
- multiple issue

- static & dynamic scheduling
- speculation
- multi threading
- exploiting thread level parallelism to improve uniprocessor throughput (core i7 and ARM cortex A8).
- data level parallelism in vector SIMD and GPU architecture.
- vector architecture, SIMD instruction set extensions for multimedia
- GPUs
- detecting and enhancing loop level parallelism.

THREAD LEVEL PARALLELISM

- centralized shared memory architecture.
- performance of shared memory multiprocessors.
- distributed shared memory multiprocessors.
- distributed shared memory & directory-based cache coherence.
- models of memory consistency.

WARE HOUSE SCALE COMPUTERS

- to exploit request-level and data-level parallelism.
- introduction to domain specific architectures.

(1) John L Hennesy, David A Patterson
"Computer Architecture: A quatitative approach".

notes

2. David E Culler, Jaswant Singh with Anoop Gupta.
"Parallel Computer Architecture".
a hardware software approach. - cache coherence prot.
- Morgan Kaufmann. 1998

3. David A Patterson & John L Hennessy
"Computer organization and design the hardware / software interface" V 2014 RISC V.

(M)
PAPPERS

① john & david "a bronze time for digital system"
communications of acm feb 2019.

② jeff dean, david & cliff young
"a new golden age in comp. arch." empowering
the machine learning revolution".
IEEE micro mar./april 208.

③ norman jouppi, cliff, nishant patel & david.
"a domain specific architecture for deep neural
networks" CACM sep 2018.

④ mit.edu MIT news building hardware for the
next generation of AI. nov. 30 2017.

proceeding of IEEE
"efficient processing of deep neural networks".

einstein theory.

(5) 21st century computer architecture a community white paper may 2012.

(6) workshop on advaced computer arch. research. aug. 2010.

(7) " " " " sep. 2010.

PROJECT

- RISC V processor.

assembly language programming RISC V.

design and simulation of a processor.

cache coherance protocols.

the gem 5 simulator (gem5.org).

mulsim multiprocessor simulator.

simics a full system simulation platform.
IEEE computer feb 2002.

2½ & 3D chips ; dark silicon.

quantum computers.

Optical interconnect.

optoelectronic microprocessors with existing tech. and manufacturing. MIT news dec 23, 2015.

non-volatile storage

"non-volatile processor architecture - exploring for energy harvesting applications".
IEEE micro sep-oct 2015.

centip3DE : a 64 core 3D stacked near threshold system

sekhar borkaar and andrew chim, "the future of microprocessors". CACM may 2011.

Knight's landing, 2nd gen. intel xeon (5) φ product
IEEE micro mar/apr 2016.

onlocking ordered parallelism with swarm arch,
IEEE micro may/jun 2016.

"instruction set should be free. the case for RISC-V" Krste Asanovic & david.

technical report UCB/EECS-2014-2016
aug 6, 2014.

RISC-V simulator called venus is available.
@. kvalis.me/venus/

the instructions to use the simulator are at the link: www-inst.eecs.berkely.edu/~cs61c/fa17/labs/3/.

classmate
Date 4.1.2020
Page 6

COMPUTER TECHNOLOGY

① ieee spectrum 83 january issuee
japanese peopl.

moore's law dennard scaling. N / 1.2V.

comp tech. improvement & advances in tech. need to build comp. and from innov. in comp. design.

stored prog. concept. - von neumann.
electromech. calc. - needed human intervention.

technological improvements historically have been fairly steady. and progress arising from better comp. arch. has been less consistent.

kaulan, jsp singh, anoop gupta,
parallel computing.