

# GDDR5 SDRAM

**GDDR5 SDRAM**, an abbreviation for **Graphics Double Data Rate 5 Synchronous Dynamic Random-Access Memory**, is a modern type of synchronous graphics random-access memory (SGRAM) with a high bandwidth ("double data rate") interface designed for use in graphics cards, game consoles, and high-performance computing.<sup>[1]</sup> It is a type of GDDR SDRAM (graphics DDR SDRAM).

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## Overview

Like its predecessor, GDDR4, GDDR5 is based on DDR3 SDRAM memory, which has double the data lines compared to DDR2 SDRAM. GDDR5 also uses 8-bit wide prefetch buffers similar to GDDR4 and DDR3 SDRAM.

GDDR5 SGRAM conforms to the standards which were set out in the GDDR5 specification by the JEDEC. SGRAM is single-ported. However, it can open two memory pages at once, which simulates the dual-port nature of other VRAM technologies. It uses an 8N-prefetch architecture and DDR interface to achieve high performance operation and can be configured to operate in ×32 mode or ×16 (clamshell) mode which is detected during device initialization. The GDDR5 interface transfers two 32-bit wide data words per write clock (WCK) cycle to/from the I/O pins. Corresponding to the 8N-prefetch, a single write or read access consists of a 256-bit wide two CK clock cycle data transfer at the internal memory core and eight corresponding 32-bit wide one-half WCK clock cycle data transfers at the I/O pins.

GDDR5 operates with two different clock types. A differential command clock (CK) as a reference for address and command inputs, and a forwarded differential write clock (WCK) as a reference for data reads and writes, that runs at twice the CK frequency. Being more precise, the GDDR5 SGRAM uses a total of three clocks: two write clocks associated with two bytes (WCK01 and WCK23) and a single command clock (CK). Taking a GDDR5 with 5 Gbit/s data rate per pin as an example, the CK runs with 1.25 GHz and both WCK clocks at 2.5 GHz. The CK and WCKs are phase aligned during the initialization and training sequence. This alignment allows read and write access with minimum latency.

A single 32-bit GDDR5 chip has about 67 signal pins and the rest are power and grounds in the 170 BGA package.

## Commercialization of GDDR5

GDDR5 was revealed by [Samsung Electronics](#) in July 2007. They announced that they would mass-produce GDDR5 starting in January 2008.<sup>[2]</sup>

[Hynix Semiconductor](#) introduced the industry's first 60 nm class "1 Gb" ( $1024^3$  bit) GDDR5 memory in 2007.<sup>[3]</sup> It supported a bandwidth of 20 GB/s on a 32-bit bus, which enables memory configurations of 1 GB at 160 GB/s with only 8 circuits on a 256-bit bus. The following year, in 2008, Hynix bested this technology with its 50 nm class "1 Gb" GDDR5 memory.

In November 2007, [Qimonda](#), a spin-off of [Infineon](#), demonstrated and sampled GDDR5,<sup>[4]</sup> and released a paper about the technologies behind GDDR5.<sup>[5]</sup> As of May 10, 2008, Qimonda announced volume production of 512 Mb GDDR5 components rated at 3.6 Gbit/s (900 MHz), 4.0 Gbit/s (1 GHz), and 4.5 Gbit/s (1.125 GHz).<sup>[6]</sup>

On November 20, 2009, [Elpida Memory](#) announced the opening of the company's Munich Design Center, responsible for Graphics DRAM (GDDR) design and engineering. Elpida received GDDR design assets from [Qimonda AG](#) in August 2009 after Qimonda's bankruptcy. The design center has approximately 50 employees and is equipped with high-speed memory testing equipment for use in the design, development and evaluation of Graphics memory.<sup>[7][8]</sup> On July 31, 2013, Elpida became a fully owned subsidiary of [Micron Technology](#) and based on current public [LinkedIn](#) professional profiles, Micron continues to operate the Graphics Design Center in Munich.<sup>[9][10]</sup>

Hynix 40 nm class "2 Gb" ( $2 \times 1024^3$  bit) GDDR5 was released in 2010. It operates at 7 GHz effective clock-speed and processes up to 28 GB/s.<sup>[11][12]</sup> "2 Gb" GDDR5 memory chips will enable graphics cards with 2 GB or more of onboard memory with 224 GB/s or higher peak bandwidth. On June 25, 2008, [AMD](#) became the first company to ship products using GDDR5 memory with its [Radeon HD 4870](#) video card series, incorporating Qimonda's 512 Mb memory modules at 3.6 Gbit/s bandwidth.<sup>[13][14]</sup>

In June 2010, [Elpida Memory](#) announced the company's 2 Gb GDDR5 memory solution, which was developed at the company's Munich Design Center. The new chip can work at up to 7 GHz effective clock-speed and will be used in graphics cards and other high bandwidth memory applications.<sup>[15]</sup>

"4 Gb" ( $4 \times 1024^3$  bit) GDDR5 components became available in the third quarter of 2013. Initially released by [Hynix](#), [Micron Technology](#) quickly followed up with their implementation releasing in 2014. On February 20, 2013, it was announced that the [PlayStation 4](#) will use sixteen 4 Gb GDDR5 memory chips for a total of 8 GB of GDDR5 @ 176 Gbit/s (CK 1.375 GHz and WCK 2.75 GHz) as combined system and graphics RAM for use with its AMD-powered system on a chip comprising 8 Jaguar cores, 1152 GCN shader processors and [AMD TrueAudio](#).<sup>[16]</sup> Product teardowns later confirmed the implementation of 4 Gb based GDDR5 memory in the [PlayStation 4](#).<sup>[17][18]</sup>

In February 2014, as a result of its acquisition of Elpida, [Micron Technology](#) added 2 Gb and 4 Gb GDDR5 products into the company's portfolio of graphics memory solutions.<sup>[19]</sup>

As of January 15, 2015, [Samsung](#) announced in a press release that it had begun mass production of "8 Gb" ( $8 \times 1024^3$  bits) GDDR5 memory chips based on a 20 nm fabrication process. To meet the demand of higher resolution displays (such as 4K) becoming more mainstream, higher density chips are required in order to facilitate larger frame buffers for graphically intensive computation, namely PC gaming and other 3D rendering. Increased bandwidth of the new high-density modules equates to 8 Gbit/s per pin  $\times$  170 pins on the BGA package  $\times$  32-bits per I/O cycle, or 256 Gbit/s effective bandwidth per chip.<sup>[20]</sup>

## GDDR5X

On January 6, 2015, [Micron Technology](#) President Mark Adams announced the successful sampling of 8 Gb GDDR5 on the company's fiscal Q1-2015 earnings call.<sup>[21][22]</sup> The company then announced, on January 25, 2015, that it had begun commercial shipments of GDDR5 using a 20 nm process technology.<sup>[23][24][25]</sup> The

formal announcement of Micron's 8 Gb GDDR5 appeared in the form of a [blog post](http://www.micron.com/about/blogs/2015/august/next-gen-graphics-products-get-extreme-speed-from-latest-graphics-memory-solutions) (<http://www.micron.com/about/blogs/2015/august/next-gen-graphics-products-get-extreme-speed-from-latest-graphics-memory-solutions>) by Kristopher Kido on the company's website September 1, 2015.<sup>[26][27]</sup>

In January 2016, JEDEC standardized GDDR5X SGRAM.<sup>[28]</sup> GDDR5X targets a transfer rate of 10 to 14 Gbit/s per pin, twice that of GDDR5.<sup>[29]</sup> Essentially, it provides the memory controller the option to use either a double data rate mode that has a prefetch of 8n, or a quad data rate mode that has a prefetch of 16n.<sup>[30]</sup> GDDR5 only has a double data rate mode that has an 8n prefetch.<sup>[31]</sup> GDDR5X also uses 190 pins per chip (190 BGA).<sup>[30]</sup> By comparison, standard GDDR5 has 170 pins per chip; (170 BGA).<sup>[31]</sup> It therefore requires a modified PCB.

## GDDR5X commercialization

Micron Technology began sampling GDDR5X chips in March 2016,<sup>[32]</sup> and began mass production in May 2016.<sup>[33]</sup>

Nvidia officially announced the first graphics card using GDDR5X, the Pascal-based GeForce GTX 1080 on May 6, 2016.<sup>[34]</sup> Later, the second graphics card to use GDDR5X, the Nvidia Titan X on July 21, 2016,<sup>[35]</sup> the GeForce GTX 1080 Ti on February 28, 2017,<sup>[36]</sup> and Nvidia Titan Xp on April 6, 2017.<sup>[37]</sup>

## See also

- [List of device bit rates](#)

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## External links

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- Introduction To GDDR5 SGRAM(by ELPIDA) (<https://web.archive.org/web/20110720090920/http://www.elpida.com/pdfs/E1600E10.pdf>)
  - Making Accurate Measurements on GDDR5 Memory Systems (<https://web.archive.org/web/20110707094741/http://cp.literature.agilent.com/litweb/pdf/5990-6130EN.pdf>)
  - GDDR5 Pinout and Description (<http://www.interfacebus.com/GDDR5-Memory-IC-Pinout.html>)
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