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EXPLOITING ILP USING MULTIPLE ISSUE PROCESSORS AND STATIC SCHEDULING

the idea is to achieve an ideal CPI . CPI < 1 possible if we issue more than 1 instructions. we want to decrease CPI to less than 1. there are 3 major flavours of the multiple issue processors.

by compiler

(a) statically scheduled superscalar processors.

(b) VLIW very long instruction word, processors → fixed no. of inst by compiler.

(c) dynamically scheduled superscalar processors.

→ executed out of order

issue variable no. of instructions.

two types of superscalar processors issue varying no. of instructions. if they are statically scheduled, they will carry out in-order execution; if they are dynamically scheduled, we will have out-of-order execution.

VLIW processors issue a fixed no. of instructions, they are formatted as - a long instruction - or fixed instruction pattern. VLIW processors are inherently statically scheduled by the compiler.

intel, HP came up with itanium architecture. EPIC. appendix H. the basic VLIW approach will have (they use multiple independent functional units

exploiting ILP using dynamic scheduling. multiple issue

and speculation.

ADVANCED TECHNIQUES WITH INSTRUCTION DELIVERY AND SPECULATION.

able to deliver a high bandwidth instruction stream. recent multiple issue processors would be delivering 4-8 instructions per clock cycle. this demands increasing the instruction delivery bandwidth.

value prediction could further enhance ILP. most difficult aspect is handling branches. so we can have branch target buffers, when can have buffer with return addresses

we have return address predictors. which is a small buffer operating on a stack.

INTEGRATED INSTRUCTION FETCH UNIT

1. integrated branch prediction
2. instruction prefetch unit.
3. instruction memory. ace
4. register renaming vs. reorder buffer.

REGISTER RENAMING VS REORDER BUFFER.

library
morali

speculation may increase power consumption but total power consumed may be less.

Studies of limitations of ILP.

hw model. ideal perfect processors.

limitations of ILP on realizable processor.

64 instructions per clock.

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