CLASSES OF PARALLELISM

AND PARALLEL ARCHITECTURE,

LLP DLP TLD RLP

bor computer design.

* IT dota level parallelism

* task level parallelism

Speec lative execution

same time.

2 kinds of parallelism in applications,

many data items can be operated boom at the

tasks of work are created. that can operate

computer hardware exploses these 2 parallelism

instruction level parallelism exploits PLP at modest levely

Or kinds of applications in a major ways)

anth compiler help using like pipelining and

2. data level parallely in is exploited by vector

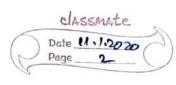
processess. and multimedia instruction sets

explain data kevel parallelism by applying a

single instruction to a collection of data in parallel

independently and lungely in parallel

parallelism of multiple levels is driving force



3. thread level parallelism exploits either data level
garallelism of task level parallelism in a timely
tightly coupled hardware module, that allows
for interaction between parallel threads.

4. reguest level parallelism exploits parallelism among

largely decoupled tasks, specified by the programmer or operating system.

sisd simd misd mind.

C. single instruction stream. (uniprocessor.

blynn (eace) booker at parallelism in instruction and data streams.

we can also exploit instruction level paralletism.

gov could also have speculative execution,

2. Single instruction stream Multiple data stream

this can exploit data level parallelism.

3. multiple instruction stream, but single data stream

there is no commercial system of this model.
4. multiple instruction stream.

multiple data tream.

more blexible than simd but inherently more.

expensive than simd.

toghtly coopled mind architectures exploit (there may be need for interaction, communication), threats lovel parallelism and loosely coopled mind and tecture are

anchitecture & ISA

+ organization of system (entrie anch.)

t handwere rerealization,

elusters and warehouse Scale a computers.

defining computer architecture

the compoter designer asil determine what attributed, are imparted tant for a new compoter to maximize performance and energy use refficiency, at the same time cost should not be too high.

while staying within cost, power, and availability constraints.



jour issue of i'eee spectrum.

this task has many aspects.

· instruction set design,

· functional organization,

· logue design

· implementation-

the implementation may encompass 10 design, packaging, power and oboling,

ibm300 systems had cool water cooling.

aprilmizing design require familiarity with a wide range

from compress, and OS to logic design

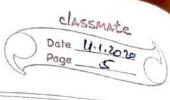
a few decades ago, computer architecture were refletted to is instruction set alsoign,

and - (regs) = implementation.

BA serves as a boundary between the & software & hardware.

ARM ~ In billion chips sola

a so times 186 processors.



RISC processors are refferred to as load and store archivedon

I dasses of ISA

hearly all ISAs are classified as general purpose register architectures, operands are either in gregister or memory locations.

8086 had 161 general purpose registers, and they can ale held le floating point data.

RISEV was 32 general purpose register and 32 floating point registers.

register memory isa.

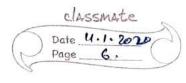
2 memory addressing.

1955 onwards all ssag are load - store

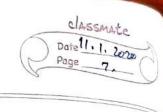
these days we have byte addressing,

ARMV8-aligned RISCV any byte / do not require 286 alignment.

& addressing mods. (imm reg.)



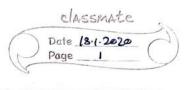
4. types & sizes of operands. 8-bit operands asci' (8-bit code anicode (1/2 word) 22-bit integer on word 64-bit double word on long integer. IFFE -754 bloating point system 32 bit single precision by but double precision So but extended double precesion. 5. Operations data trasfer operation. avithmetic logical. floating point operations a control flow instructions Conditional branches. enconderconal branches, (jumps) procedure call return.



7. encoding of ISA.

fixed length -> complementation is much simplen and variable length. -> size of code could be compact.

architecture - 18th, organization, tardware



computer architects design computer to mech functional requirements and in addition must not be too costly, power, performance, avalaitiff.

end use architects also aware of technology development & use of cmp [computers wers

producers TRENDS IN TECHNOLOGY

become

ISA survival depends on technological development, as

there are technological development, ISA may change. it may be affected by rapid changes in technology.

earlier we had instructions of variable length. Since 1985 RISC arch were introduced, size of instructions remains same.

117 madras, TATAS 2000 arch. The arch of that processor remain same for 50 years. The iBM mainframe survived nearly so years and the designers must be aware of the technological developments, rapid changes

there are 5 implementation technologies, and as pen the book, they change at a dramatic pace they are very critical for ic legic technology.

in implementation technology.

moords low - dennard scaling (2004) often 30 years,

classmate Date 18. 2.2020 explore user more transiston density has been increasing about 357. /yan and die size is less predictable and growth has been clover at 10-20x, /year. = semiconductor DRAM SDRAM 80-B DRAM was shipped in 2014. IS GB RAM may have been introduced in 2019. 32 CrB RAM may not come, * semiconductor blash (EEPROM) used in personal mobiled devices = magnetic olisk technology 2600 rpm -> 15000 rpm, size come docon to 300, could be 2 platters, one company awarking on heat assisted magnetic recovery don't have get commercial technology = network technology 10 Mbits -> 10 Cobits/s. cohon ethernet introduced PERFORMANCE TRENDS 1 bandwidth 1 throughput @ parformance latency.

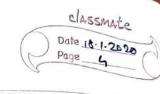
= scaling of transistor performance. prof. arant agaroval Toler a company 69 core step processors - or nm chips underway. TRENDS IN POWER AND ENERGY IN ICS. energy is the biggest challenge, if power is supplied a continuous amount of time, and power must be brought from the source power must be brought in and distributed around the chips, moders processors have hundreds of pings. &. mutiple interconnect layers ones power as heat. then you took a't power and energy, we have we have to worry about performance. 3 primary concerns = maximum power ever required + sustained power thermal design power CTDP)

max power & 1.5 x TDP

which takes care of cooling also

many cores not used, some processors.

many not used all the time - dark sillicon (comp).



dynamic energy imp. supply voltage some down or current comed down, difference between on and off current also has come down,

TRENDS IN COST

fobrication is better understood ever a period of time. therefore field can be improved, impact of time, volume, and commoditize from.

= can bey parts and do it

may not be good. what muses faulty processes understanding.

learning curve commicanduction are taken with

cost of an IC is given by the cost of die + ?

cost of tosting diet

fabricating +

Cost of packing +

final test

final test yield (a gox).



cost of die = cost of water dies per water X die yield dies/water = 1 x (water dia 12)2 die area - x wager dia V 2x die area die gield = water gield » [1 + deck / areax diearea for 28nm defuces in 2017 = 7.5-9.5 lenm cost of manufacturing depends upon CAPEX, CPEX dependability earlier prins were vulnerable, and fault may accor over comm, channels, and this cons referred to as conventional wisdom, it changed when devices became very small. there could be transient boolts in devices or permanent foolts. and to overcome these boults, we have service level agreements and service level boults. mean time between failures = mean time to failure +

mean time to repaire

MEASURING, REPORTING, AND SUMMARIZING PERFORM

performance depends upon the response time. we have the execution time and through put, and also depends upon workload.

then we have benchmarks. early days kernels used, toy programs, synthetic benchmarks; ede systems in the 70s. @ kanpur main brame systems. time.

Shoring system. 117 mumbai, kgp russian systems.

subsequently we have dinystone benchmank suite, all have another EEMBC electronic design new embedded microprocesson benchmank consortium.

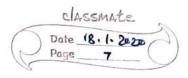
programs are in the area of automating industries consumer networking office automation and tele comm,

performance depends upon clock cycle time, and how many cycles per instruction, time it takes depends on no. of instructions.

SPEC system performance evaluation corporation.

benchmarks 1989 1992 1995 2000 2006 2007,

talk about how many instructions per clock.



OUANTITATIVE	PRINCIPLES OF	COMPUTER	DECIGA
			0 5 011

take advantage of parallelism - some scientific applications already - you have to write multicore programs, take advantage of parallelism,

PRINCIPLE OF LOCALITY

temporal locality

recent chetruction may be executed again, like the
bor loop:

spatial locality

applications will have 10-15x.