INSTRUCTION LEVEL PARALLELISM

i way - instruction pipelining

multiple instructions are overlapped in execution

each stage in the pipeline is referred to a pipe stage or pipe segment.

each stage must be able to complete i'ts operation in a clock cycle, try to balance the time taken by each stage.

the length of a processor cycle is determined by the slowest stage. so pipeline designer's goal is to

balance the length of each pipeline stage time / instruction

time for exec, in unpipelined stage no. of pipeline stages.

cons like CS 252 2011 & 2012 PPTS. ACM 47 (october 10) 71-23 2004 organt,

latency lags bandwidth,



(CPI (oxcles per cing.) for a pipelined processor,

is given by the base CPI

CPI = Sum of base CPI and all contributions from stalls.

pipeline (PI = cideal pipeline (PI + Structural Stalls + data hazard Stalls + control Stalls.

Cwrite after redd...) (Granch)

THE BASICS OF THE RISCV INSTRUCTION SET

its concerned with load and store operation. Commission of all operations on data apply to data in register, the only operations that affect memory are the load & store operations.

a construction fetch cycle. (1)

(2) Enstruction decode and register fetch (10)

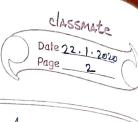
6 memory access. (MEM)

Swrite back cycle (WB).

Sove instruction 4 cycles

other instructions 5 cycles

Dipelining increases the (throughput) of processor construction.



each instruction. major hundle of pipelining - pipeline hazards.

O structural hazards.

they arise from resource conflicts, when the hardware may not support all possible Combinations of instructions simultaneously, in overlapped execution.

achen an instruction depends on the result of a previous instruction in a way that is exposed by the averlapping instruction in the pipeline.

(a) control hazards.

may arise from the pipeline of branch and other instruction

that change the PC.

(lady namic (Static)

by compiler

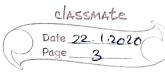
-loop unvolving

2 normally seperative approaches to explaite ILP.

- reordering instructions.

e- an approach that relies on offware technology to fill

partletism statically at compiletime,



we have to exploit IPL across multiple blocks. dynamic schedoling - hw will change order of exec, while maintaining Correctness of the program. imprecise exceptions must be avoided dynamic scheduling example. Adivod. fo, fz, fr food fie for funce can be executed in advance. to check for these borrards, the iD phage. we must separate the issue process into two points, Thecking for any structural hazards and wating for the obsence of data hazand. fdiv.d fo, 62, 64 Amd.d 66, 70, 68 foolded to for fing register renaming 152 study from book for pipelining. Fronds prediction appendix l in on 15th Edition -glord dormat TIP thread level paralellism. - water.