

	FUNDAMENTALS OF QUANTITATIVE DESIGN
	AND ANALYSIS
	rointendent
	entro duction
-	classes of computers
1	define computer architecture
-	trends in technology
	power and energy.
	cost
	dependability
	performance
-	principles of computer design.
	energy proportion to the same
-	
	MEMORY HIERARCHY DESIGN
	introduction 1021 11 11 11 11 11 11 11 11 11 11 11 11 1
	optimization of cache performance.
- 1	- memory technology, band optimization
	- protection
	INSTRUCTION LEVEL PARLELLISM (ILP)
	AND ITS EXPLOITATION
	- ILP concepts and challenges
	- basic compiler techniques for exploiting rip.
	- reduced branch costs with advanced branch pred.
	overcoming data hazards with dynamic scheduling
	dynamic scheduling examples & algorithms.
1	

- hardware based speculation.

- multiple issue



-static & dynamic scheduling -speculation - multi threading - exploiting thread level parallelism to wimprove uniprocessor throughput (core it and ARM Cortex A8) -data level parallelism in vector SIMD and GPU architecture - vector architecture, SIMD instruction cet extensions for multimedia - GPUS - detecting and enhancing loop level parallelism THREAD LEVEL PARALLELISM cont-centralized shared memory architecture. - performance of shared memory multiprocessors - distributed shared memory multiprocessors, - distributed shared memory & directory-based suche - models of memory consistency. WAR WARE HOUSE SCALE COMPUTERS · to exploit request-level and data-level parallelism. introduction to domain specific architectures.

Computer Architecture: A quatitative approach

mores.

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2. David F Giller, Jaswant Singh with Apoop Erupta.

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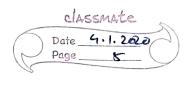
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6	workshop on advaced computer aug. 2010.	arch. yesearch.
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- - -	PROJECT  RISG V processor.  assembly language programming	RISC V.
Sec. 1	design and smulation of a process  ache coherance protocols.	
	the gem 5 amulaton Gems.or	
	mulsim multiprocessor simulat	
	Simics a foll System amolation.  IEEE computer feb 2002	
	2 1/2 & 3D Chips dark sillicon quantum competers.	7
	optical interconnet optoelectronic microprocessors with and manufacturing. MIT news dec	existing tech.



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Centip SDE . a 64 core 30 stacked near threshold

Knight's landing, 2nd gen. ontel xeon' of product

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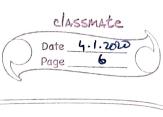
onlocking ordered parallelism with swarm arch,

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Rise v simulator called venus is available. @ Kvakil. me / venus/

the instructions to use the simulator are at the link: www-inst: eecs. berkely.odu/ncs61c /fv 17/labs/3/.



COMPUTER TECHNOLOGY

1 rece spectrum 83 january 185000 japanese people

moore's how dennard scaling. IN 11.2V.

comp tech, improvement & advances un tech. used to build comp and from innove in comp design,

Stored prog. concept. - von neumann electromech. calc. Eneeded human intervention

technological improvements historically have been fairly steady. and progress arising from

better comp. arch. has been less consistent.

koulan, Jepsingh, anoop gupta,

parallel computings