

## MULTIPLE LANES

on a combination II and pipelined units.

by adding more lanes

designers to trade off area, Clock rate, voltage

and energy without suscripicing performance

max. vector length (32) Cmve)

VECTOR LENGTH REGISTERS

vector length register (ve)

to add a vector length reguster (VL)

for (1=0, c/n; i= c+1)

the VL controls the length of any vector operation including vector load and store.

when the vector is lenger than the max. length,

vector operation is done for a size <= MUL

a technique called strip mining is used.



# enable 2 64-bit FP vector

PREDICATE REGISTERS

for (1=0; 1264; 1=1+1)

if (x[1] != 0)

x[1] = X[1] - Y[1]

vseltdofg 2+FP64

tt registers

vsetpcfgi | # enable | predicate register

vld vo, \$≥ x5 # load vector x into vo

vld vi x6 # load vector y into vi

6mv.d.x 60, x0 # put FP zero into 60

vpne po, vo, bo # Set Po (i) to 1 if vo (i) \$0

vsb vo, vo, vI # subtract under vector.

Vst vo, x5 # store the result in x

Volisable # disable voctor registers.

Volisable # alisable predicate registers.

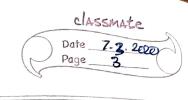
MEMORY BANKS (Gorage) (holding area).

supplying bandwidth for vector load/stone units.

most vector processor use memory bank which allow several independent accesses, rather than memory

interleaving proving following reasons.

per dock cycle and the memory bank cycle time is usually several times larger than the processor cycle.



most rector processor support the ability to load on Store data coords that are not sequential.

3 most vector pro computers support moltiple processons sharing the same memory system, so each processon

will be generating its own separate stream of addresses.

STRIDE

for (c=0; c< 100; c++) for (1'=0; j(100; j++) ACIJ OCI I S

for ( K =0; K < 100; K++ )

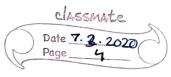
ACITE O \* DECTOR + COLITA + COLITA

the distance separating elements to be gathered into a single vector register is called the stricte.

GATHER AND SCATTER

for ( i=o, ikn, it+) ALKEIT = ALKEIT + CEMEIT

ender vectors X5 X6 X7



			Page 4
	vsetdefg	4 * FP64	# 4 64 bit vector registers
	vld	Vo, x7	# load K[]
	vodn	V1, X5, V0	# load A[K[]]
منر	vld	V2, ×28	# load MI]
100	vldi	V3, X6, V2	# load c[M[]]
_	vadd	V1, V1, V3	# add them
	VStx	VI , X5, Vo	# Store A [K[]]
	Vdisable	13.14.1	# disable vector registers.
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