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# DDR4 SDRAM

**Double Data Rate 4 Synchronous Dynamic Random-Access Memory**, officially abbreviated as **DDR4 SDRAM**, is a type of synchronous dynamic random-access memory with a high bandwidth ("double data rate") interface.

Released to the market in 2014,[1][2][3] it is a variant of dynamic random-access memory (DRAM), of which some have been in use since the early 1970s,[4] and a higher-speed successor to the DDR2 and DDR3 technologies.

DDR4 is not compatible with any earlier type of random-access memory (RAM) due to different signaling voltage and physical interface, besides other factors.

DDR4 SDRAM was released to the public market in Q2 2014, focusing on ECC memory,[5] while the non-ECC DDR4 modules became available in Q3 2014, accompanying the launch of Haswell-E processors that require DDR4 memory.[6]

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**DDR4 SDRAM**
**Double Data Rate 4 Synchronous Dynamic Random-Access Memory**

| Type of RAM | |
|---|---|
|  8 GiB DDR4-2133 ECC 1.2 V RDIMM | |
| **Developer** | JEDEC |
| **Type** | Synchronous dynamic random-access memory (SDRAM) |
| **Generation** | 4th generation |
| **Release date** | 2014 |
| **Standards** | DDR4-1600 (PC4-12800)<br>DDR4-1866 (PC4-14900)<br>DDR4-2133 (PC4-17000)<br>DDR4-2400 (PC4-19200)<br>DDR4-2666 (PC4-21333)<br>DDR4-2933 (PC4-23466)<br>DDR4-3200 (PC4-25600) |
| **Clock rate** | 800–1600 MHz |
| **Voltage** | Reference 1.2 V |
| **Predecessor** | DDR3 SDRAM (2007) |
| **Successor** | DDR5 SDRAM (2020) |

## Features

The primary advantages of DDR4 over its predecessor, DDR3, include higher module density and lower voltage requirements, coupled with higher data rate transfer speeds. The DDR4 standard allows for DIMMs of up to 64 GiB in capacity, compared to DDR3's maximum of 16 GiB per DIMM.[7]

Unlike previous generations of DDR memory, prefetch has *not* been increased above the 8n used in DDR3;[8]:16 the basic burst size is eight words, and higher bandwidths are achieved by sending more read/write commands per second. To allow this, the standard divides the DRAM banks into two or four selectable bank groups,[9] where transfers to different bank groups may be done more rapidly.

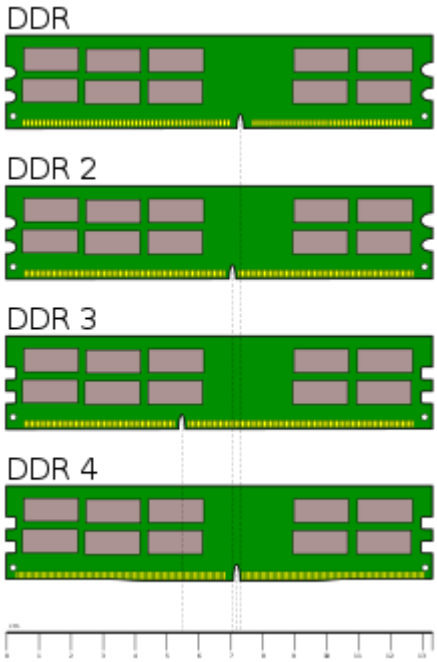
Because power consumption increases with speed, the reduced voltage allows higher speed operation without unreasonable power and cooling requirements.

DDR4 operates at a voltage 1.2 V with a frequency between 800 and 1600 MHz (DDR4-1600 through DDR4-3200), compared to frequencies between 400 and 1067 MHz (DDR3-800 through DDR3-2133)[10][a] and voltage requirements of 1.5 V of DDR3. Due to the nature of DDR, speeds are typically advertised as doubles of these numbers (DDR3-1600 and DDR4-2400 are common, with DDR4-3200, DDR4-4800 and DDR4-5000 available at high cost). Unlike DDR3's 1.35 V low voltage standard DDR3L, there is no DDR4L low voltage version of DDR4.[12][13]

# Timeline

The first DDR4 memory module prototype was manufactured by Samsung and announced in January 2011.[b]

- **2005:** standards body JEDEC began working on a successor to DDR3 around 2005,[15] about 2 years before the launch of DDR3 in 2007.[16][17] The high-level architecture of DDR4 was planned for completion in 2008.[18]
- **2007:** some advance information was published in 2007,[19] and a guest speaker from Qimonda provided further public details in a presentation at the August 2008 San Francisco Intel Developer Forum (IDF).[19][20][21][22] DDR4 was described as involving a 30 nm process at 1.2 volts, with bus frequencies of 2133 MT/s "regular" speed and 3200 MT/s "enthusiast" speed, and reaching market in 2012, before transitioning to 1 volt in 2013.[20][22]
- **2009:** in February, Samsung validated 40 nm DRAM chips, considered a "significant step" towards DDR4 development[23] since in 2009, DRAM chips were only beginning to migrate to a 50 nm process.[24]
- **2010:** subsequently, further details were revealed at MemCon 2010, Tokyo (a computer memory industry event), at which a presentation by a JEDEC director titled "Time to rethink DDR4"[25] with a slide titled "New roadmap: More realistic roadmap is 2015" led some websites to report that the introduction of DDR4 was probably[26] or definitely[27][28] delayed until 2015. However, DDR4 test samples were announced in line with the original schedule in early 2011 at which time manufacturers began to advise that large scale commercial production and release to market was scheduled for 2012.[1]




Physical comparison of DDR, DDR2, DDR3, and DDR4 SDRAM

- **2011:** in January, Samsung announced the completion and release for testing of a 2 GiB DDR4 DRAM module based on a process between 30 and 39 nm.[29] It has a maximum data transfer rate of 2133 MT/s at 1.2 V, uses pseudo open drain technology (adapted from graphics DDR memory[30]) and draws 40% less power than an equivalent DDR3 module.[29][31][32]
  In April, Hynix announced the production of 2 GiB DDR4 modules at 2400 MT/s, also running at 1.2 V on a process between 30 and 39 nm (exact process unspecified),[1] adding that it anticipated commencing high volume production in the second half of 2012.[1] Semiconductor

processes for DDR4 are expected to transition to sub-30 nm at some point between late 2012 and 2014.[33][34]

Front and back of 8 GB DDR4 memory modules

- **2012:** in May, Micron announced[2] it is aiming at starting production in late 2012 of 30 nm modules.
  In July, Samsung announced that it would begin sampling the industry's first 16 GiB registered dual inline memory modules (RDIMMs) using DDR4 SDRAM for enterprise server systems.[35][36]
  In September, JEDEC released the final specification of DDR4.[37]
- **2013:** DDR4 was expected to represent 5% of the DRAM market in 2013,[1] and to reach mass market adoption and 50% market penetration around 2015;[1] as of 2013, however, adoption of DDR4 had been delayed and it was no longer expected to reach a majority of the market until 2016 or later.[38] The transition from DDR3 to DDR4 is thus taking longer than the approximately five years taken for DDR3 to achieve mass market transition over DDR2.[33] In part, this is because changes required to other components would affect all other parts of computer systems, which would need to be updated to work with DDR4.[39]
- **2014:** in April, Hynix announced that it had developed the world's first highest-density 128 GiB module based on 8 Gibit DDR4 using 20 nm technology. The module works at 2133 MHz, with a 64-bit I/O, and processes up to 17 GB of data per second.
- **2016:** in April, Samsung announced that they had begun to mass-produce DRAM on a "10 nm-class" process, by which they mean the 1x nm node regime of 16 nm to 19 nm, which supports a 30% faster data transfer rate of 3,200 megabits per second. Previously, a size of 20 nm was used.[40][41]

### Market perception and adoption

In April 2013, a news writer at International Data Group (IDG) – an American technology research business originally part of IDC – produced an analysis of their perceptions related to DDR4 SDRAM.[42] The conclusions were that the increasing popularity of mobile computing and other devices using slower but low-powered memory, the slowing of growth in the traditional desktop computing sector, and the consolidation of the memory manufacturing marketplace, meant that margins on RAM were tight.

As a result, the desired premium pricing for the new technology was harder to achieve, and capacity had shifted to other sectors. SDRAM manufacturers and chipset creators were, to an extent, "stuck between a rock and a hard place" where "nobody wants to pay a premium for DDR4 products, and manufacturers don't want to make the memory if they are not going to get a premium", according to Mike Howard from iSuppli.[42] A switch in market sentiment toward desktop computing and release of processors having DDR4 support by Intel and AMD could therefore potentially lead to "aggressive" growth.[42]

Intel's 2014 Haswell roadmap, revealed the company's first use of DDR4 SDRAM in Haswell-EP processors.[43]

AMD's Ryzen processors, revealed in 2016 and shipped in 2017, use DDR4 SDRAM.[44]

## Operation

DDR4 chips use a 1.2 V supply[8]:16[45][46] with a 2.5 V auxiliary supply for wordline boost called $V_{PP}$,[8]:16 as compared with the standard 1.5 V of DDR3 chips, with lower voltage variants at 1.35 V appearing in 2013. DDR4 is expected to be introduced at transfer rates of 2133 MT/s,[8]:18 estimated to rise to a potential 4266 MT/s[39] by 2013. The minimum transfer rate of 2133 MT/s was said to be due to progress made in DDR3

speeds which, being likely to reach 2133 MT/s, left little commercial benefit to specifying DDR4 below this speed.[33][39] Techgage interpreted Samsung's January 2011 engineering sample as having CAS latency of 13 clock cycles, described as being comparable to the move from DDR2 to DDR3.[30]

Internal banks are increased to 16 (4 bank select bits), with up to 8 ranks per DIMM.[8]:16

Protocol changes include:[8]:20

- Parity on the command/address bus
- Data bus inversion (like GDDR4)
- CRC on the data bus
- Independent programming of individual DRAMs on a DIMM, to allow better control of on-die termination.

Increased memory density is anticipated, possibly using TSV ("through-silicon via") or other 3D stacking processes.[33][39][47][48] The DDR4 specification will include standardized 3D stacking "from the start" according to JEDEC,[48] with provision for up to 8 stacked dies.[8]:12 X-bit Labs predicted that "as a result DDR4 memory chips with very high density will become relatively inexpensive".[39]

Switched memory banks are also an anticipated option for servers.[33][47]

In 2008 concerns were raised in the book *Wafer Level 3-D ICs Process Technology* that non-scaling analog elements such as charge pumps and voltage regulators, and additional circuitry "have allowed significant increases in bandwidth but they consume much more die area". Examples include CRC error-detection, on-die termination, burst hardware, programmable pipelines, low impedance, and increasing need for sense amps (attributed to a decline in bits per bitline due to low voltage). The authors noted that, as a result, the amount of die used for the memory array itself has declined over time from 70–78% for SDRAM and DDR1, to 47% for DDR2, to 38% for DDR3 and to potentially less than 30% for DDR4.[49]

The specification defined standards for ×4, ×8 and ×16 memory devices with capacities of 2, 4, 8 and 16 Gib.[50]

## Command encoding

Although it still operates in fundamentally the same way, DDR4 makes one major change to the command formats used by previous SDRAM generations. A new command signal, $\overline{\text{ACT}}$, is low to indicate the activate (open row) command.

The activate command requires more address bits than any other (18 row address bits in an 16 Gb part), so the standard $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, and $\overline{\text{WE}}$ active low signals are shared with high-order address bits that are not used when $\overline{\text{ACT}}$ is high. The combination of $\overline{\text{RAS}}$=L and $\overline{\text{CAS}}$=$\overline{\text{WE}}$=H that previously encoded an activate command is unused.

As in previous SDRAM encodings, A10 is used to select command variants: auto-precharge on read and write commands, and one bank vs. all banks for the precharge command. It also selects two variants of the ZQ calibration command.

As in DDR3, A12 is used to request *burst chop*: truncation of an 8-transfer burst after four transfers. Although the bank is still busy and unavailable for other commands until eight transfer times have elapsed, a different bank can be accessed.

Also, the number of bank addresses has been increased greatly. There are four bank select bits to select up to 16 banks within each DRAM: two bank address bits (BA0, BA1), and two bank group bits (BG0, BG1). There are additional timing restrictions when accessing banks within the same bank group; it is faster to access a bank in

DDR4 command encoding[51]

| ommand | $\overline{CS}$ | BG1–0, BA1–0 | $\overline{ACT}$ | A17 | A16 / RAS | A15 / CAS | A14 / WE | A13 | A12 BC | A11 | A10 AP | A9–0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| eselect o eration) | H | X | | | | | | | | | | |
| ctive ctivate): en a row | L | Bank | L | Row address | | | | | | | | |
| eration | L | V | H | V | H | H | H | V | | | | |
| libration | L | V | H | V | H | H | L | V | | | Long | V |
| ead (BC, rst chop) | L | Bank | H | V | H | L | H | V | BC | V | AP | Column |
| rite (AP, to- echarge) | L | Bank | H | V | H | L | L | V | BC | V | AP | Column |
| assigned, served | L | V | v | V | L | H | H | V | | | | |
| echarge banks | L | V | H | V | L | H | L | V | | | H | V |
| echarge e bank | L | Bank | H | V | L | H | L | V | | | L | V |
| efresh | L | V | H | V | L | L | H | V | | | | |
| ode gister set IR0–MR6) | L | Register | H | L | L | L | L | L | Data | | | |

gnal level (H, high · L, low · V, either low or high, a valid signal · X, irrelevant) · Logic level ( Active · Inactive · Not erpreted)

a different bank group.

In addition, there are three chip select signals (C0, C1, C2), allowing up to eight stacked chips to be placed inside a single DRAM package. These effectively act as three more bank select bits, bringing the total to seven (128 possible banks).

Standard transfer rates are 1600, 1866, 2133, 2400, 2666, 2933, and 3200 MT/s[51][52] ($^{12}/_{15}$, $^{14}/_{15}$, $^{16}/_{15}$, $^{18}/_{15}$, $^{20}/_{15}$, $^{22}/_{15}$, and $^{24}/_{15}$ GHz clock frequencies, double data rate), with speeds up to DDR4-4800 (2400 MHz clock) commercially available.[53]

## Design considerations

The DDR4 team at Micron Technology identified some key points for IC and PCB design:[54]

IC design:[54]

- VrefDQ calibration (DDR4 "requires that VrefDQ calibration be performed by the controller");

- New addressing schemes ("bank grouping", ACT to replace RAS, CAS, and WE commands, PAR and Alert for error checking and DBI for data bus inversion);
- New power saving features (low-power auto self-refresh, temperature-controlled refresh, fine-granularity refresh, data-bus inversion, and CMD/ADDR latency).

Circuit board design:[54]

- New power supplies (VDD/VDDQ at 1.2 V and wordline boost, known as VPP, at 2.5 V);
- VrefDQ must be supplied internal to the DRAM while VrefCA is supplied externally from the board;
- DQ pins terminate high using pseudo-open-drain I/O (this differs from the CA pins in DDR3 which are center-tapped to VTT).[54]

Rowhammer mitigation techniques include larger storage capacitors, modifying the address lines to use address space layout randomization and dual-voltage I/O lines that further isolate potential boundary conditions that might result in instability at high write/read speeds.

### Module packaging

DDR4 memory is supplied in 288-pin dual in-line memory modules (DIMMs), similar in size to 240-pin DDR3 DIMMs. The pins are spaced more closely (0.85 mm instead of 1.0) to fit the increased number within the same 5¼ inch (133.35 mm) standard DIMM length, but the height is increased slightly (31.25 mm/1.23 in instead of 30.35 mm/1.2 in) to make signal routing easier, and the thickness is also increased (to 1.2 mm from 1.0) to accommodate more signal layers.[55] DDR4 DIMM modules have a slightly curved edge connector so not all of the pins are engaged at the same time during module insertion, lowering the insertion force.[14]

DDR4 SO-DIMMs have 260 pins instead of the 204 pins of DDR3 SO-DIMMs, spaced at 0.5 rather than 0.6 mm, and are 2.0 mm wider (69.6 versus 67.6 mm), but remain the same 30 mm in height.[56]

For its Skylake microarchitecture, Intel designed a SO-DIMM package named UniDIMM, which can be populated with either DDR3 or DDR4 chips. At the same time, the integrated memory controller (IMC) of Skylake CPUs is announced to be capable of working with either type of memory. The purpose of UniDIMMs is to help in the market transition from DDR3 to DDR4, where pricing and availability may make it undesirable to switch the RAM type. UniDIMMs have the same dimensions and number of pins as regular DDR4 SO-DIMMs, but the edge connector's notch is placed differently to avoid accidental use in incompatible DDR4 SO-DIMM sockets.[57]

## Modules

### JEDEC standard DDR4 module

**CAS latency (CL)**
: Clock cycles between sending a column address to the memory and the beginning of the data in response

**tRCD**
: Clock cycles between row activate and reads/writes

**tRP**
: Clock cycles between row precharge and activate

DDR4-xxxx denotes per-bit data transfer rate, and is normally used to describe DDR chips. PC4-xxxxx denotes overall transfer rate, in megabytes per second, and applies only to modules (assembled DIMMs). Because DDR4 memory modules transfer data on a bus that is 8 bytes (64 data bits) wide, module peak transfer rate is

| Standard name | Memory clock (MHz) | I/O bus clock (MHz) | Data rate (MT/s) | Module name | Peak transfer rate (MB/s) | Timings CL-tRCD-tRP | CAS latency (ns) |
|---|---|---|---|---|---|---|---|
| DDR4-1600J*<br>DDR4-1600K<br>DDR4-1600L | 200 | 800 | 1600 | PC4-12800 | 12800 | 10-10-10<br>11-11-11<br>12-12-12 | 12.5<br>13.75<br>15 |
| DDR4-1866L*<br>DDR4-1866M<br>DDR4-1866N | 233.33 | 933.33 | 1866.67 | PC4-14900 | 14933.33 | 12-12-12<br>13-13-13<br>14-14-14 | 12.857<br>13.929<br>15 |
| DDR4-2133N*<br>DDR4-2133P<br>DDR4-2133R | 266.67 | 1066.67 | 2133.33 | PC4-17000 | 17066.67 | 14-14-14<br>15-15-15<br>16-16-16 | 13.125<br>14.063<br>15 |
| DDR4-2400P*<br>DDR4-2400R<br>DDR4-2400T<br>DDR4-2400U | 300 | 1200 | 2400 | PC4-19200 | 19200 | 15-15-15<br>16-16-16<br>17-17-17<br>18-18-18 | 12.5<br>13.32<br>14.16<br>15 |
| DDR4-2666T<br>DDR4-2666U<br>DDR4-2666V<br>DDR4-2666W | 333.33 | 1333.33 | 2666.67 | PC4-21333 | 21333.33 | 17-17-17<br>18-18-18<br>19-19-19<br>20-20-20 | 12.75<br>13.50<br>14.25<br>15 |
| DDR4-2933V<br>DDR4-2933W<br>DDR4-2933Y<br>DDR4-2933AA | 366.67 | 1466.67 | 2933.33 | PC4-23466 | 23466.67 | 19-19-19<br>20-20-20<br>21-21-21<br>22-22-22 | 12.96<br>13.64<br>14.32<br>15 |
| DDR4-3200W<br>DDR4-3200AA<br>DDR4-3200AC | 400 | 1600 | 3200 | PC4-25600 | 25600 | 20-20-20<br>22-22-22<br>24-24-24 | 12.5<br>13.75<br>15 |

calculated by taking transfers per second and multiplying by eight.[58]

## Successor

At the 2016 Intel Developer Forum, the future of DDR5 SDRAM was discussed. The specifications were finalized at the end of 2016 – but no modules will be available before 2020.[59] Other memory technologies – namely HBM in version 3 and 4[60] – aiming to replace DDR4 have also been proposed.

In 2011, JEDEC published the Wide I/O 2 standard; it stacks multiple memory dies, but does that directly on top of the CPU and in the same package. This memory layout provides higher bandwidth and better power performance than DDR4 SDRAM, and allows a wide interface with short signal lengths. It primarily aims to replace various mobile DDR*X* SDRAM standards used in high-performance embedded and mobile devices, such as smartphones.[61][62] Hynix proposed similar High Bandwidth Memory (HBM), which was published as JEDEC JESD235. Both Wide I/O 2 and HBM use a very wide parallel memory interface, up to 512 bits wide for Wide I/O 2 (compared to 64 bits for DDR4), running at a lower frequency than DDR4.[63] Wide I/O 2 is targeted at high-performance compact devices such as smartphones, where it will be integrated into the processor or system on a chip (SoC) packages. HBM is targeted at graphics memory and general computing, while HMC targets high-end servers and enterprise applications.[63]

Micron Technology's Hybrid Memory Cube (HMC) stacked memory uses a serial interface. Many other computer buses have migrated towards replacing parallel buses with serial buses, for example by the evolution of Serial ATA replacing Parallel ATA, PCI Express replacing PCI, and serial ports replacing parallel ports. In general, serial buses are easier to scale up and have fewer wires/traces, making circuit boards using them easier to design.[64][65][66]

In the longer term, experts speculate that non-volatile RAM types like PCM (phase-change memory), RRAM (resistive random-access memory), or MRAM (magnetoresistive random-access memory) could replace DDR4 SDRAM and its successors.[67]

GDDR5 SGRAM is a graphics type of DDR3 synchronous graphics RAM, which was introduced before DDR4, and is not a successor to DDR4.

## See also

- Synchronous dynamic random access memory – main article for DDR memory types
- List of device bandwidths
- Memory timings

## Notes

a. Some factory-overclocked DDR3 memory modules operate at higher frequencies, up to 1600 MHz.[11]

b. As a prototype, this DDR4 memory module has a flat edge connector at the bottom, while production DDR4 DIMM modules have a slightly curved edge connector so not all of the pins are engaged at a time during module insertion, lowering the insertion force.[14]

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# External links

- *Main Memory: DDR3 & DDR4 SDRAM* (http://www.jedec.org/category/technology-focus-area/main-memory-ddr3-ddr4-sdram), JEDEC, DDR4 SDRAM STANDARD (JESD79-4) (http://www.jedec.org/standards-documents/docs/jesd79-4)
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