STUDY OF IMPLEMENTATION OF PENTIUM PROCESSOR IN VHDL

The Pentium is fully compatible with previous Intel processor, but it also different from them in many ways. The Pentium features **twin data pipelines**, which enable it to execute two instructions at a same time. Intel calls the capability to execute two instructions at the same time **superscalar** technology. This technology provides additional performance compared with the 486. With superscalar technology, the Pentium can execute many instructions at a rate of **two instructions per cycle**. Superscalar architecture usually is associated with high-output RISC chips. The Pentium is one of the first CISC chips to be considered superscalar.

The two instruction pipelines within the chip are called the **u- and v-pipes**. The u-pipe, which is the primary pipe, can execute all integer and floating-point instructions. The v-pipe is a secondary pipe that can execute only simple integer instructions and certain floating –point instructions. The process of operating on two instructions simultaneously in the different pipes is called pairing. Not all sequentially executing instructions can be paired, and when pairing is not possible, only the u-pipe is used. To optimize the Pentium's efficiency, you can recompile software to allow more instructions to be paired.

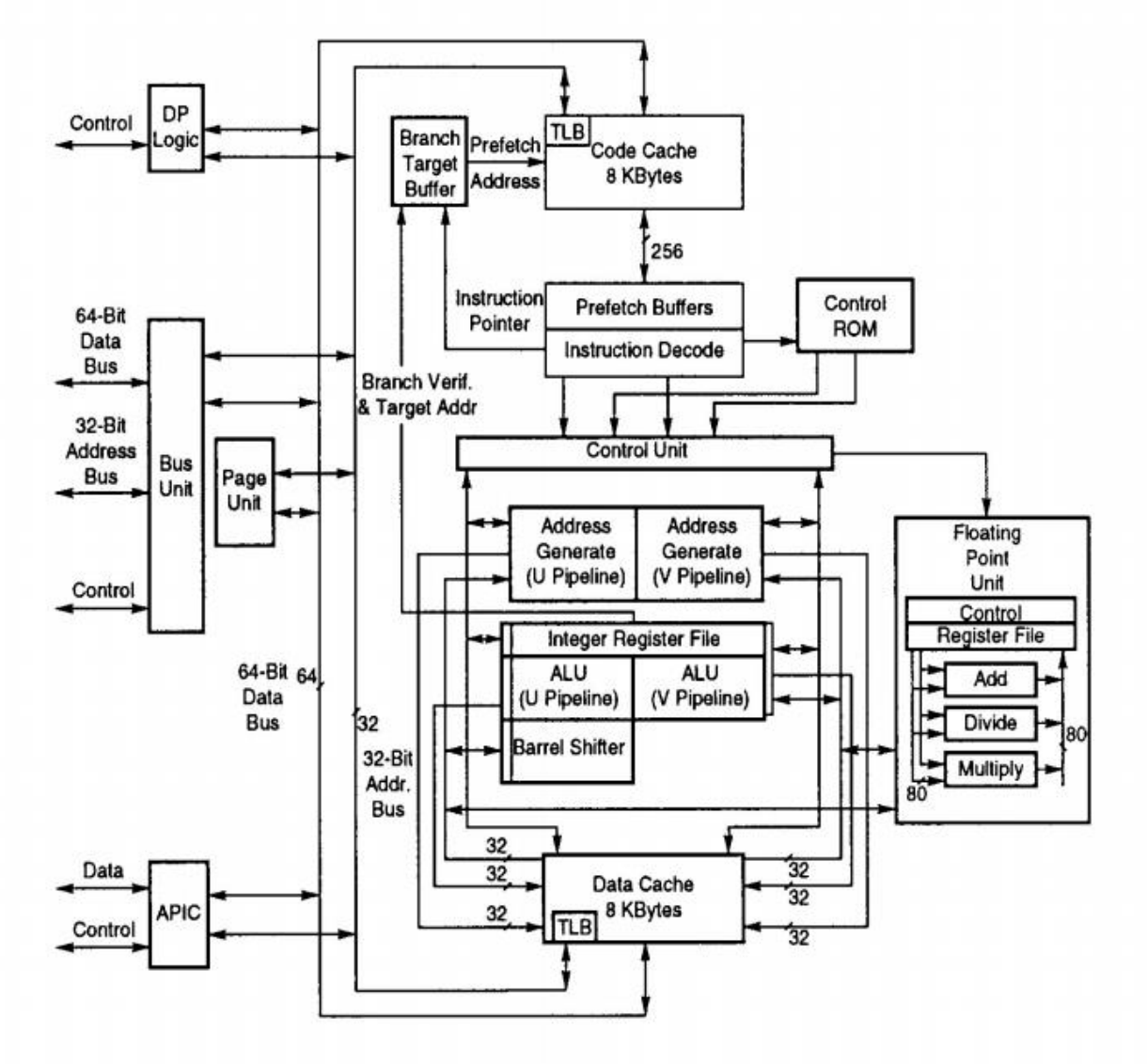
The Pentium processor has a Branch Target Buffer (**BTB**), which employs a technique called **branch predication**. It minimizes stalls in one or more of the pipes caused by delays in fetching instructions that branch to non-linear memory locations. The BTB attempts to predict whether a program branch will be taken, and then fetches the appropriate instructions. The use of branch prediction enables the Pentium to keep both pipelines operating at full speed.

The Pentium has a **32-bit address** bus width, given it the same 4GB memory-addressing capabilities. But the Pentium expands the **data to 64 bits**, which means that it can more twice as much data into or out of the CPU. The 66-bit data bus requires that system memory be accessed 64 bits wide, which means that each bank of memory is 64 bits. Most Pentium systems use 32-bits wide SIMMs – two of these SIMMs per bank of memory. Most Pentium motherboards have at least four of these 32-bit SIMM sockets, providing for a total of two banks of memory. The newest Pentium systems and most Pentium II systems today use DIMMs, which are 64 bits wide.

The Pentium has only 32-bit internal registers. As instructions are being processed internally, they are broken down into 32-bit instructions and data elements. The Pentium has **two separate internal 8KB caches**, compared with a single 8KB or 16KB cache in the 486. The cache-controller circuitry and the cache memory are embedded in the CPU chip. The cache mirrors the information in normal RAM by keeping a copy of the data and code from different memory locations. The Pentium cache also can hold information to be written to memory when the load on the CPU and other system components is less. The separate code and data caches are organized in a **two-way set associative** fashion, with each set split into lines of 32 bytes each. Each cache has a dedicated Translation Lookaside Buffer (**TIB**) that translates linear addresses to **physical addresses**.

You can configure the data cache as **write-back or write-through** on a line-by-line basis. When you use the writeback capability, the cache can store write operations and reads, further improving performance over read-only writethrough mode. Using write-back mode results in less activity between the CPU and system memory. The code cache is an inherently write-protected cache because it contains only execution instructions and not data, which are updated. Systems based on the Pentium can benefit greatly from secondary processor caches (L2), which usually consist of up to 512KB or more of extremely fast (15ns or less). Static RAM (SRAM) chips. When the CPU fetches data that is not already available in its internal processor (LI) cache, wait states slow the CPU. If the data already is in the secondary processor cache, however, the CPU can go ahead with its work without pausing for wait states.

The Pentium uses a BiCMOS process and superscalar architecture to achieve the high level of performance expected from the chip. The Pentium contains an internal math coprocessor or **FPU**. The FPU in the Pentium has been rewritten and performs significantly better than the FPU in the 486. The Pentium FPU is estimated at two to as much as 10 times faster than the FPU in the 486. In addition, the two standard instruction pipelines in the Pentium provide two units to handle standard integer math.



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