

COMPUTER ARCHITECTURE OF WAREHOUSE SCALE COMPTS

the total storage capacity

## DOMAIN SPECIFIC ARCHITECTURE

- ① "tensorflow a system for large scale machine Arch." usenix nov 2016.
  - ② norman joppa, nishant patil, david patterson.  
motivation for evolution of ist tensor processing unit.
  - ③ a domain specific arch. for ML apps.
  - ④ jeff , cliff yoon.  
a golden age: empowering the ML revolution.
  - ⑤ norman p joppa.  
any data center perf. analysis of a TPU.  
44th international symposium, Jun 2017.
- 4 DSAs discussed in book
- TPU - cotapult - - Crust by intel.
  - pixel visual core Intel. 7.4 - - 7.7.

## GUIDELINES

- use dedicated memories to minimize distance over which data is moved.

data movement is managed by SW.

- invest in resources
- use easiest form of utilism that matches the domain.
- reduce the data size and type to simplest needed for the domain.
- use domain specific prog. lang. to port the code to DSA.

5 main instructions. TPU

- read host memory  $\rightarrow$  unified buffer.
- reads weights from weights memory into weight fifo for matrix unit.
- matrix multiply + stroke convolve multiply, dot, convolution.

- activate

non-linear functions for NN, relu, sigmoid, tanh.

- write host memory

TPU, 28 nm, 700 MHz,

1/3rd space = unified buffers.

1/4 space = matrix multiply unit.

[local data buffer + memory]

registers

flags

93

.. 20

