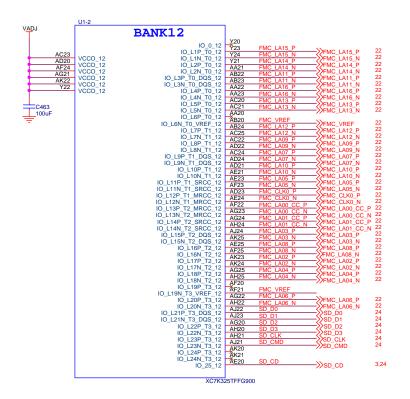
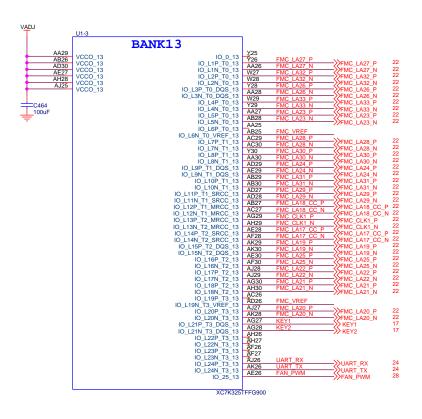


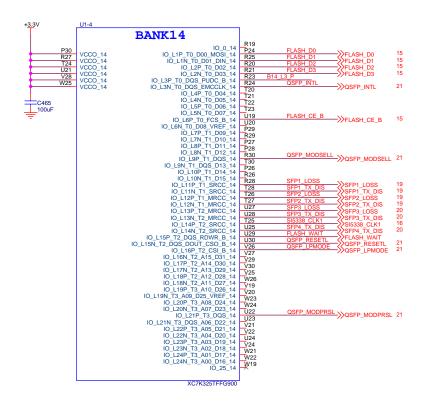
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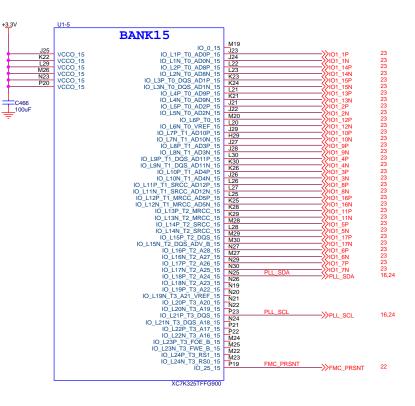






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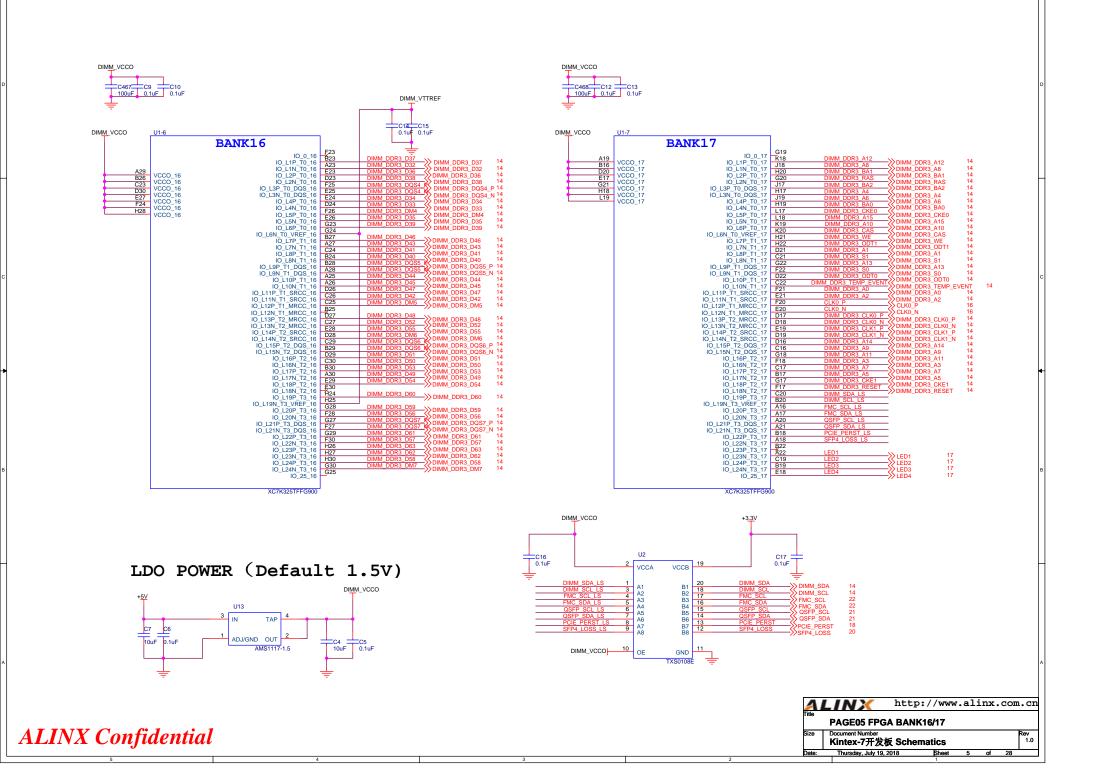
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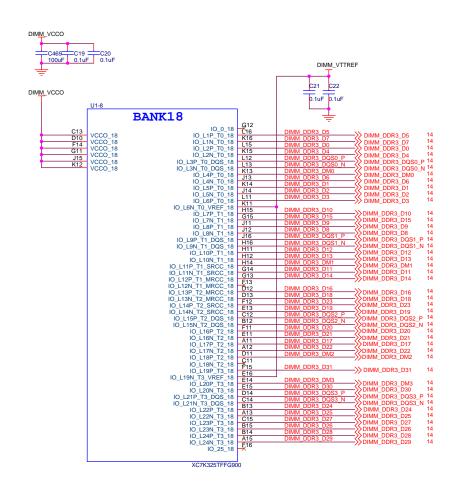
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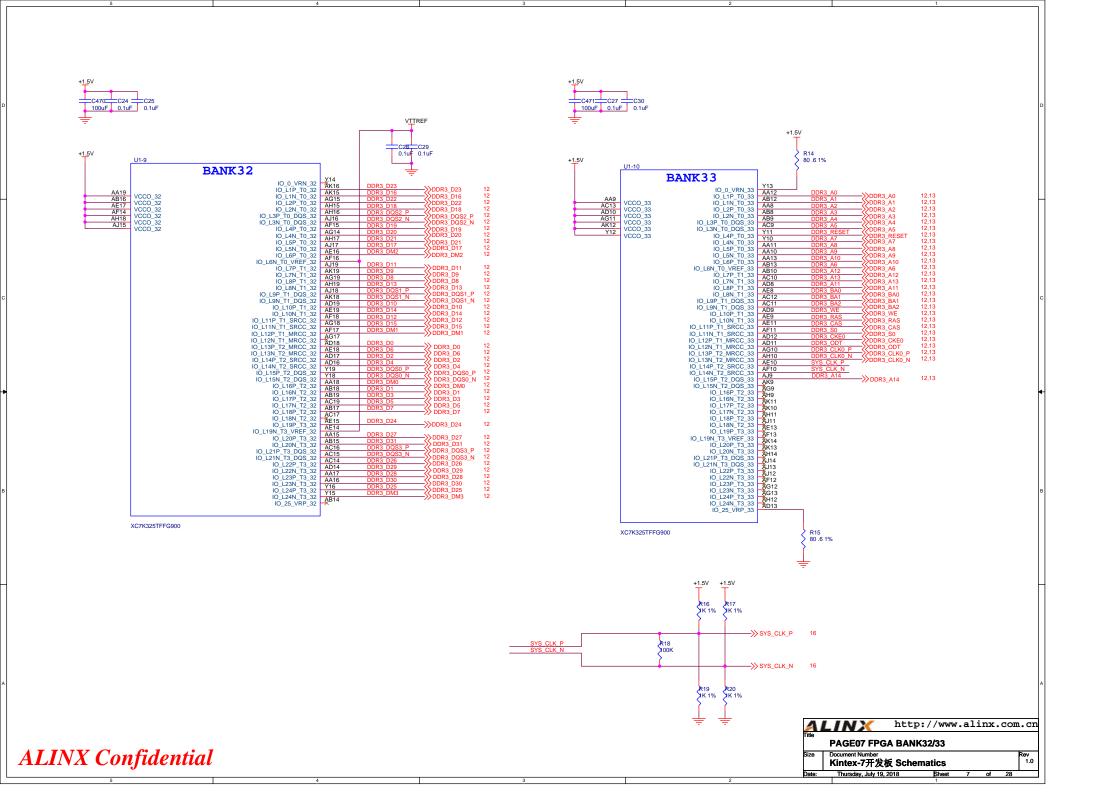


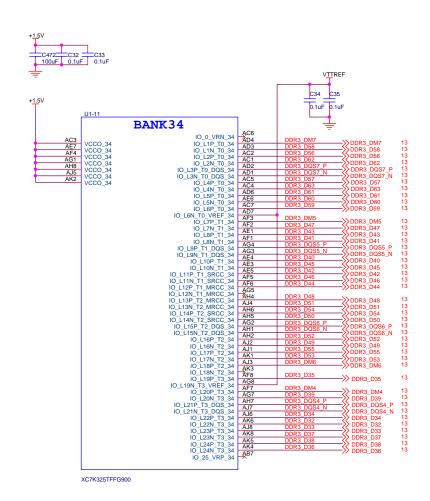


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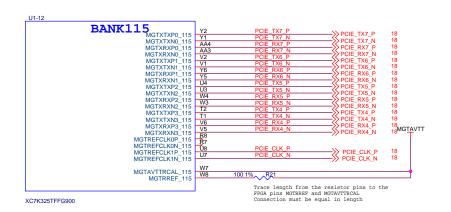


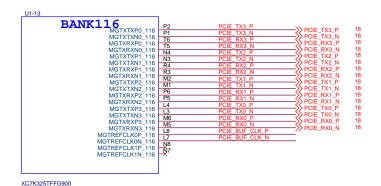


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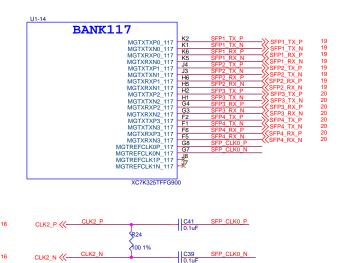
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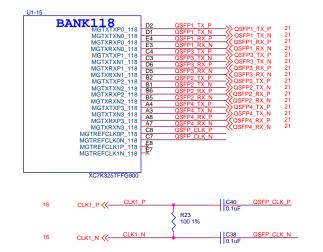
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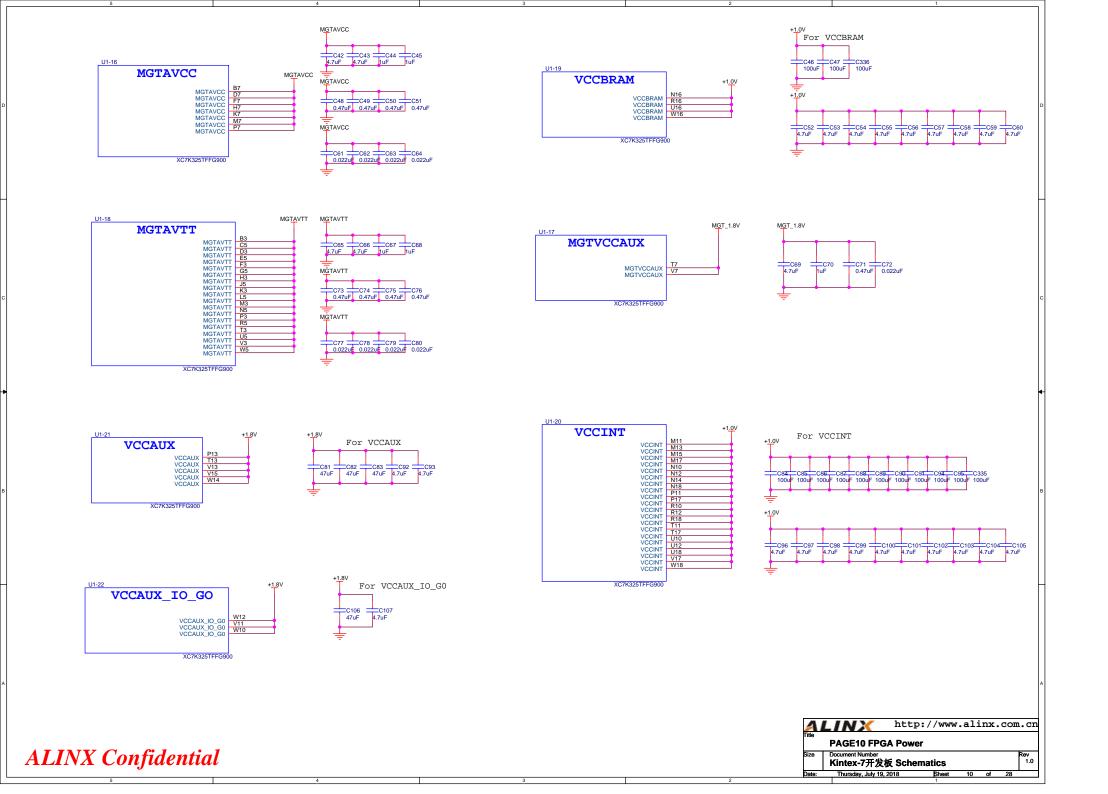
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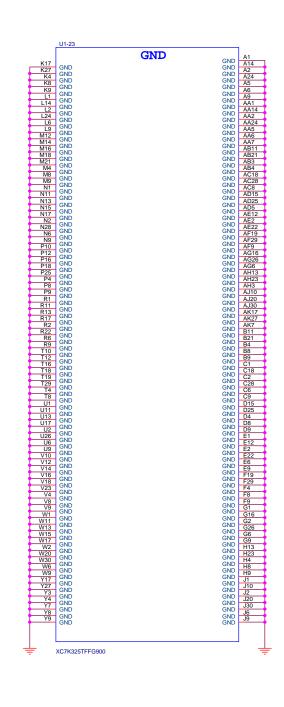




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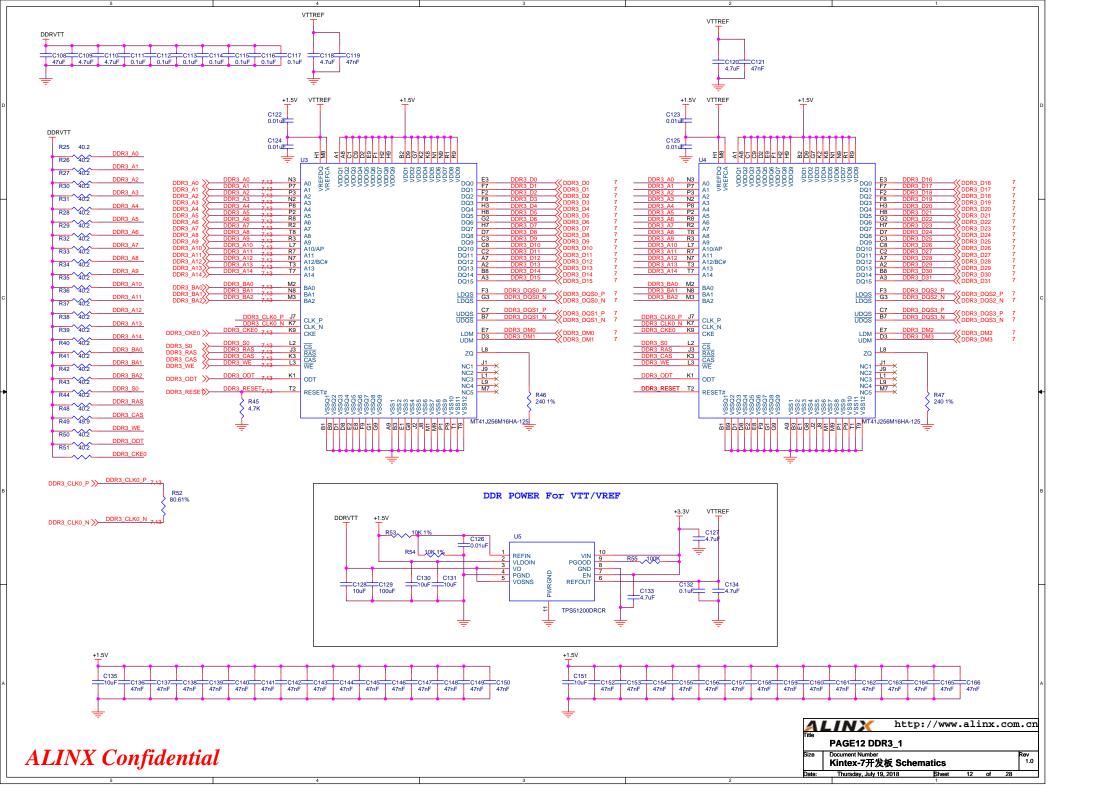
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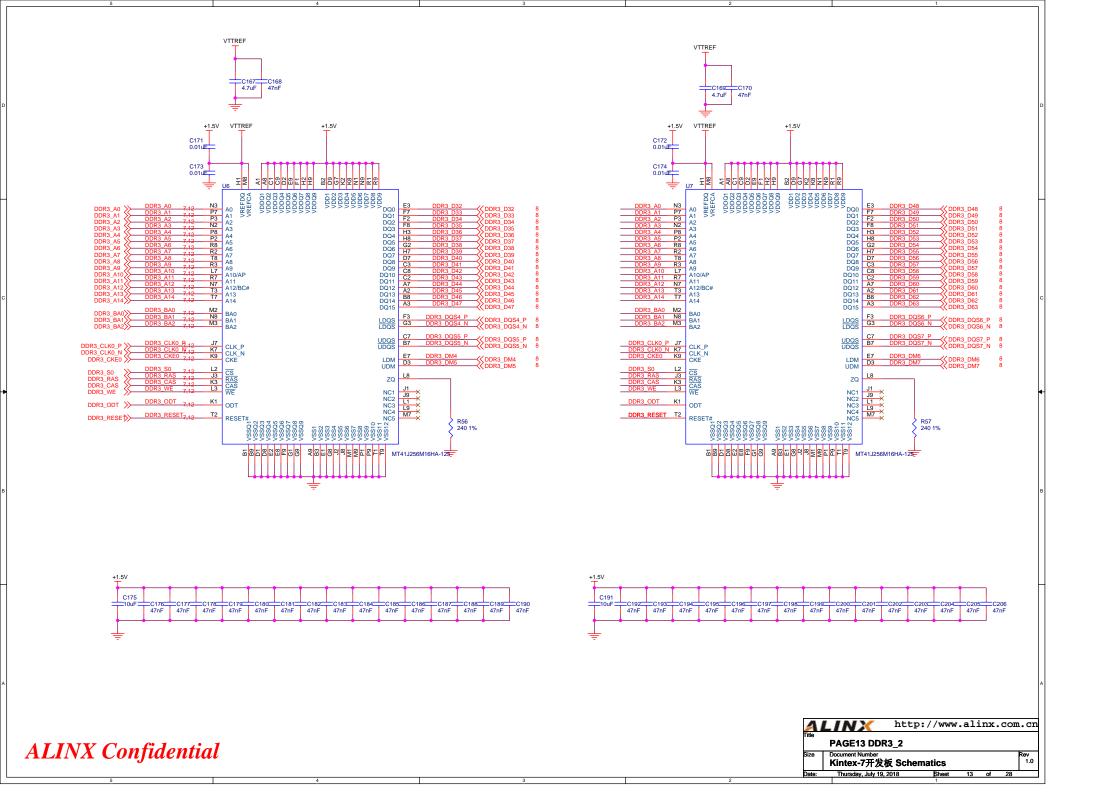
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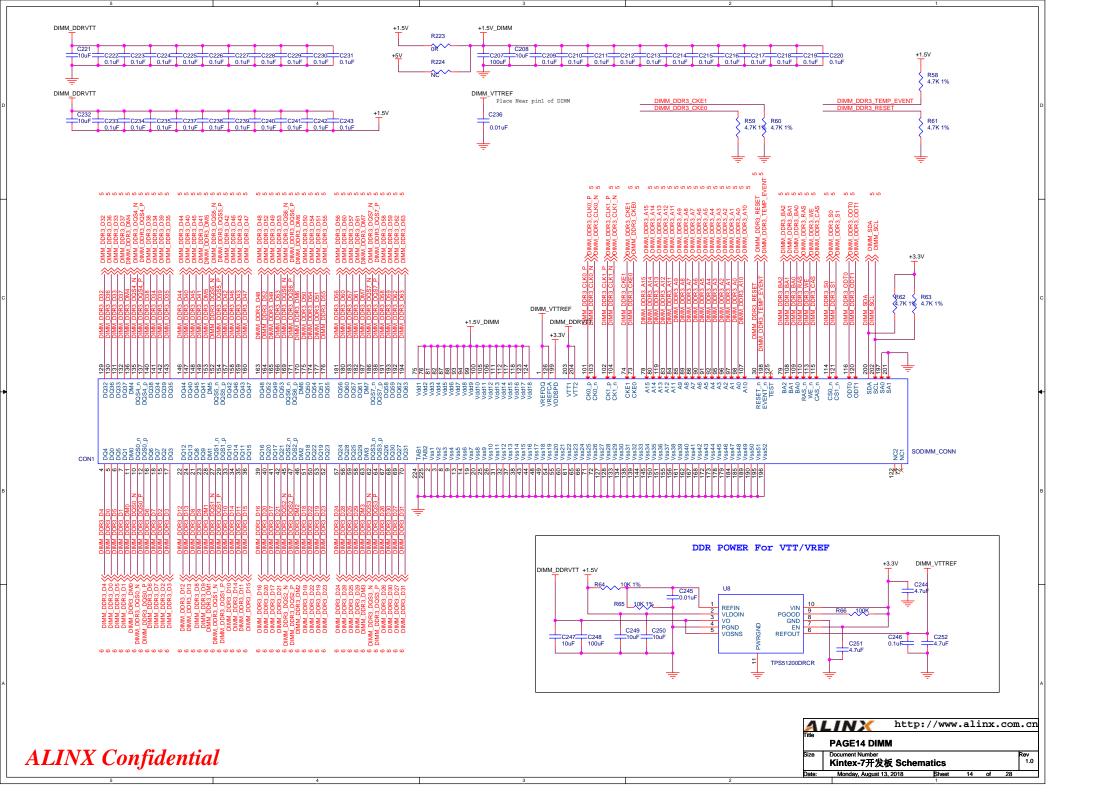
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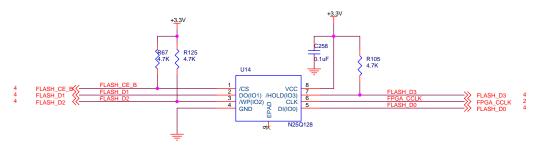
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FPGA CONFIG SPI



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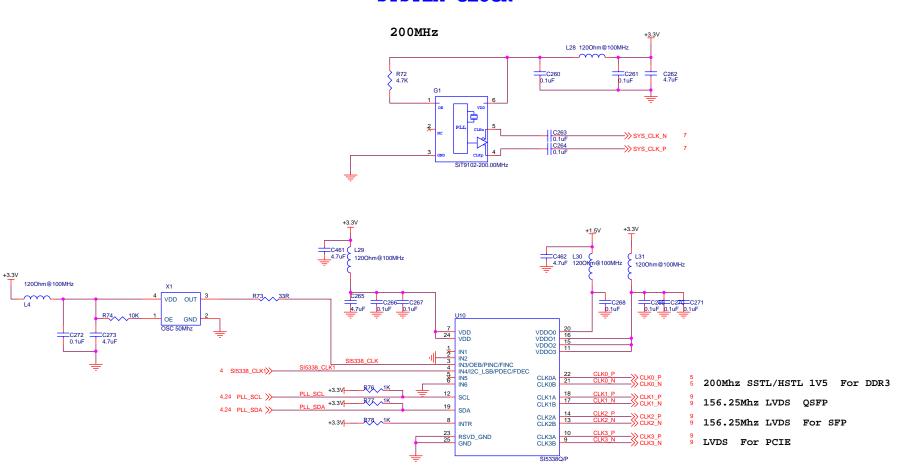
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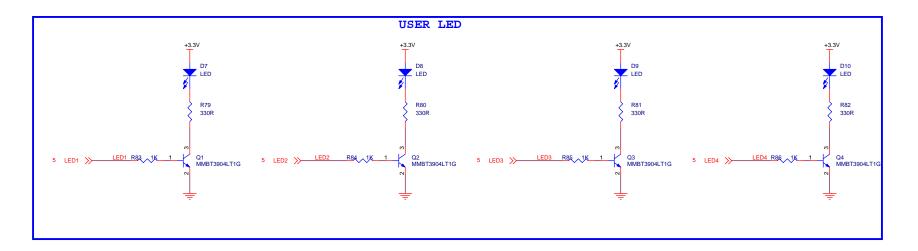
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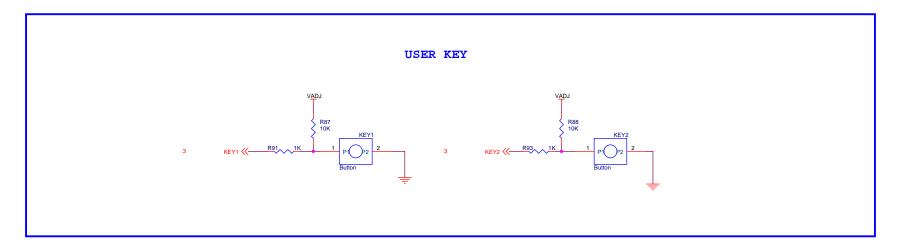
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SYSTEM CLOCK

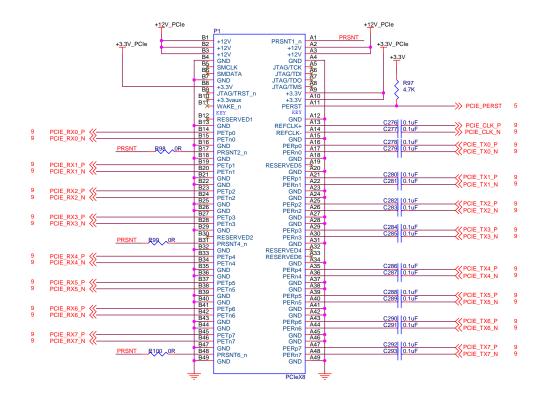




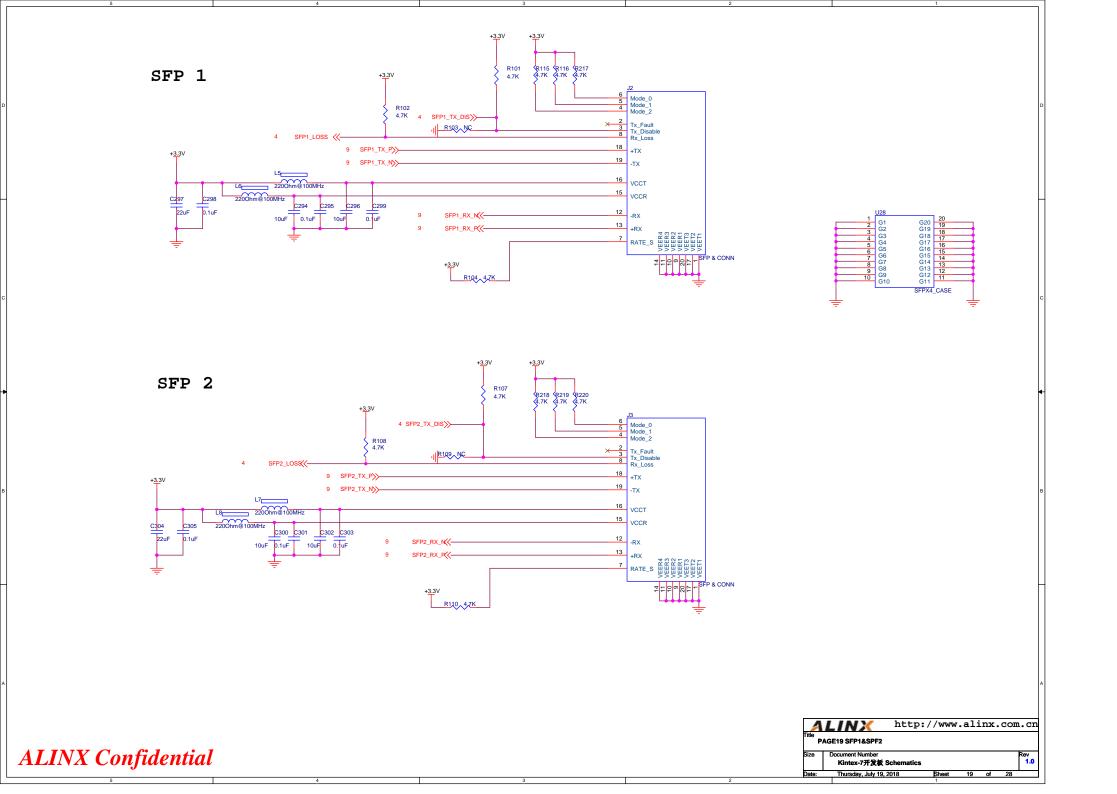


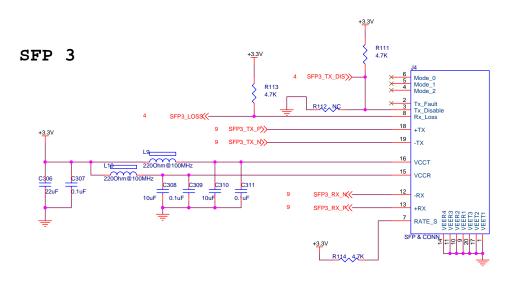


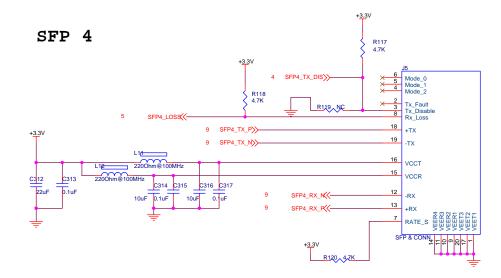
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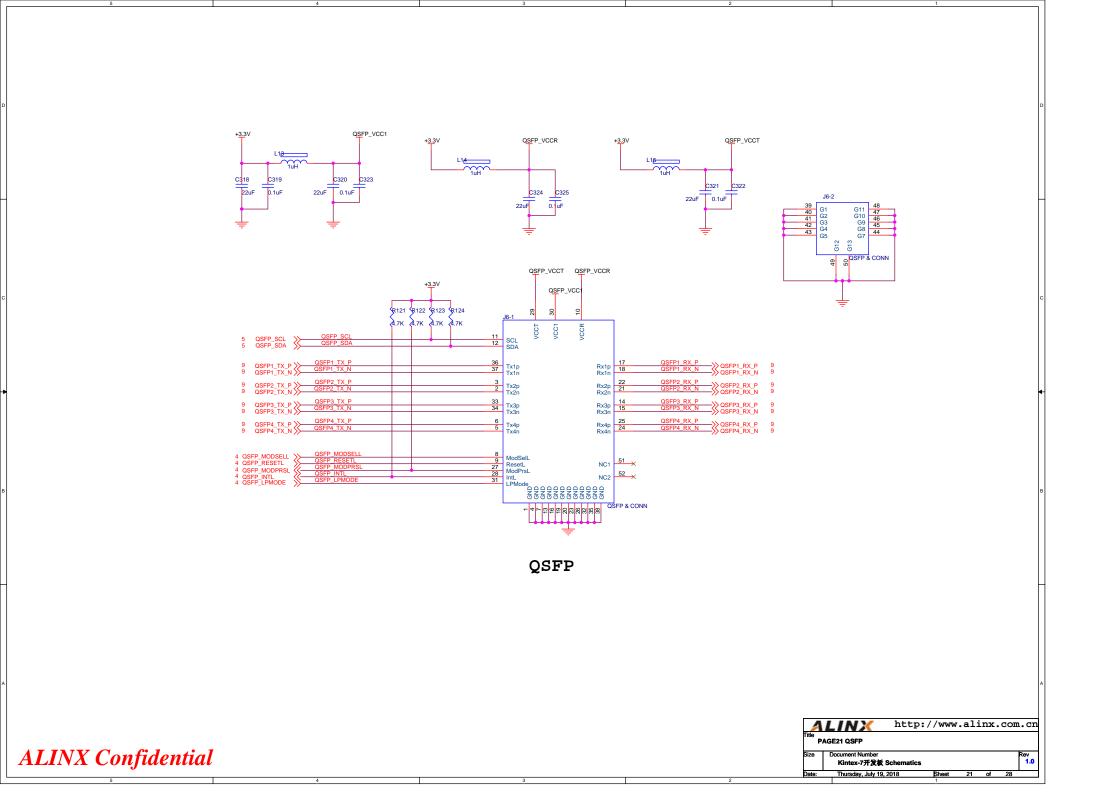
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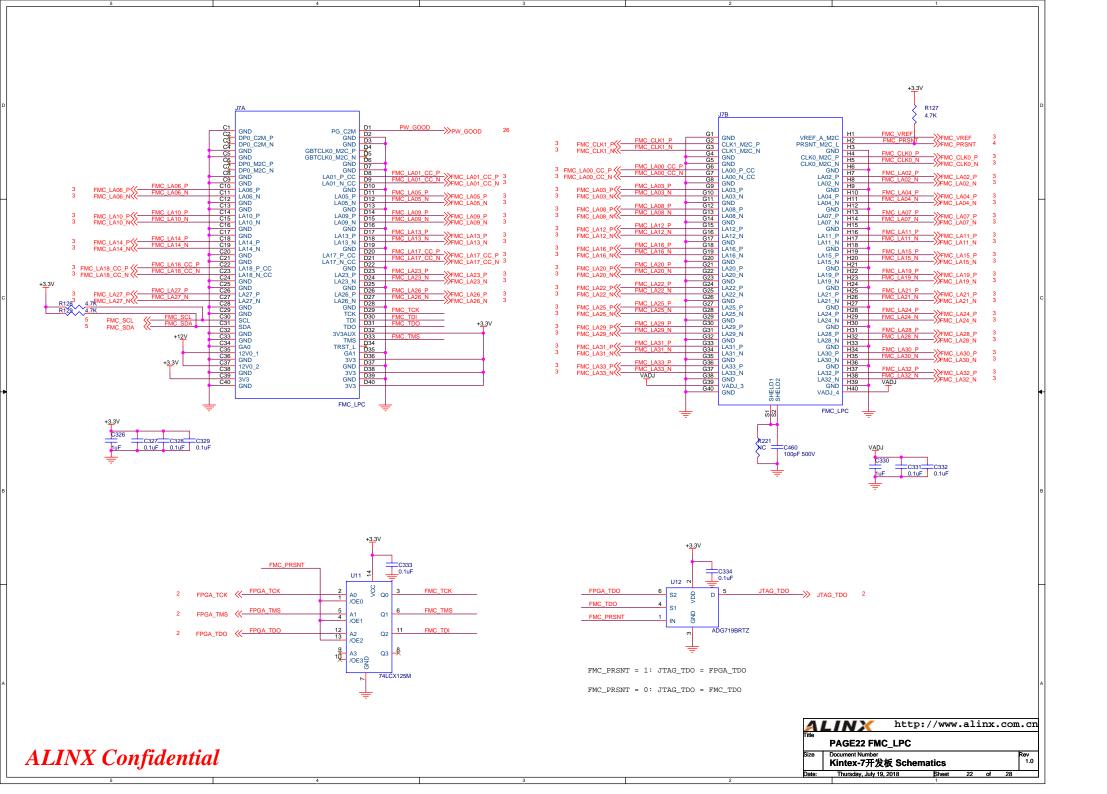


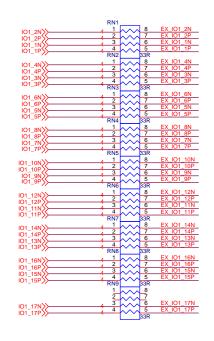




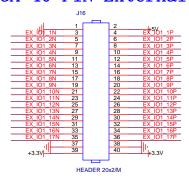
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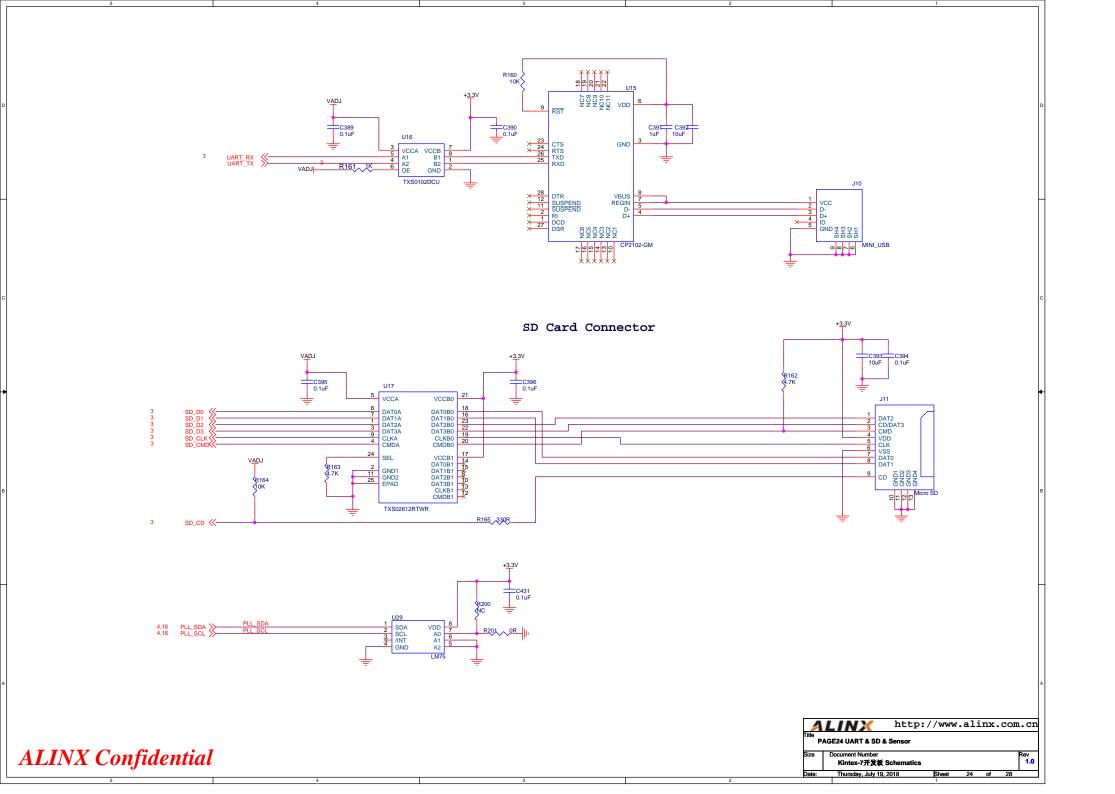


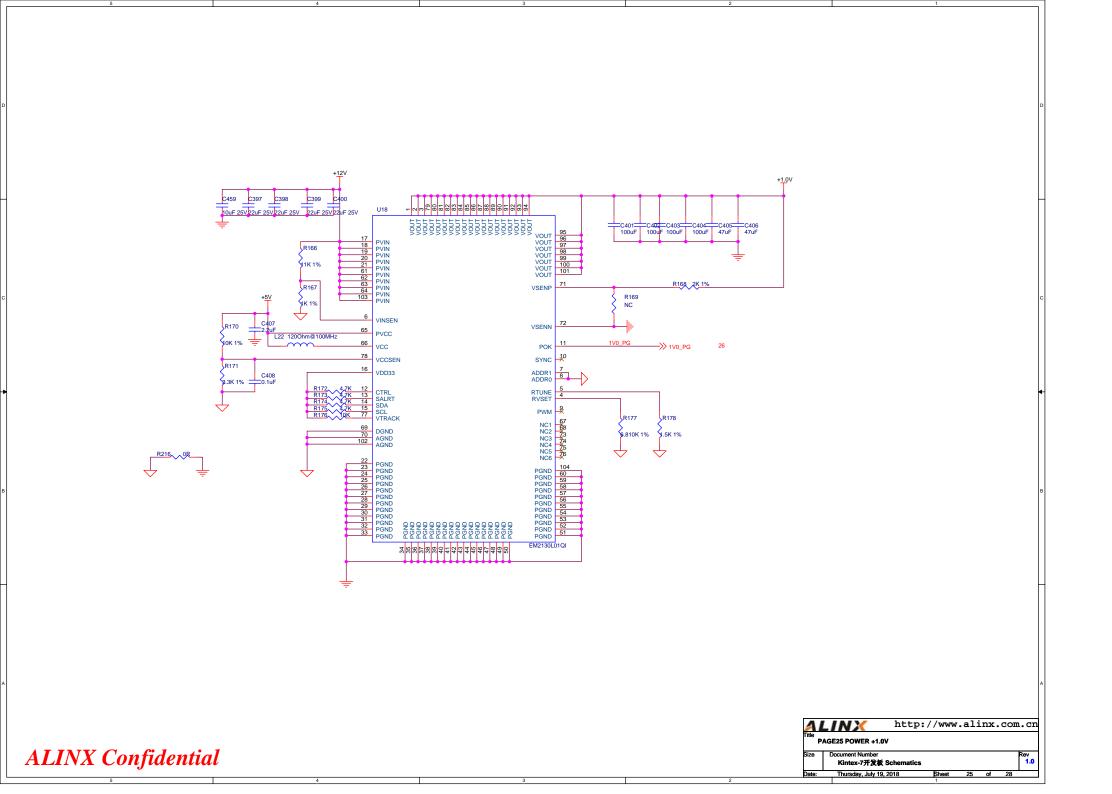


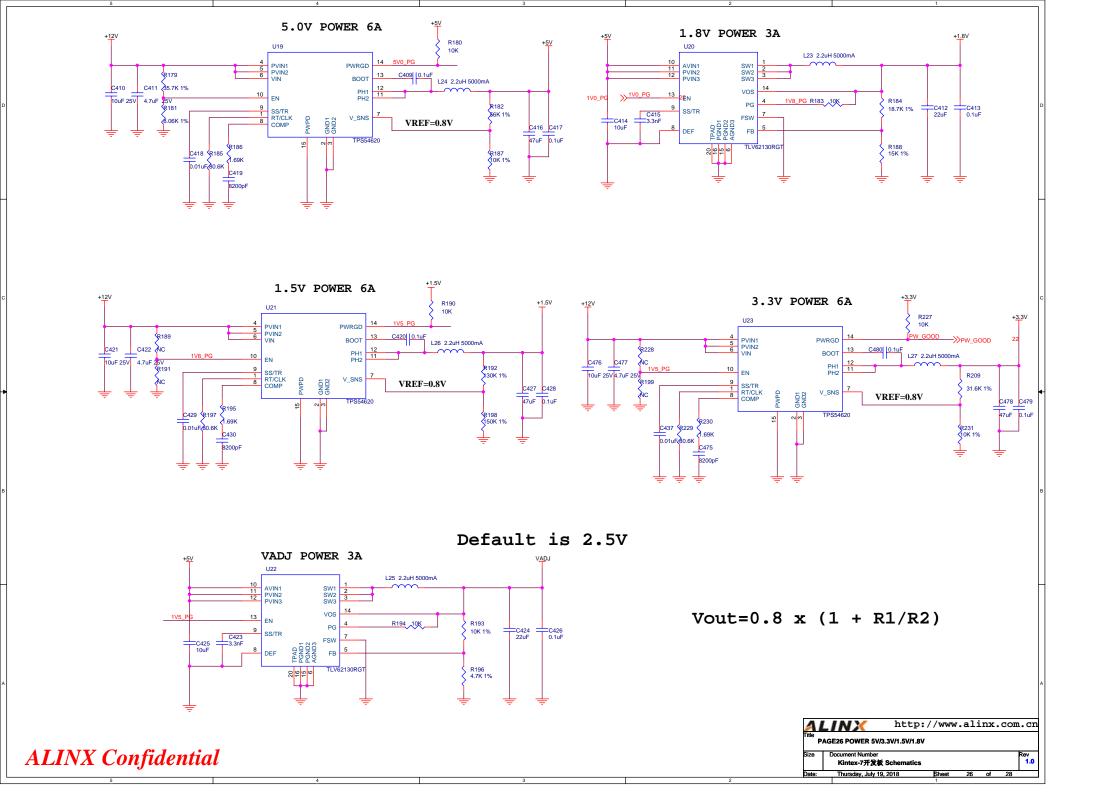


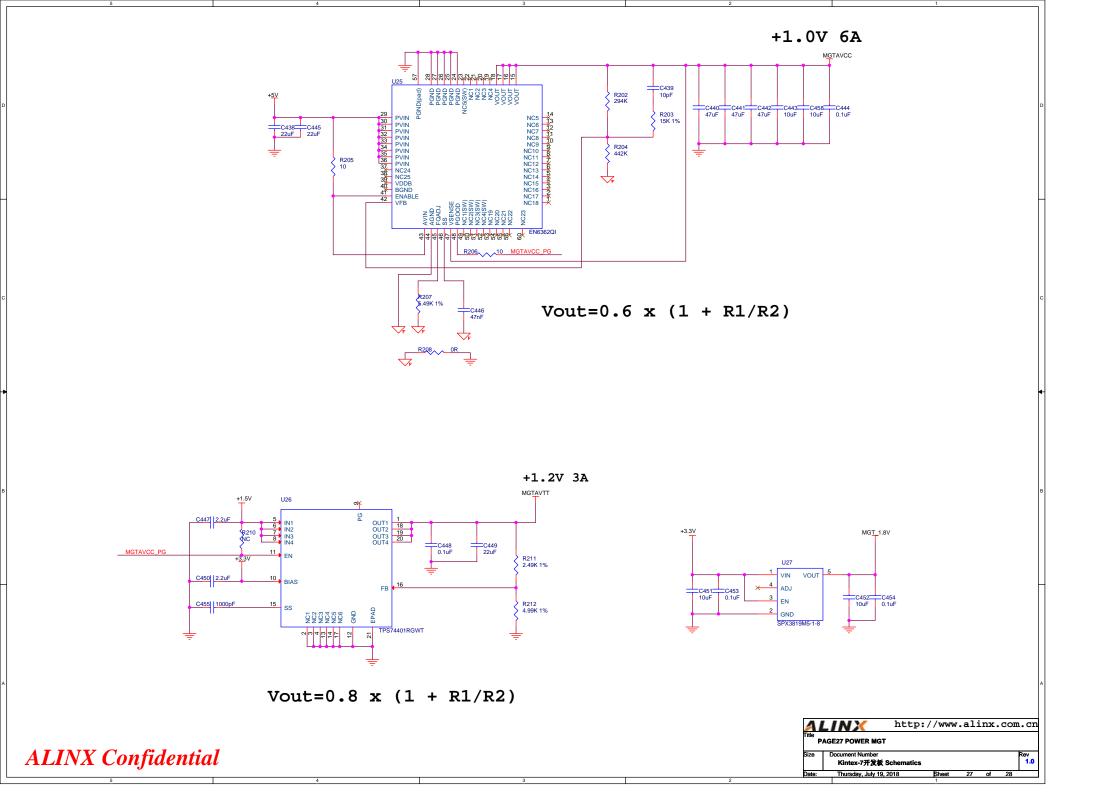
FPGA 40 PIN External IO

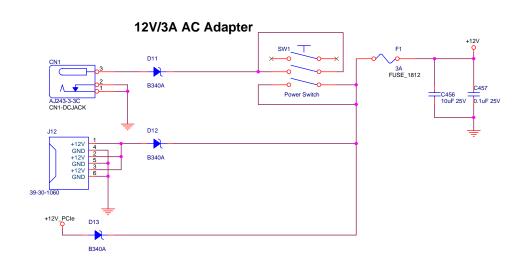




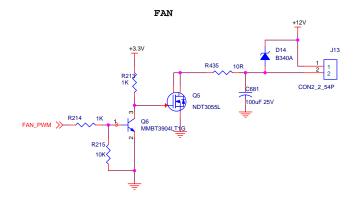












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