Lab Assignment #0

EE-126/COMP-46: Computer Engineering w/lab
Professor: Mark Hempstead **TA:** Parnian Mokri
Tufts University, Fall 2021

Due as per the class calendar, via 'provide'

The ultimate goal of this project is to design a pipelined version of a ARM processor that can detect control and data hazards. The functionality of the processor and its components should match the descriptions in the textbook unless otherwise noted. All work must be your own; copying of code will result in a zero for the project and a report to the administration.

Extra resources

Please refer to LabResourcesTutorials for more resources on using Questasim and VHDL tutorials. If you decide to use halligan's windows machine for your labs, every machine in Halligan Hall **Room 122** has Questasim installed and running. Make sure you save your files in a write-able directory. Halligan Facilities ae listed here.

List of assignments

- **Lab 0: Set up modelsim, simulate an AND gate with 2 inputs and 1 output**
- Lab 1: Basic Processor Components and Testbenches
- Lab 2: Remaining Processor Components including ALU, Memories, and control logic
- Lab 3: Implementation LEGv8: a single cycle processor that executes a subset of ARM v8-64bit ISA
- Lab 4: Pipelined processor with no hardware hazard detection
- Lab 5: Overcoming data-hazards using forwaring and stalling
- Lab 6: Overcoming control hazards by resolving conditional/unconditional branches in ID and using flushing
- Lab 7: Advanced Topics: open-ended team project (groups up to 2 people)

Lab Submission

Please submit your VHDL files *and* a PDF report via 'provide' command on the EE/CS machines. Please follow the announcement on Canvas about Provide to submit your labs and pay attention to messages you get when you try to provide.

VHDL Files: Submit the VHDL source files **(*.vhd)**[1] and any dependencies thereof. Use the entity descriptions provided at the end of this document.[2] These descriptions can also be found in assignment0.zip.

Report: Submit your report as a PDF**(*.pdf)**. Demonstrate the functionality of your code by providing waveforms as detailed in the Deliverables Section. Label/annotate important signals and events in your waveforms and then provide a brief description of what is happening.

Lab 0 Objectives

- Make sure you have set up your EECS account. You need this to be able to submit your labs. If you need a CS/ECE account, please email staff@eecs.tufts.edu
- If you are not familiar with VHDL, feel free to review VHDL_Tutorial_Fall2020.pdf on Canvas
- Implement AND2 in VHDL

[1] Do NOT submit your entire Modelsim project (including but not limited to ***.mpf** and files in **work/**)

[2] Submissions that fail to to follow any of these directions may be penalized at the discretion of the grader. If you have questions, contact the TA (Parnian Mokri: parnian.mokri@tufts.edu).

- Write a simple testbench for AND2.
- Run QuestaSim; you have two ways to run QuestaSim either
  - ssh to Tufts servers type ssh -X eecsUsername@homework.cs.tufts.edu and follow the instructions on QuestaSim_Instructions_on_Linux.pdf on canvas.
  - Install Modelsim on your computer. Please refer to QuestaSim_Windows_Install_Instruction.pdf on canvas.
- Verify functionality of AND2 module via simulation using Questasim
- Submit a report with the inputs and output waveform and analyze it

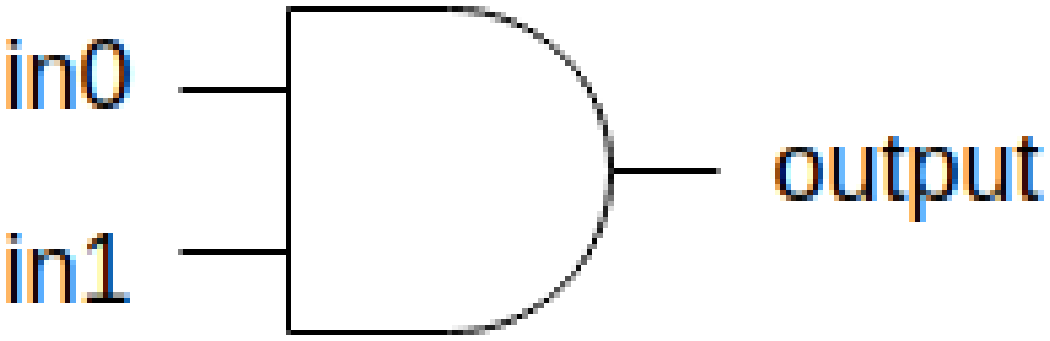

Figure 1: **A AND gate with two inputs and one output.**

Deliverables

VHDL Files:
AND2 with a testbench. These components are shown in Figure 1.

Report:

- State whether you are using the QuestaSim by ssh-ing to servers or downloading the student version.
- A brief explanation of your choices for modeling type (dataflow, behavioral, structural)
- Waveforms obtained by simulating your testbenches with brief descriptions
  - AND2: (no labeling is necessary)

Entity Descriptions **(provided in assignment0.zip)**

AND2

```
entity AND2 is
port (
      in0    : in  STD_LOGIC;
      in1    : in  STD_LOGIC;
      output : out STD_LOGIC -- in0 and in1
);
end AND2;
```

Provide

To provide,

- Log in to homework.cs.tufts.edu : ssh -X eecsUsername@homework.cs.tufts.edu
- Type: **provide ee126 lab0 "files"**
- Type **yes** for the following question: Are you ready to provide these for testing (yes or no)?
- Make sure you see the following message:
  your submission has been accepted!
  your submission is complete!