Lab Assignment #6

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EE-126/COMP-46: Computer Engineering w/lab

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Introduction + Purpose

In this lab, the hazard detection and forwarding modules were built for branch hazards on top of the last lab which was the pipelined cpu.

Components built

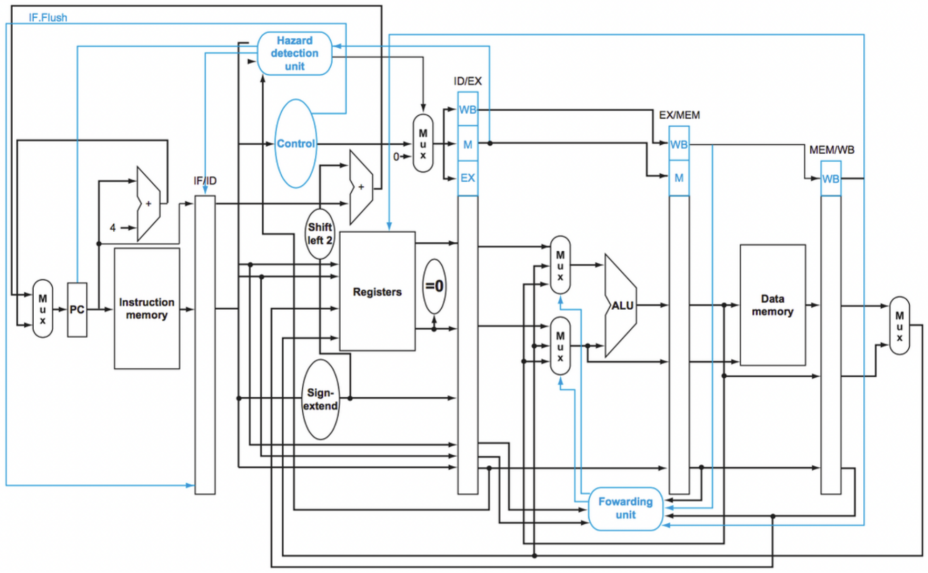

Figure 1: *Overall system diagram of the Hazard detection and Forwarding Units*

```
vcom -quiet -2008 *.vhd tb/*.vhd imem/*.vhd
vsim -quiet -c work.pipelinedcpu2_tb -do "log -r /*; run 500ns; exit" -wlf
pipelinedcpu2.wlf &&  wlf2vcd pipelinedcpu2.wlf -o pipelinedcpu2.vcd
```

Figure 2: *Commands to analyze and run the code*

Cycle	PC			
0	0	SUB X23, X20, X19	11001011000100110000001010010111	cb 13 02 97
1	4	CBZ X23, 5	10110100000000000000000010110111	b4 00 00 b7
2	8	ADD X9, X9, X9	10001011000010010000000100101001	8b 09 01 29
3	8			
4	12	SUB X24, X22, X21	11001011000101010000001011011000	cb 15 02 d8
5	16	CBZ X24, 3	10110100000000000000000001111000	b4 00 00 78
6	20	ADD X10, X10, X10	10001011000010100000000101001010	8b 0a 01 4a
7	20			
8	24	ADD X11, X11, X11	10001011000010110000000101101011	8b 0b 01 6b
9	28	ADD X12, X12, X12	10001011000011000000000110001100	8b 0c 01 8c
10	32	B 2	00010100000000000000000000000010	14 00 00 02
11	36	ADD X19, X19, X19	10001011000100110000001001110011	8b 13 02 73
12	40	ADD X20, X20, X20	10001011000101000000001010010100	8b 14 02 94

Figure 4: *Test program in Assembly, Binary, and Hex along with the associated cycles and PC counter*

Cycle	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
PC	0	4	8	8	12	16	20	20	28	32	36	40	44	48	52
SUB X23, X20, X19	IF	ID	EX	MEM	WB										
CBZ X23, 5		IF	ID*	ID	EX	MEM	WB								
ADD X9, X9, X9			IF*	IF	ID	EX	MEM	WB							
SUB X24, X22, X21					IF	ID	EX	MEM	WB						
CBZ X24, 3						IF	ID*	EX	MEM	WB					
ADD X10, X10, X10							IF*	Flush							
ADD X11, X11, X11															
ADD X12, X12, X12								IF	ID	EX	MEM	WB			
B 2									IF	ID	EX	MEM	WB		
ADD X19, X19, X19										IF	Flush				
ADD X20, X20, X20											IF	ID	EX	MEM	WB

Figure 5: *Test program and instructions with their associated pipeline phase for each clock cycle.*

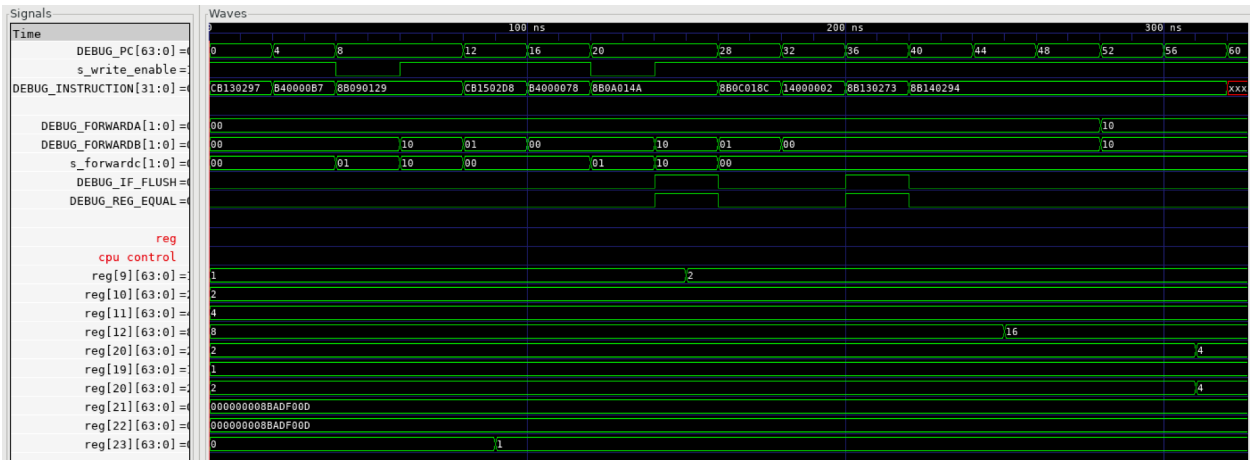

Figure 6: *Output waveforms from test program on pipelinedcpu2.vhd*

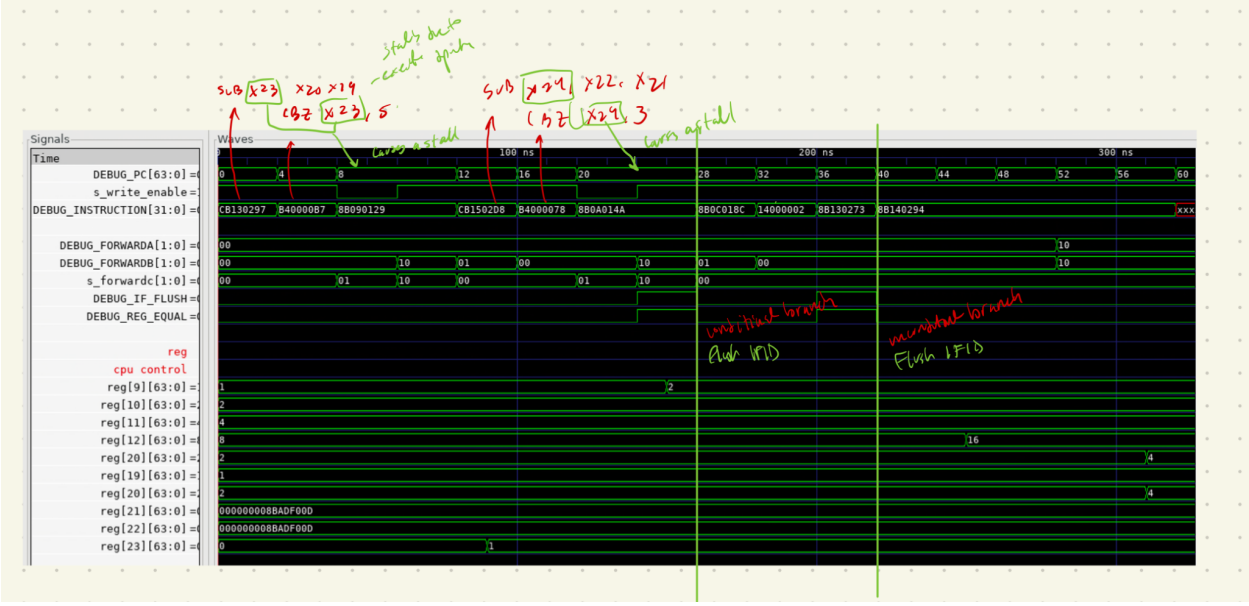

Figure 7: *Annotated Output waveforms from test program on pipelinedcpu2.vhd*

As seen in Figure 7, there several main events;

- There are two stalls and two flushes. The first one occurs because of the first two instructions and the second occurs because of the conflict between the fourth and fifth instructions. These stalls temporarily disable the ifid register and the pc write.
- There are also two flushes of the ifid register which occur when branches are successfully taken and the pc is enabled.