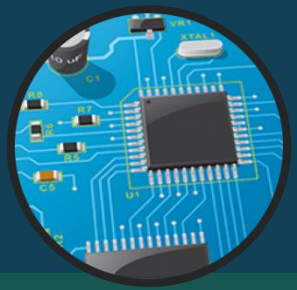
Introduction to 8088/8086 Architecture



Topic 6

Fall 2019

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Modes of operation

8086/8088 can be configured in two modes:

The minimum mode:

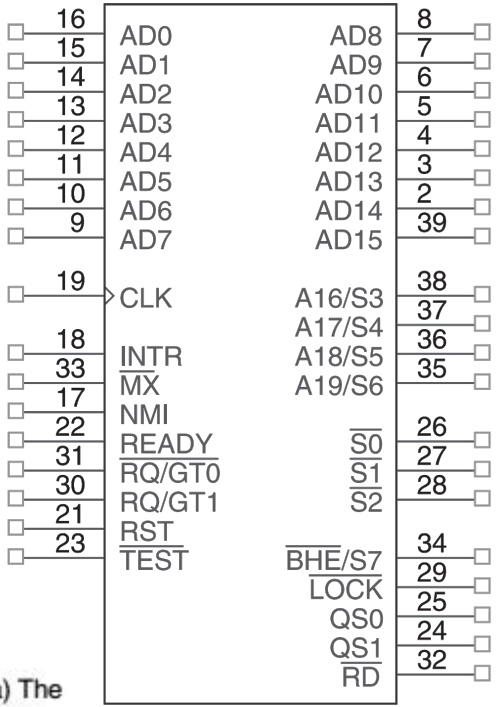
- Used for single processor system, where 8086/8088 directly generates all the necessary control signals

The maximum mode:

- Designed for multiprocessor systems, where an additional "Bus Controller" IC is required to generate the control signals. The processor controls the Bus controller using status codes

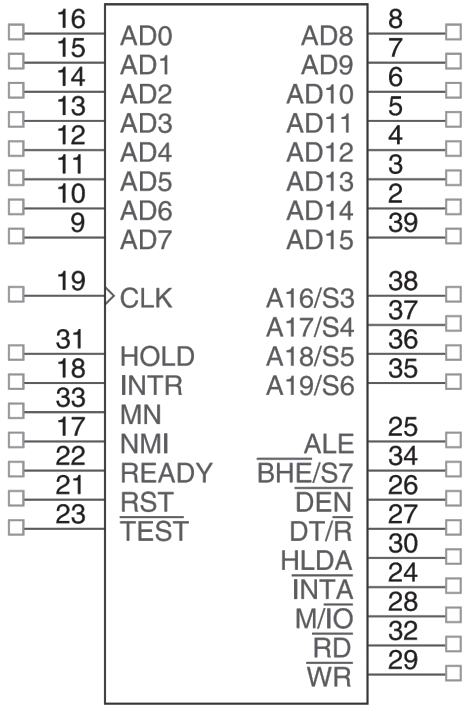
[2]

Pinout of 8086



8086MAX

(a)



8086MIN

(b)

FIGURE 9–1 (a) The pin-out of the 8086 in maximum mode; (b) the pin-out of the 8086 in minimum mode.

[3]

Pinout of 8086

Clock (pin 19)

- 8284 clock generator IC is connected to 8086/8

Reset (pin 21)

- Reboots the microprocessor

Vcc (pin 40)

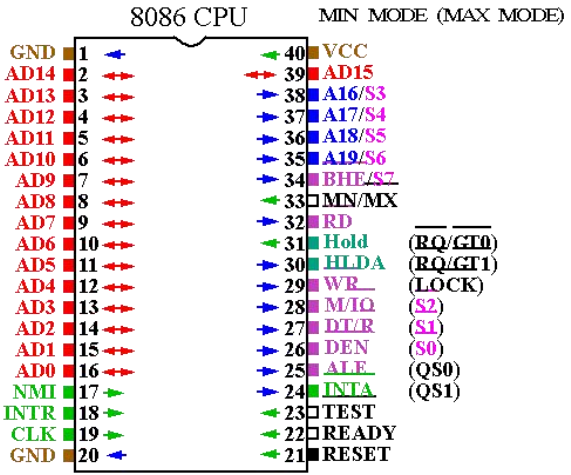
- Supply voltage

GND (Pin no. 1 & 20)

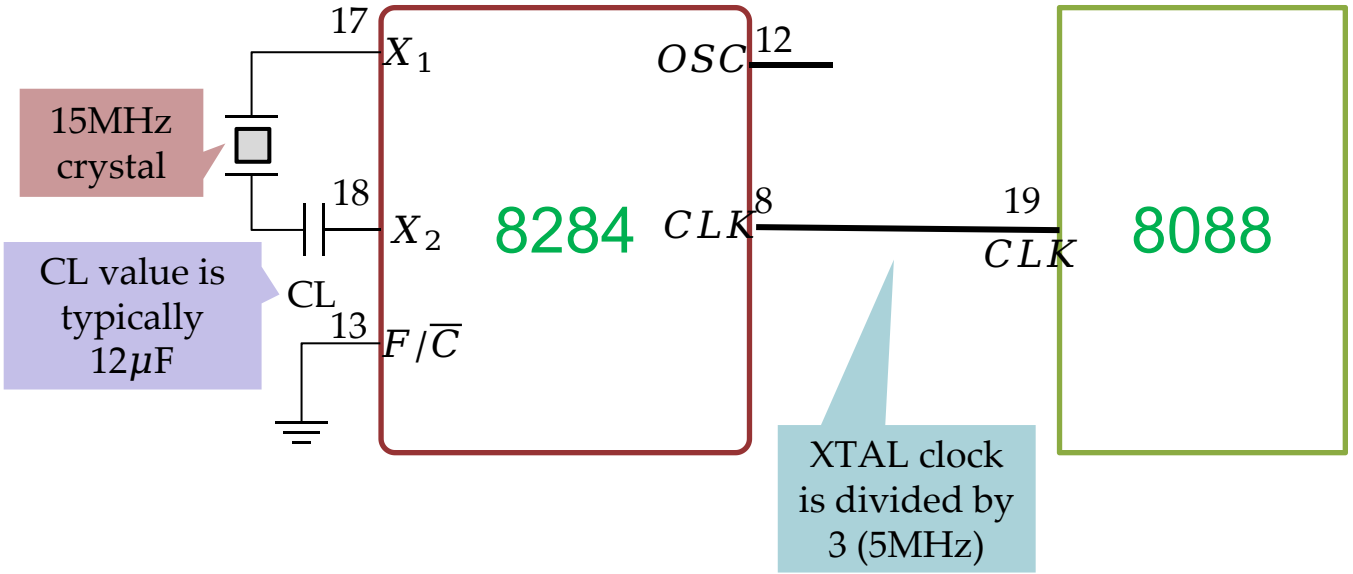
- Common Ground

MN/MAX (pin 33)

- Select either minimum mode or maximum mode



Pinout of 8086



- 8088 operates at 5MHz to 8MHz
- 8086 operates at 5MHz to 10MHz

[5]

Fanout

- **Fanout:** Maximum number of digital inputs that a single logic gate can feed.
- Most TTL gates have fan-out of 10.
- In-order to extend number of connection beyond fan-out range, buffers are used.

[6]

Fanout of TTL standard

- A TTL signal must meet output & input voltage and current specifications.
- OH = Output High
- IL = Input Low
- Fanout = 10

Output characteristics		Input characteristics	
V_{OL}	0.4 V max	V_{IL}	0.8V max
V_{OH}	2.4 V min	V_{IH}	2.0 V min
I_{OL}	16 mA max	I_{IL}	1.6 mA max
I_{OH}	400 μA max	I_{IH}	40 μA max

$$DC\ Fan-out = \min\left(\left[\frac{I_{out\ high}}{I_{in\ high}}\right], \left[\frac{I_{out\ low}}{I_{in\ low}}\right]\right)$$

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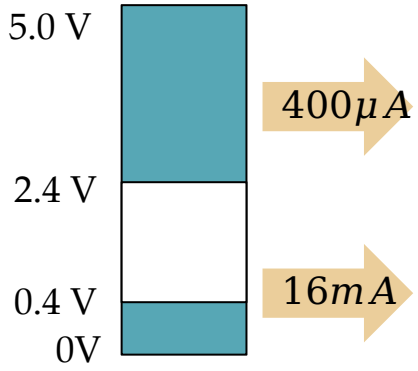

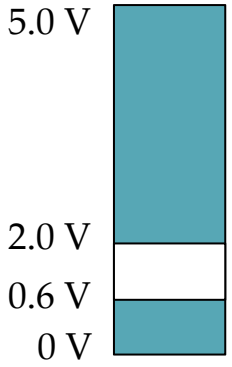

[8]

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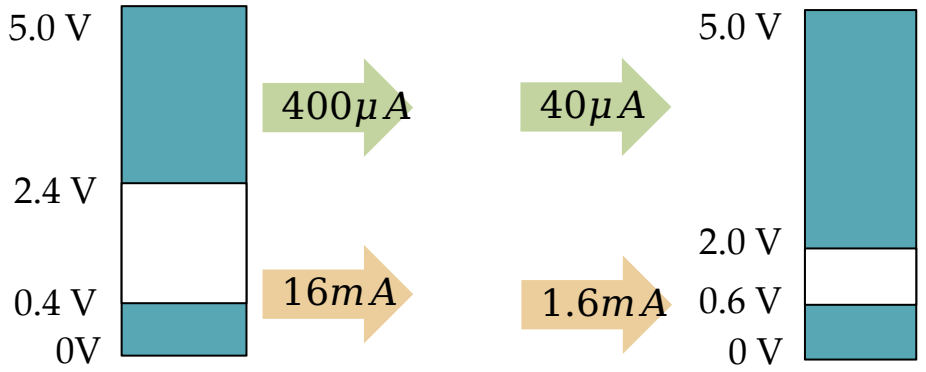
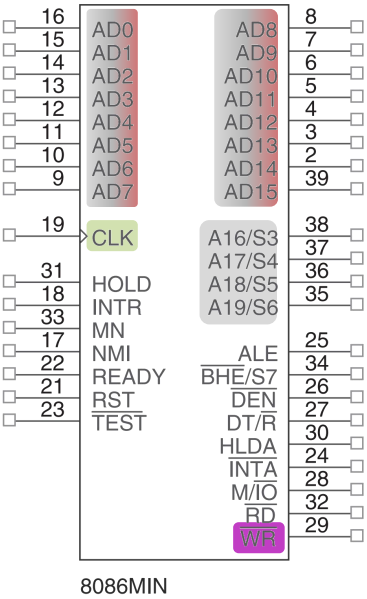
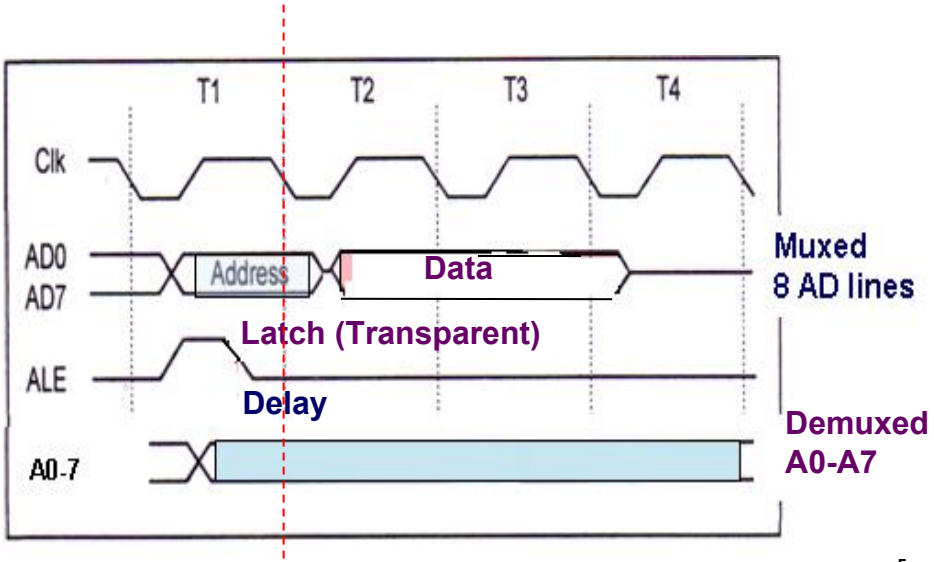


[9]

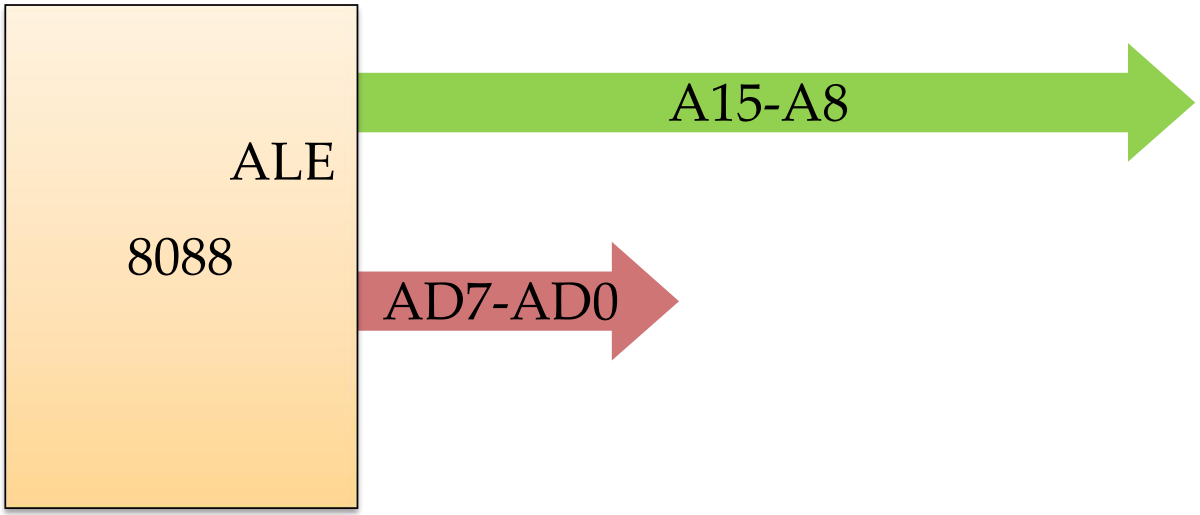
Bus Buffering And Latching



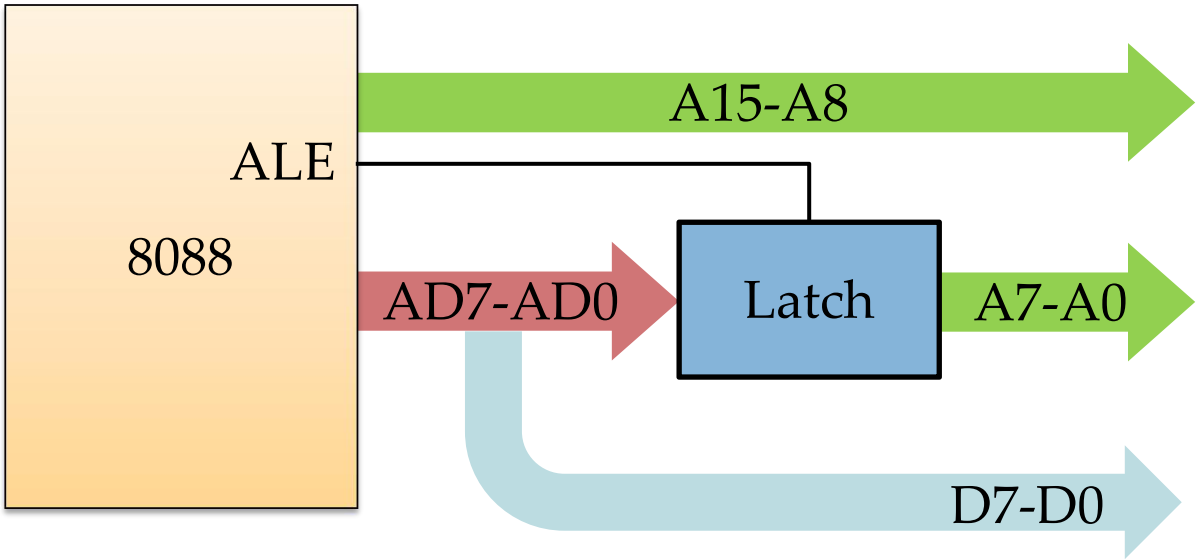


[10]

Bus Buffering And Latching



Bus Buffering And Latching



Bus Buffering And Latching

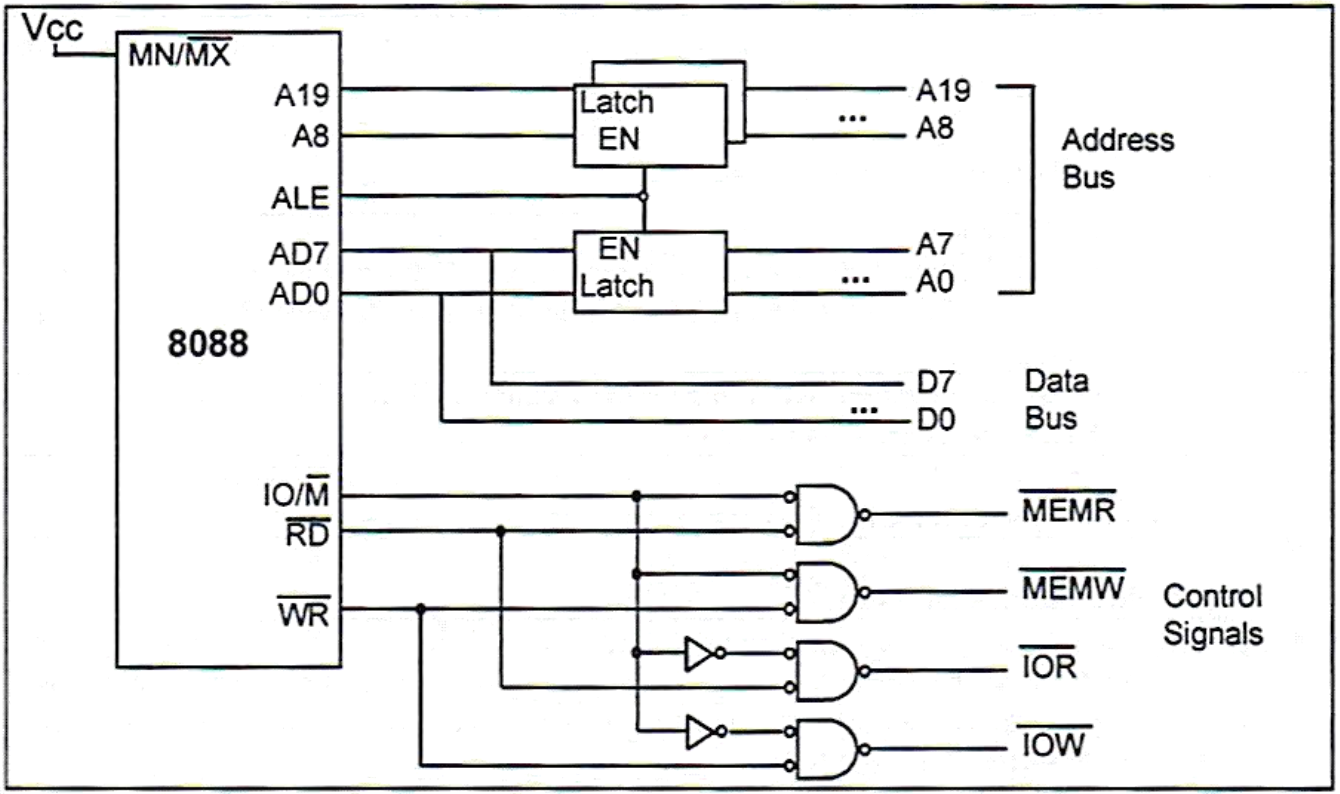


Figure 9-5. Address, Data, and Control Buses in 8088-based System

[13]

Bus Buffering And Latching

- Before the 8086/8088 microprocessors can be used with memory or I/O interfaces, their multiplexed buses must be demultiplexed.

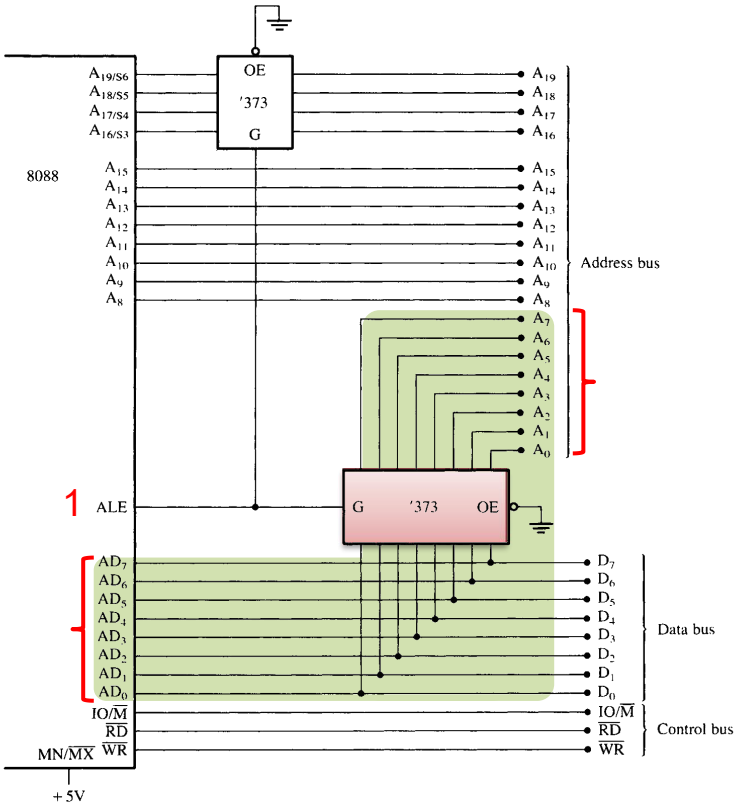


FIGURE 9–5 The 8088 microprocessor shown with a demultiplexed address bus. This is the model used to build many 8088-based systems.

[14]

Bus Buffering And Latching

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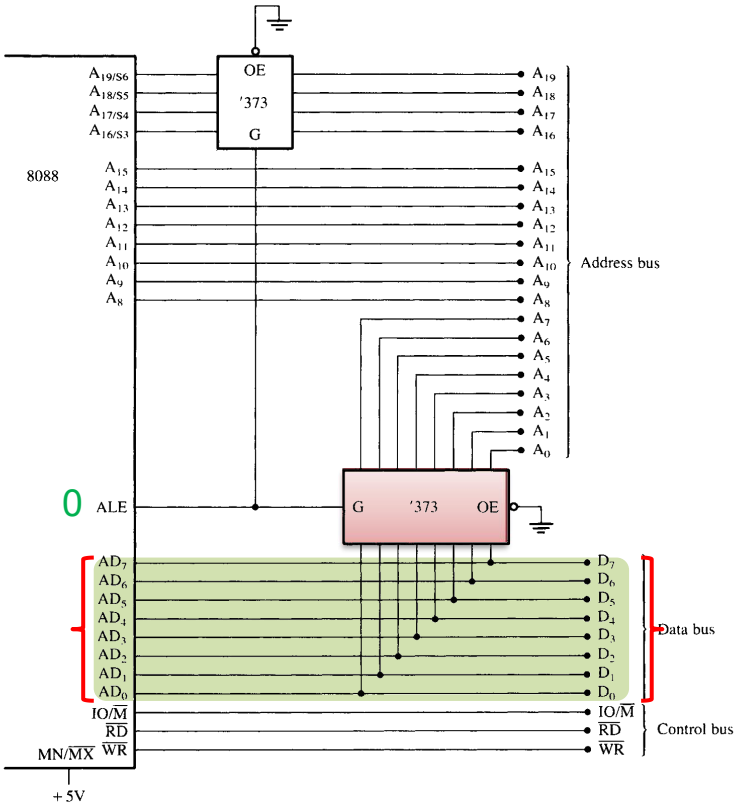
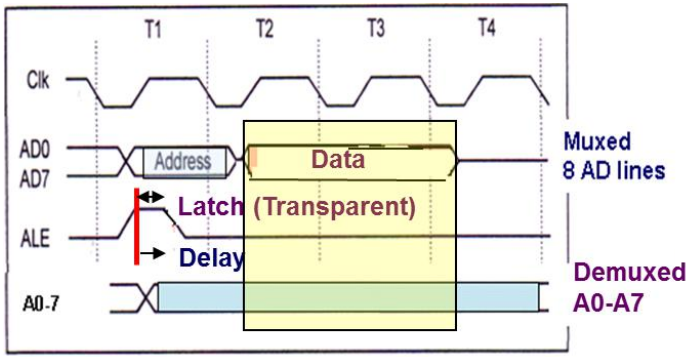


FIGURE 9–5 The 8088 microprocessor shown with a demultiplexed address bus. This is the model used to build many 8088-based systems.

[15]

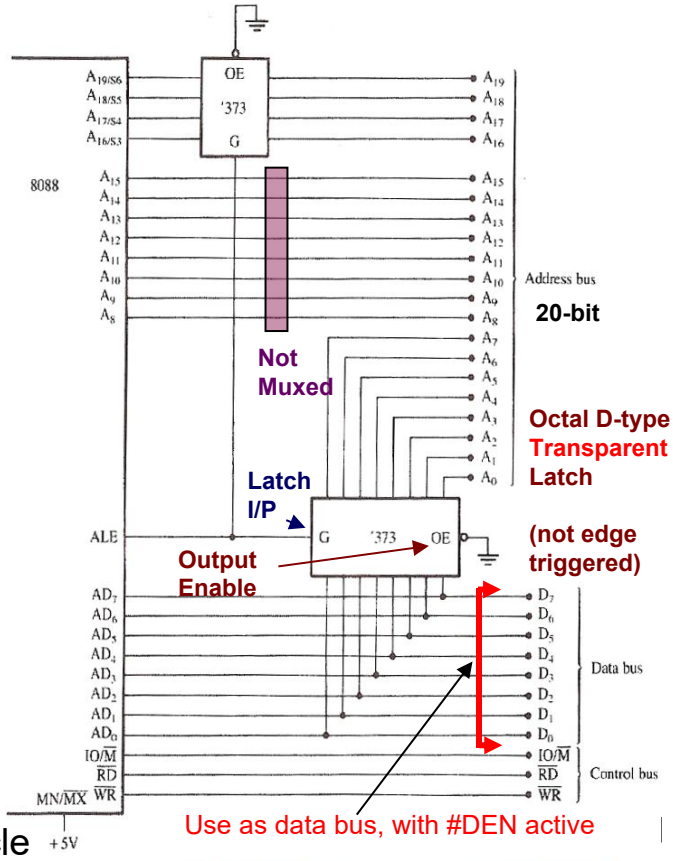
Bus Buffering And Latching

Using the ALE signal to Demultiplex:
-The Address lines A0-7
from the AD0-7 muxed bus
-The A16-19 lines from the
A16/S3-A19/S6 muxed bus

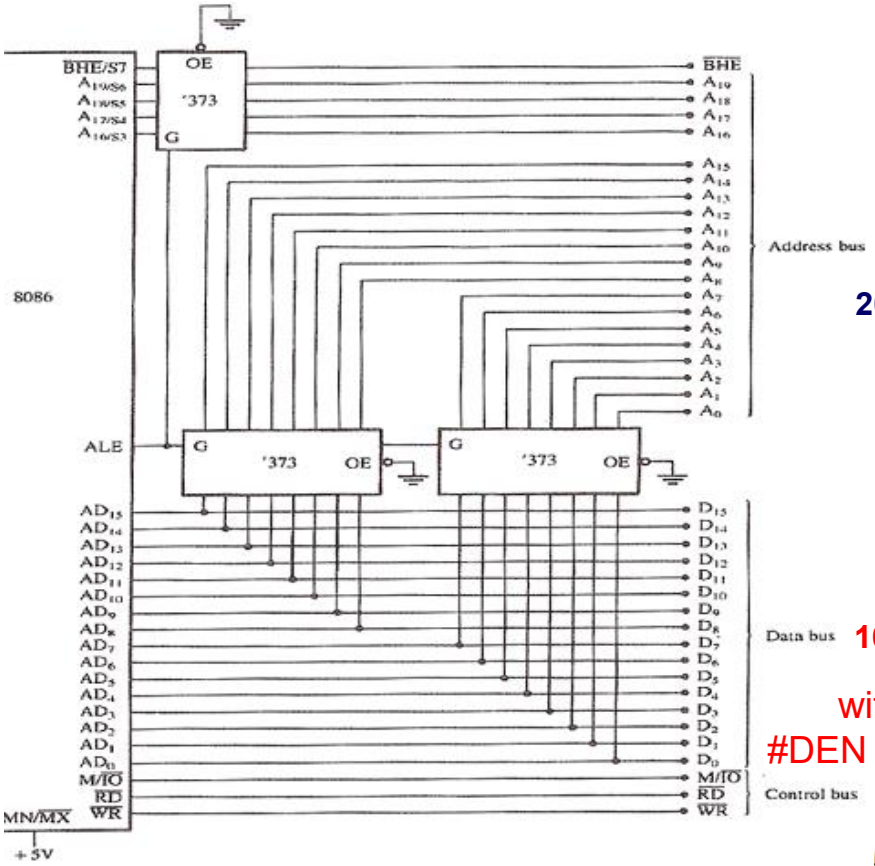


Memory write cycle for the 8088
(non-muxed line are not shown)

Data and address lines must remain
valid and stable for the duration of the cycle



De-multiplexing 8086 data/address bus



20-bit

16-bit

with
#DEN active

[17]

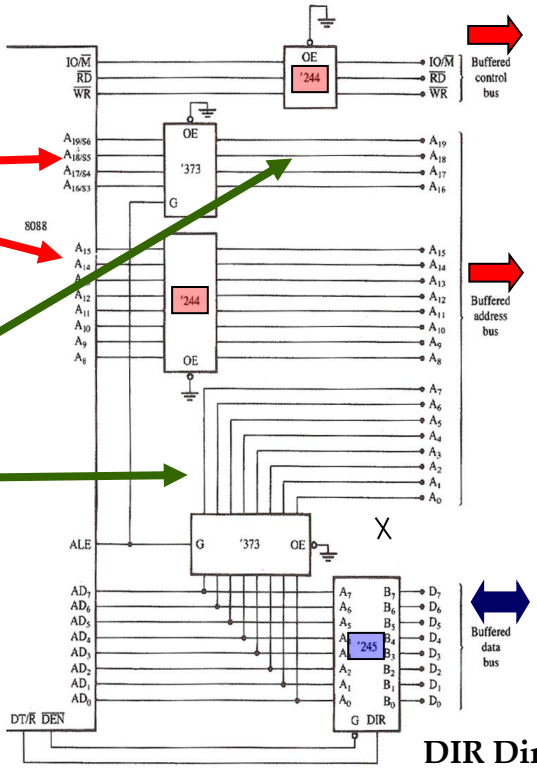
Fully DeMuxed & buffered 8088

74244 is an Octal Buffer with 3-state outputs

Non-DeMuxed Address Lines (unidirectional-Always O/Ps)
→ 244 Buffer

DeMuxed Address Lines (unidirectional-Always O/Ps)
→Latch provides the buffering

Non-Demuxed Bidirectional Data Lines
→ 245 Buffer

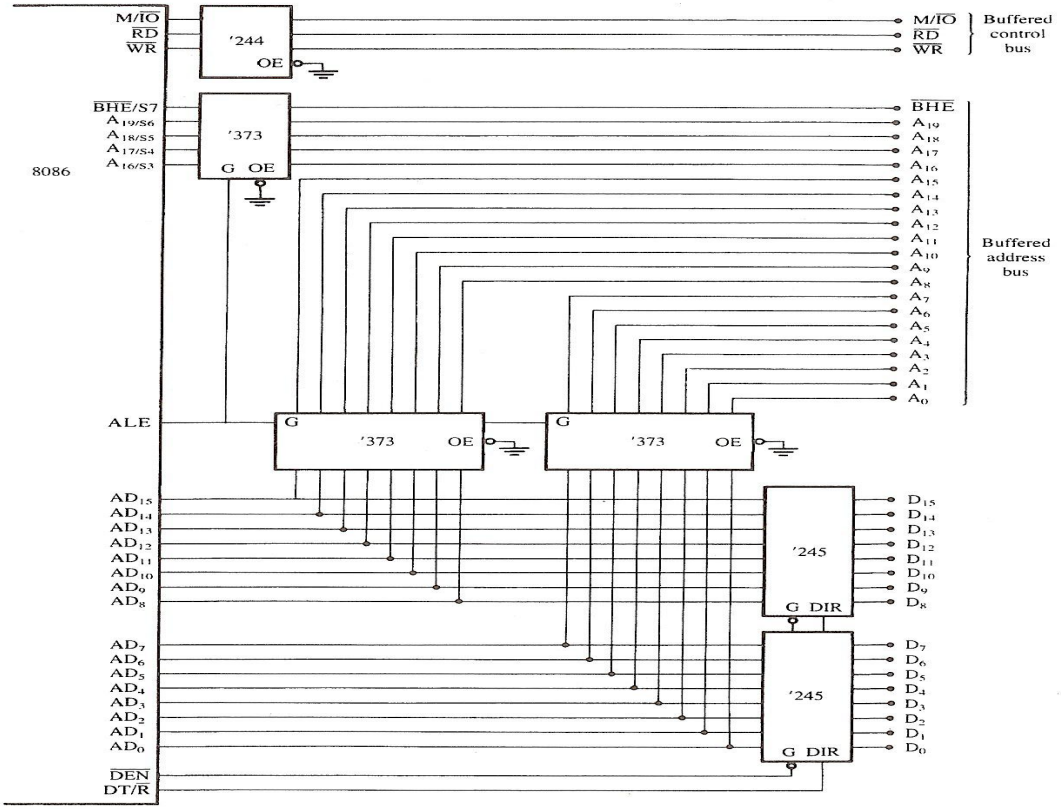


74245 is an Octal Bus Transceiver with 3-state outputs

Enable external buffers

DIR Direction
1: A→B
0: A←B

Fully DeMuxed & buffered 8086



[19]

Book reference

- Intel microprocessor by Barry B. Brey.
- Chapter 9

Questions?

THANK YOU!