Virtex-4™ FX12 LC Development Board
User's Guide

Version 1.1
May 2006

Memec

Table of Contents

Figures

1 Overview

The Memec Virtex-4™ FX12 LC Development Kit provides a complete development platform for designing and verifying applications based on the Xilinx Virtex-4 FPGA family. This kit enables designers to implement DSP and embedded processor based applications with extreme flexibility using IP cores and customized modules. The Virtex-4 FPGA along with its integrated PowerPC processor core makes it possible to prototype processor based applications, enabling software design teams early access to a hardware platform prior to working with the final product/target board.

The Virtex-4 FX12 LC system board utilizes the Xilinx XC4VFX12-10FF668C FPGA. The board includes 64MB of DDR SDRAM, 4MB of Flash, USB-RS232 Bridge, a 10/100/1000 Ethernet PHY, 100 MHz clock source, RS-232 port, and additional user support circuitry to develop a complete system. The board also supports the Memec P160 expansion module standard, allowing application specific expansion modules to be easily added.

2 The Virtex-4 FX12 LC System Board

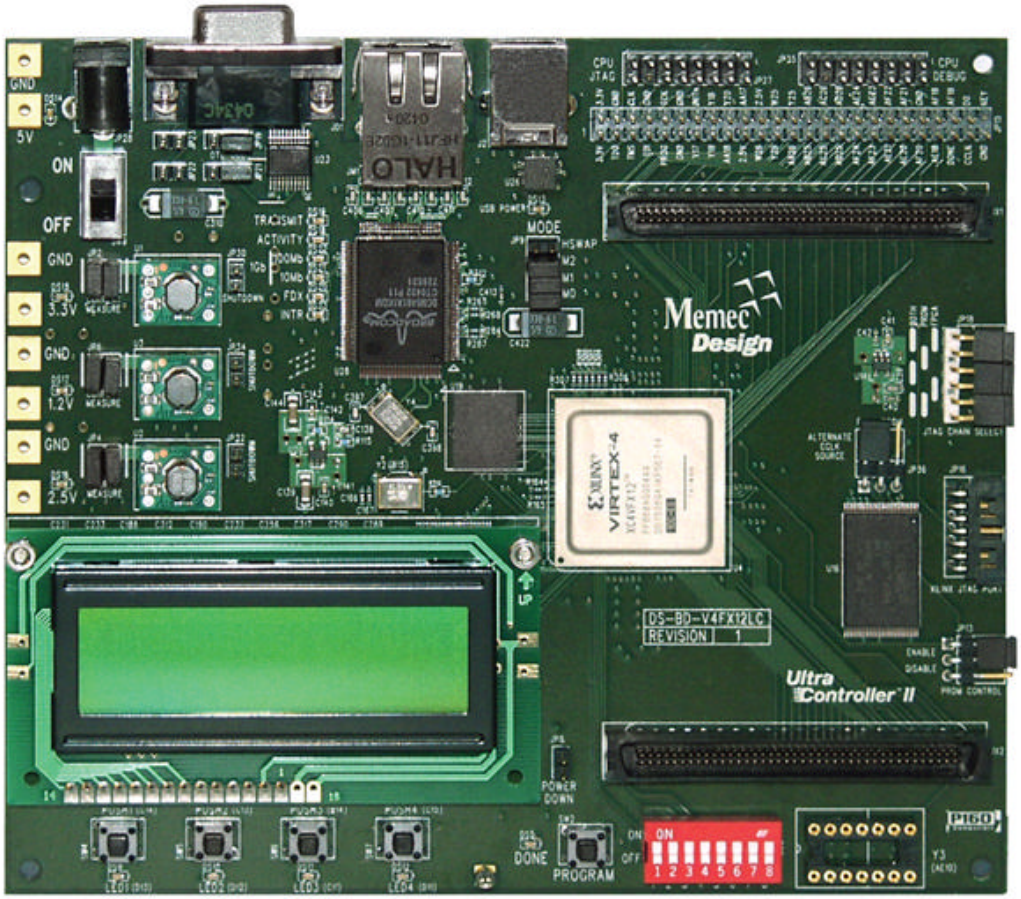


Figure 1 - Virtex-4 FX12 LC Development Board

3 Functional Description

A high-level block diagram of the Virtex-4™ FX12 LC development platform is shown below followed by a brief description of each sub-section. A list of features for this board is shown below:

- Xilinx XC4VFX12-10FF668 FPGA
- 64MB of DDR SDRAM
- 4MB of Flash
- 10/100/1000 Ethernet PHY
- On-board 100MHz LVTTL Oscillator
- On-board LVTTL Oscillator Socket (4/8-Pin Oscillators)
- P160 Connectors
- LCD Panel
- Platform Flash configuration PROM
- PC4 JTAG Programming/Configuration Port
- SystemACE™ Module Connector
- CPU JTAG Port
- CPU Debug Port
- RS232 Port
- Four User LEDs
- Four User Push Button Switches
- An 8-position DIP Switch
- USB-RS232 Bridge

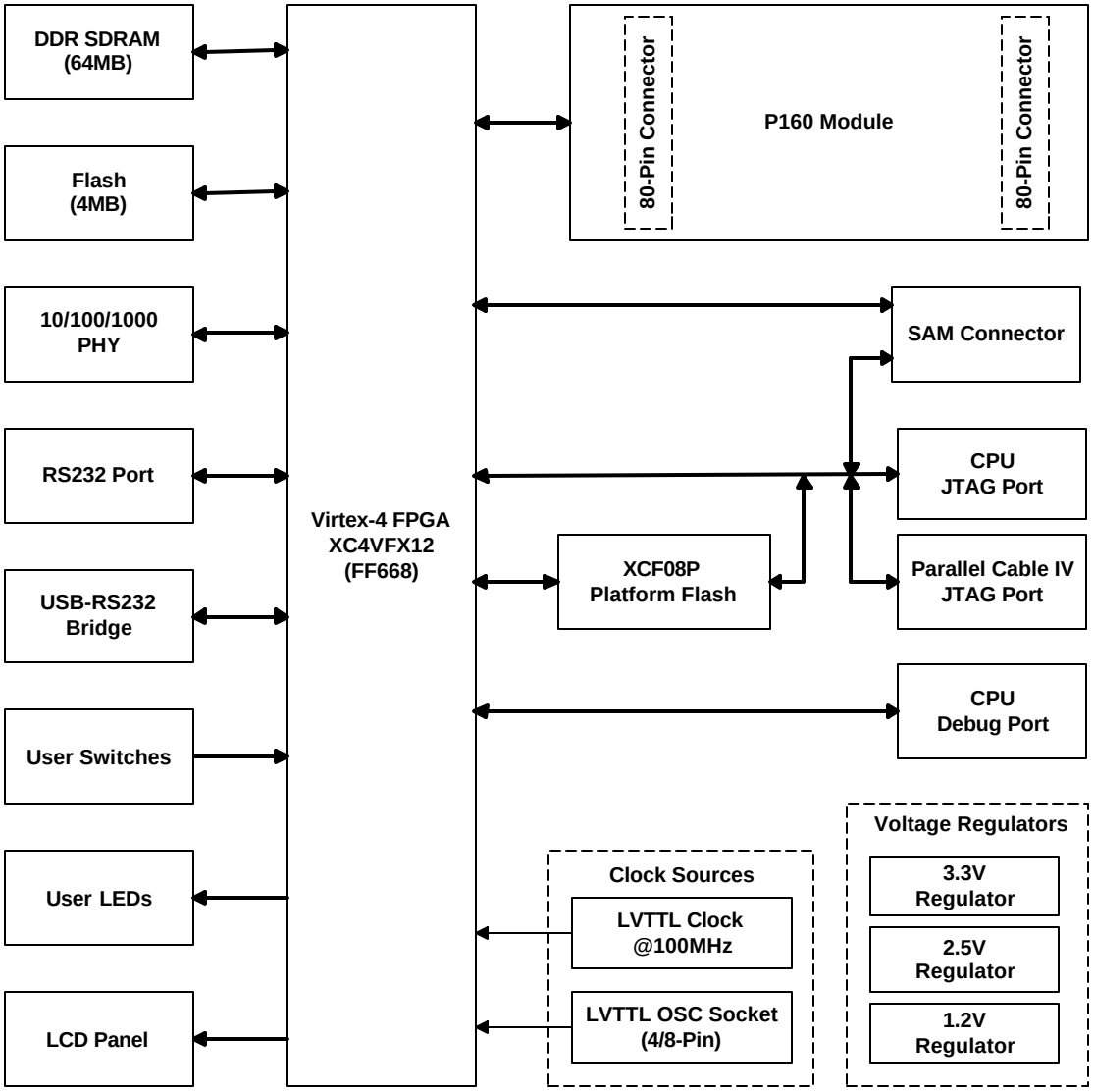


Figure 2 - Virtex-4 FX12 LC Development Platform Block Diagram

3.1 DDR SDRAM

The Virtex-4™ FX12 LC development board provides 64MB of DDR SDRAM memory (x16). A high-level block diagram of the DDR SDRAM interface is shown below followed by a table describing the SDRAM memory interface signals.

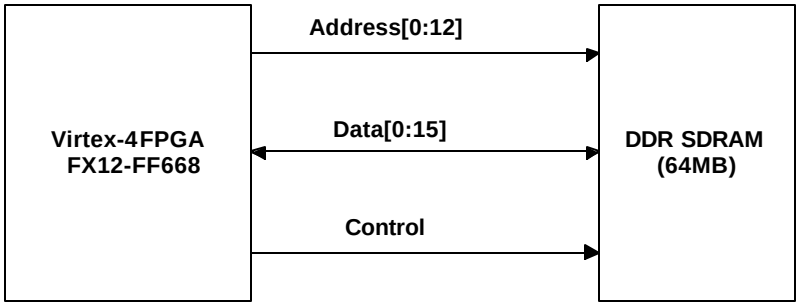


Figure 3 – DDR SDRAM Interface

Table 1 – DDR SDRAM Interface Pin Assignments

Signal Name	Description	FPGA Pin #
ddr_addr[0]	Address 0	D20
ddr_addr[1]	Address 1	B18
ddr_addr[2]	Address 2	E18
ddr_addr[3]	Address 3	D17
ddr_addr[4]	Address 4	C17
ddr_addr[5]	Address 5	A18
ddr_addr[6]	Address 6	D18
ddr_addr[7]	Address 7	A19
ddr_addr[8]	Address 8	C19
ddr_addr[9]	Address 9	B20
ddr_addr[10]	Address 10	A20
ddr_addr[11]	Address 11	C20
ddr_addr[12]	Address 12	A23
ddr_dq[0]	Data 0	H22
ddr_dq[1]	Data 1	H21
ddr_dq[2]	Data 2	F23
ddr_dq[3]	Data 3	H20
ddr_dq[4]	Data 4	F20
ddr_dq[5]	Data 5	G20
ddr_dq[6]	Data 6	F19
ddr_dq[7]	Data 7	G19
ddr_dq[8]	Data 8	C23
ddr_dq[9]	Data 9	F17
ddr_dq[10]	Data 10	D23
ddr_dq[11]	Data 11	F18
ddr_dq[12]	Data 12	C24
ddr_dq[13]	Data 13	H23
ddr_dq[14]	Data 14	E23
ddr_dq[15]	Data 15	E22
ddr_ba[0]	Bank Select 0	A21
ddr_ba[1]	Bank Select 1	E20
ddr_dm[0]	Write Mask0	E17
ddr_dm[1]	Write Mask1	A24
ddr_dqs[0]	Data Strobe0	G18

ddr_dqs[1]	Data Strobe1	G17
ddr_csn	Chip Select	A22
ddr_rasn	Row Address Strobe	C21
ddr_casn	Column Address Strobe	B23
ddr_wen	Write Enable	E21
ddr_clk	Clock	D22
ddr_clkn	Clock	C22
ddr_clke	Clock Enable	B21

3.2 Flash

The Virtex-4™ FX12 LC development board provides 4MB of flash memory (x16). A high-level block diagram of the flash interface is shown below followed by a table describing the flash memory interface signals.

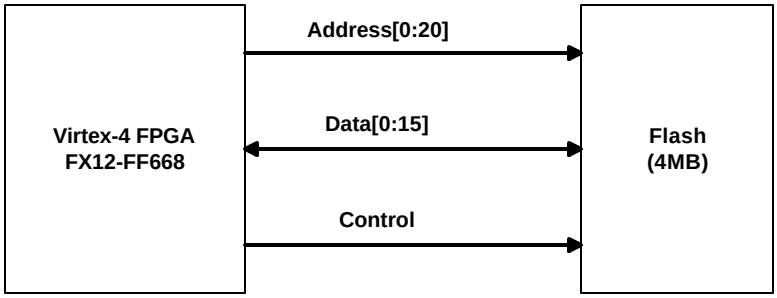


Figure 4 – Flash Interface

Table 2 – Flash Interface Pin Assignments

Signal Name	Description	FPGA Pin #
flash_addr[0]	Address 0	B4
flash_addr[1]	Address 1	A4
flash_addr[2]	Address 2	A5
flash_addr[3]	Address 3	B6
flash_addr[4]	Address 4	A6
flash_addr[5]	Address 5	B7
flash_addr[6]	Address 6	A7
flash_addr[7]	Address 7	D7
flash_addr[8]	Address 8	E7
flash_addr[9]	Address 9	F8
flash_addr[10]	Address 10	E9
flash_addr[11]	Address 11	E10
flash_addr[12]	Address 12	F7
flash_addr[13]	Address 13	G8
flash_addr[14]	Address 14	F9
flash_addr[15]	Address 15	F10
flash_addr[16]	Address 16	G10
flash_addr[17]	Address 17	C7
flash_addr[18]	Address 18	D8
flash_addr[19]	Address 19	E5
flash_addr[20]	Address 20	E6

flash_d[0]	Data 0	C2
flash_d[1]	Data 1	D2
flash_d[2]	Data 2	D6
flash_d[3]	Data 3	D5
flash_d[4]	Data 4	D4
flash_d[5]	Data 5	G6
flash_d[6]	Data 6	H7
flash_d[7]	Data 7	G7
flash_d[8]	Data 8	C1
flash_d[9]	Data 9	C6
flash_d[10]	Data 10	C5
flash_d[11]	Data 11	C4
flash_d[12]	Data 12	G5
flash_d[13]	Data 13	H6
flash_d[14]	Data 14	H8
flash_d[15]	Data 15	G9
flash_cen	Chip Select	A3
flash_oen	Output Enable	B3
flash_wen	Write Enable	C10
flash_rdy	Ready	C8
flash_reset	Reset	D10
flash_vpp	Fast Programming	D9

3.3 Clock Sources

The Clock Generation section of the Virtex-4 FX12 LC board provides all the necessary clocks for the PowerPC processor, the I/O devices located on the board, as well as the DDR SDRAM memory.

An on-board 100MHz oscillator provides the system clock input to the processor section. This 100Mhz clock will be used by the Virtex-4 Digital Clock Managers (DCMs) to generate various processor clocks. In addition to the above clock inputs, a socket is provided on the board that can be used to provide single ended LVTTL clock input to the FPGA via an 8 or 4-pin oscillator. The following figure shows the clock resources on the Virtex-4 FX12 LC development board.

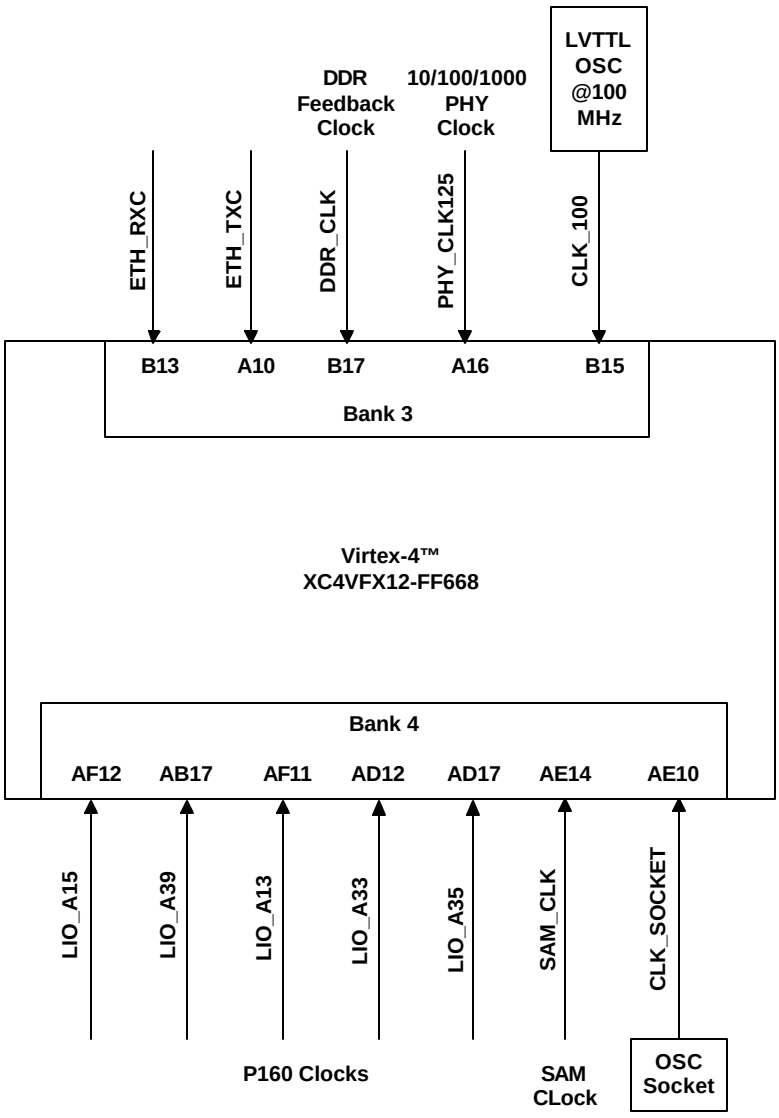


Figure 5 - Clock Sources on the Virtex-4 FX12 LC Board

The following table provides a brief description of each clock input to the Virtex-4 FPGA.

Table 3 - Clock Inputs

Signal Name	FPGA Pin #	Description
LIO_A15, LIO_A39, LIO_A13, LIO_A33, LIO_A35	AF12, AB17, AF11, AD12, AD17	***P160 Module Single-ended Clock Inputs***– These clock inputs are connected to the P160 connector located on the Virtex-4 FX12 LC board.
DDR_CLK	B17	***DDR Feedback Clock Input*** – This clock input is connected to the DDR clock.

CLK_100	B15	***System Clock*** – This clock input is connected to a 100MHz LVTTL oscillator.
CLK_SOCKET	AE10	***LVTTL Clock Input*** – LVTTL socket on the Virtex-4 board.
PHY_CLK125	A16	***10/100/1000 PHY Clock*** – This clock input is connected to the 125MHz clock output of the 10/100/1000 PHY.
ETH_RXC	B13	***Ethernet Receive Clock Input*** – This clock input is connected to the Ethernet receive clock.
ETH_TXC	A10	***Ethernet Transmit Clock Input*** – This clock input is connected to the Ethernet transmit clock.
SAM_CLK	AE14	***SystemACE Module Clock Input*** – This clock input is connected to the SystemACE Module connector.

3.4 10/100/1000 Ethernet PHY

The Virtex-4 FX12 LC development board provides a 10/100/1000 Ethernet port for network connection. This interface uses the Virtex-4 embedded 10/100/1000 MAC. A high-level block diagram of the 10/100/1000 Ethernet interface is shown in the following figure followed by FPGA pin assignments for this interface.

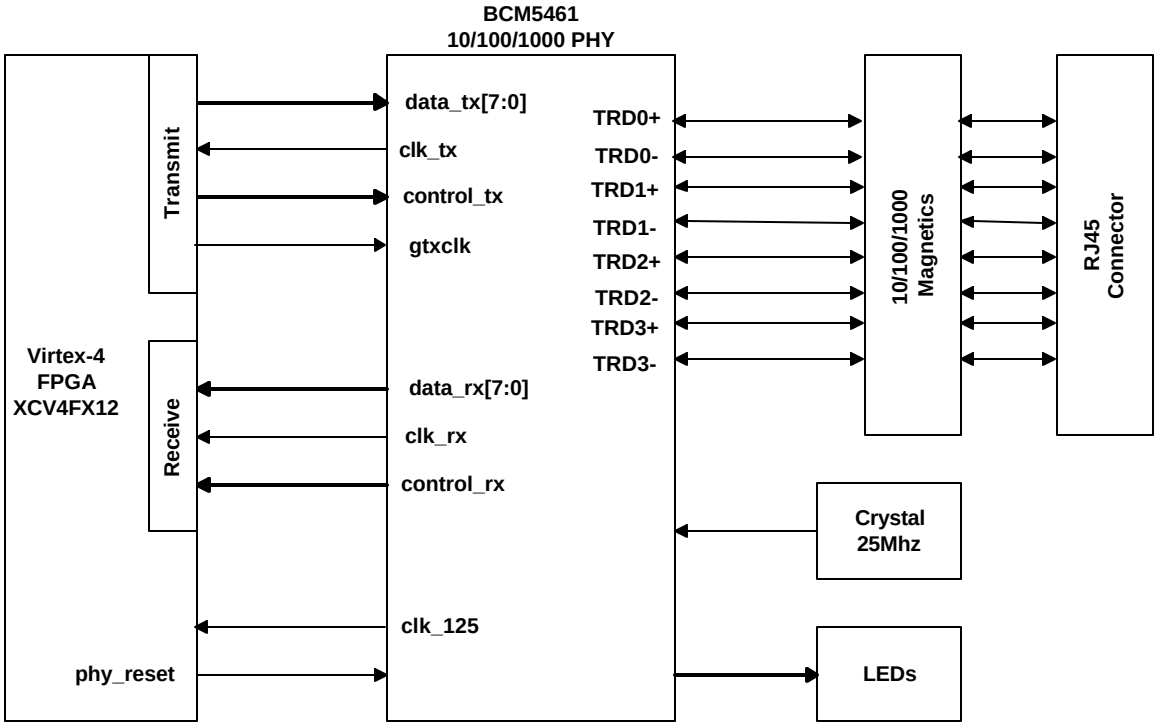


Figure 6 – 10/100/1000 Ethernet Interface

The following table shows the FPGA pin assignments for the Ethernet interface.

Table 4 – Ethernet Pin Assignments

Signal Name	Virtex-4 Pin #
PHY_RESETn	E25
PHY_RXC	B13
PHY_MDC	G25
PHY_COL	B24
PHY_CRS	D25
PHY_TXD0	H26
PHY_TXD1	H24
PHY_TXD2	G26
PHY_TXD3	G24
PHY_TXD4	F26
PHY_TXD5	F24
PHY_TXD6	E26
PHY_TXD7	E24
PHY_TXEN	D26
PHY_TXC	A10
PHY_TXER	D24
PHY_RXD0	D16
PHY_RXD1	C16
PHY_RXD2	D15
PHY_RXD3	D14
PHY_RXD4	E14
PHY_RXD5	F14
PHY_RXD6	F11
PHY_RXD7	F12
PHY_RXDV	F13
PHY_MDIO	H25
PHY_RXER	E13
PHY_GTXCLK	C26
PHY_CLK125	A16

3.5 LCD Panel

The Virtex-4 FX12 LC development board provides an 8-bit interface to a 2x16 LCD panel (MYTECH MOC-16216B-B). The following table shows the LCD interface signals.

Table 5 – LCD Interface Signals

Signal Name	Description	Virtex-4 Pin #
D0	LCD Data Bit 0	H3
D1	LCD Data Bit 1	G4
D2	LCD Data Bit 2	G3
D3	LCD Data Bit 4	F3
D4	LCD Data Bit 4	F4
D5	LCD Data Bit 5	E3
D6	LCD Data Bit 6	E4
D7	LCD Data Bit 7	D3
EN	LCD Enable Signal	H4
RW	LCD Write Signal (this signal is connected to logic “0” on the Virtex-4 FX12 board, enabling write only cycles).	N/A
RS	LCD Register Select Signal	H5

3.6 USB 2.0 to RS232 Port

The Virtex-4 FX12 LC development board implements a USB 2.0 port. This is accomplished using the Cygnal CP2101 USB-to-UART Bridge Controller. The FPGA interfaces to the CP2102 as a simple UART. The UART interface to the CP2102 can run at speeds ranging from 300 to 921,600 baud.

The CP2102 is a highly integrated USB-to-UART Bridge Controller, providing a simple solution for USB serial communications using a minimum of components and PCB space. The CP2102 includes a USB 2.0 full-speed function controller, USB transceiver, oscillator, EEPROM, and asynchronous serial data bus (UART) with full modem control signals in a compact 5mm X 5mm MLP-28 package. No other external USB components are required.

The on-chip EEPROM may be used to customize the USB Vendor ID, Product ID, Product Description String, Power Descriptor, Device Release Number, and Device Serial Number as desired. The EEPROM is programmed on-board via the USB allowing the programming step to be easily integrated into the product manufacturing and testing process.

Royalty-free Virtual COM Port (VCP) device drivers provided by Cygnal allow the Virtex-4 FX12 LC development board to appear as a COM port to PC applications. The CP2102 UART interface implements all RS232 signals, including control and handshaking signals. These signals are interfaced to the Virtex-4 FPGA as follows:

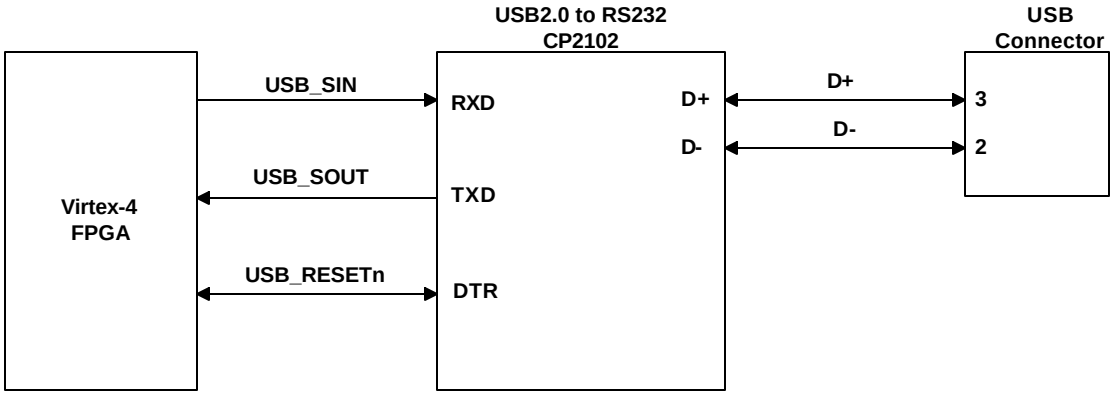


Figure 7 – USB 2.0 to RS232 Serial Interface

The following table shows the RS232 interface signal names and their Virtex-4 FPGA pin assignments.

Table 6- USB 2.0 to RS232 Port Signal Description

FPGA Signal Name	Virtex-4 Pin #	Description
RS232 Signals		
USB_SIN	A8	RS232 receive signal
USB_SOUT	D1	RS232 transmit signal
USB 2.0 Signals		
D+	NA	USB D+ signal
D-	NA	USB D- signal
Common Signal		

USB_RESETn	E2	CP2102 reset signal

To use the USB port, the CP2102 device drivers must be installed. These drivers are included on the Virtex-4 FX12 LC Development Kit CD and contained in the self-extracting file **CP2101.exe**. To install the CP2101/2 virtual COM port device drivers, refer to Appendix A.

3.7 RS232

The Virtex-4 FX12 LC development board provides an RS232 interface with RX and TX signals and jumpers for connecting the RTS and CTS signals. The following figure shows the RS232 interface to the Virtex-4 FX12 FPGA.

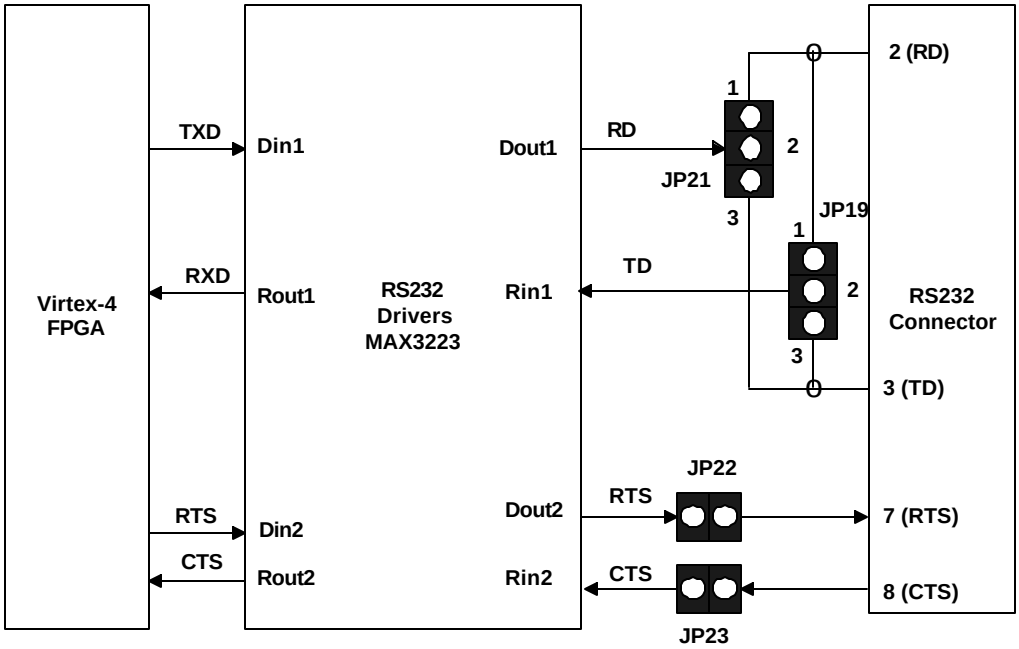


Figure 8 - RS232 Interface

Table 7 – RS232 Signals

Signal Name	Description	Virtex-4 Pin #
RS232_RXD	Received Data, RD	F1
RS232_TXD	Transmit Data, TD	A9
RS232_RTS	Request To Send, RTS	B9
RS232_CTS	Clear To Send, CTS	E1

Table 8 - RS232 Jumper Settings

Mode of Operation	JP19	JP21
DCE	Install a jumper on pins 2-3	Install a jumper on pins 1-2
DTE	Install a jumper on pins 1-2	Install a jumper on pins 2-3

Jumpers must be installed on JP22 and JP23 if RTS and CTS signal connections are needed.

3.8 User DIP and PB Switches

The Virtex-4 FX12 LC development board provides four user push button switches as described in the following table. An active low signal is generated when a given switch is pressed.

Table 9 – Push Button Switch Pin Assignments

Signal Name	Description	Virtex-4 Pin #
PUSH1	SW5	C14
PUSH2	SW6	C13
PUSH3	SW7	B14
PUSH4	SW8	C15

The Virtex-4 FX12 LC development board provides an 8-position DIP switch as described in the following table. An active low signal is generated when a given switch is ON.

Table 10 – DIP Switch Pin Assignments

Signal Name	Description	Virtex-4 Pin #
DIP1	User Switch Input 1	G2
DIP2	User Switch Input 2	G1
DIP3	User Switch Input 3	H2
DIP4	User Switch Input 4	H1
DIP5	User Switch Input 5	Y10
DIP6	User Switch Input 6	Y9
DIP7	User Switch Input 7	Y7
DIP8	User Switch Input 8	Y8

3.9 User LEDs

The Virtex-4 FX12 LC development board provides four user LEDs that can be turned “ON” by driving the LEDx signal to logic “0”. The following table shows the user LEDs and their associated Virtex-4 FPGA pin assignments.

Table 11 – LED Pin Assignments

LED Designation	LED #	Virtex-4 Pin #
DS9	LED1	D13
DS10	LED2	D12
DS11	LED3	C11
DS12	LED4	D11

3.10 Configuration and Debug Ports

Various methods of configuration and debug support are provided on the Virtex-4 FX12 development board to assist designers during the testing and debugging of their applications. The following sections provide brief descriptions of each of these interfaces.

3.10.1 JTAG Chain

The following figure shows the JTAG chain on the Virtex-4 FX12 LC development board.

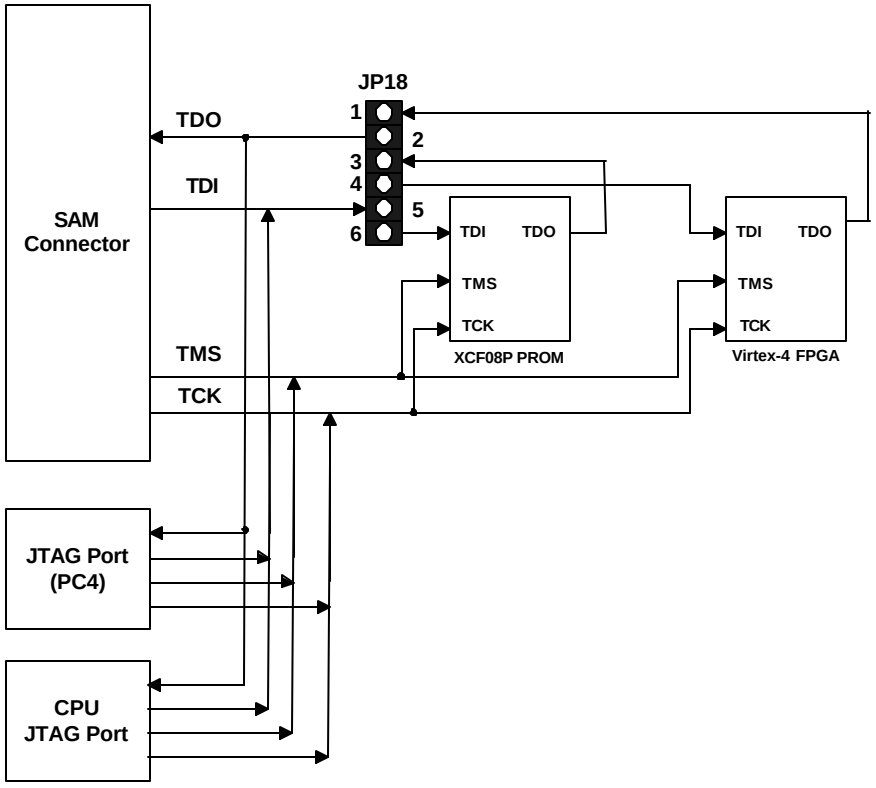


Figure 9 – Vitex-4 FX12 LC Development Board JTAG Chain

3.10.2 System ACE Module Connector

The Virtex-4 FX12 LC development board provides the SAM 50-pin connector on the board for using the Memec System ACE Module (SAM). The SAM can be used to configure the FPGA or to provide bulk flash memory to the PowerPC processor.

The Virtex-4 FX12 LC development board provides a System ACE interface that can be used to configure the Virtex-4 FPGA. The interface also gives software designers the ability to run real-time operating systems (RTOS) from removable CompactFlash cards. The Memec System ACE module (DS-KIT-SYSTEMACE) can be used to perform both of these functions. The figure below shows the System ACE module connected to the header on the Virtex-4 board.

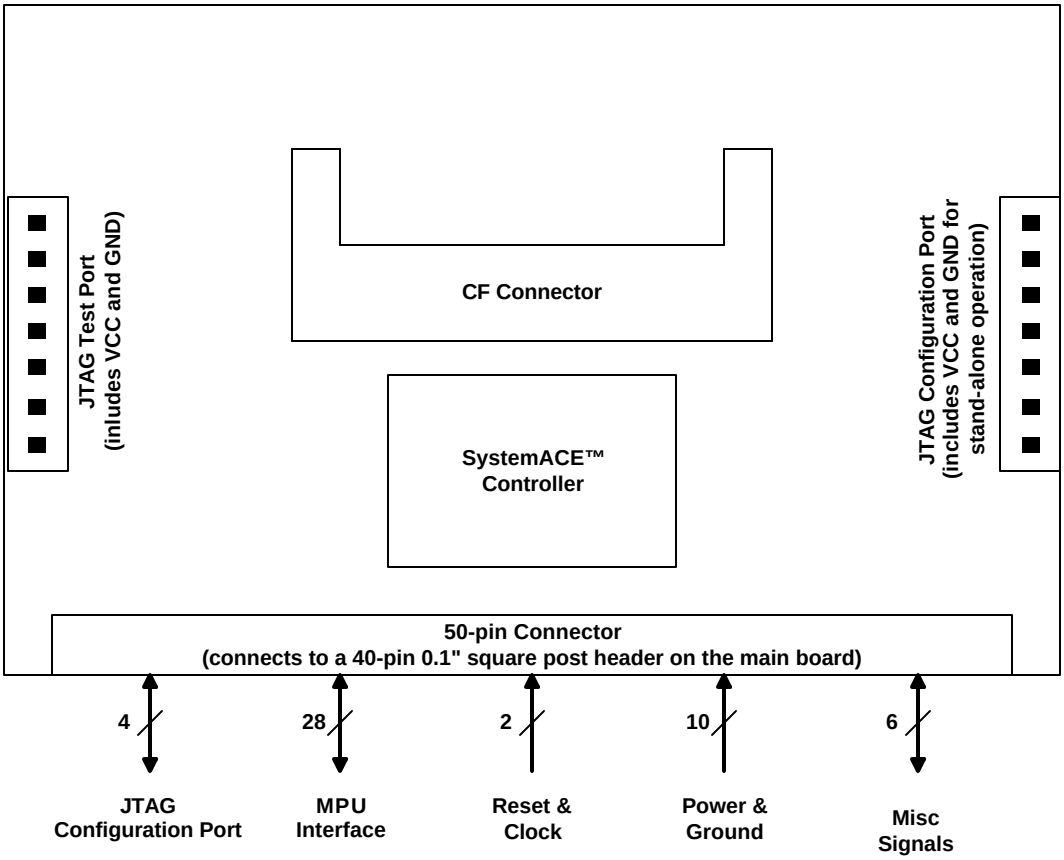


Figure 10 – SystemACE Module

3.10.2.1 System ACE Controller Signal Description

The following table shows the System ACE Module signal assignments to the FPGA I/O pins.

Table 12 - SAM Interface Signals

Virtex-4 Pin #	System ACE Signal Name	SAM Connector Pin # (JP16)		System ACE Signal Name	Virtex-4 Pin #
	3.3V	1	2	**3.3V**	
	TDO	3	4	**GND**	
	TMS	5	6	CLOCK	AE14
	TDI	7	8	**GND**	
	PROGRAMn	9	10	TCK	
	GND	11	12	**GND**	
Y17	OEn	13	14	INITn	
Y19	MPA0	15	16	WEn	Y18
AA18	MPA2	17	18	MPA1	Y20
	2.5V	19	20	MPA3	AA17
W26	MPD00	21	22	**2.5V**	
Y26	MPD02	23	24	MPD01	W25
AA26	MPD04	25	26	MPD03	Y25
AB25	MPD06	27	28	MPD05	AB26
AC25	MPD08	29	30	MPD07	AC26

AD25	MPD10	31	32	MPD09	AD26
AF24	MPD12	33	34	MPD11	AE24
AF23	MPD14	35	36	MPD13	AE23
AE21	MPA4	37	38	MPD15	AF22
AE20	MPA6	39	40	MPA5	AF21
AF20	IRQ	41	42	**GND**	
AE18	RESETn	43	44	CEn	AF19
	DONE	45	46	BRDY	AF18
	CCLK	47	48	BITSTREAM	
	GND	49	50	**NC**	

3.10.3 JTAG Port (PC4)

The Virtex-4 FX12 LC development board provides a JTAG port (PC4 type) connector for configuration of the FPGA. The following figure shows the pin assignments for the PC4 header on this development board.

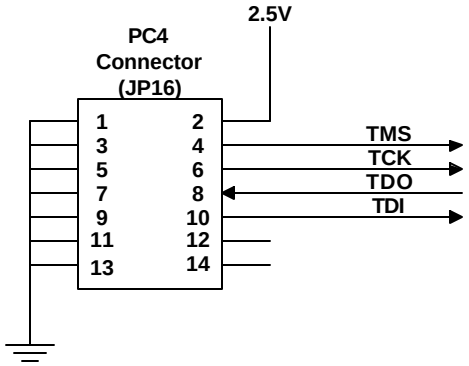


Figure 11 - PC4 JTAG Port Connector

3.10.4 Configuration Modes

The following table shows the Virtex-4 configuration modes.

Table 13 - FPGA Configuration Mode Jumper Settings

Mode	PC Pull-up	Configuration Mode Jumpers			
		1-2 (M2)	3-4 (M1)	5-6 (M0)	7-8 (HSWAP_EN)
Master Serial	Yes	Closed	Closed	Closed	Closed
Master Serial	No	Closed	Closed	Closed	Open
Slave Serial	Yes	Open	Open	Open	Closed
Slave Serial	No	Open	Open	Open	Open
Master SelectMap	Yes	Closed	Open	Open	Closed
Master SelectMap	No	Closed	Open	Open	Open
Slave SelectMap	Yes	Open	Open	Closed	Closed
Slave SelectMap	No	Open	Open	Closed	Open
JTAG	Yes	Open	Closed	Open	Closed
JTAG	No	Open	Closed	Open	Open

3.10.5 CPU JTAG Port

The Virtex-4 FX12 LC development board provides a CPU JTAG connector that can be used to download code into the Virtex-4 integrated PowerPC processor memory. This JTAG port can also

be used as the processor debug port. The following figure shows the pin assignments for the CPU JTAG connector on the board.

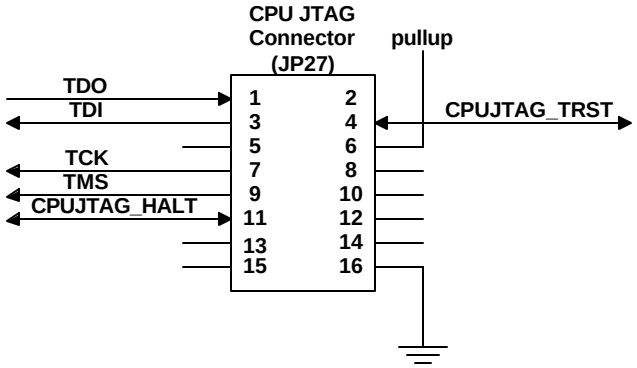


Figure 12 - CPU JTAG Port Connector

Table 14 - CPU JTAG Interface Signals

Signal Name	Virtex-4™ Pin #	Description
TCK		CPU JTAG Clock Input
TDI		CPU JTAG Data Input
TMS		CPU JTAG TMS Input
TDO		CPU JTAG Data Output
CPUJTAG_TRST	AA16	CPU JTAG Reset Input
CPUJTAG_HALT	AC16	CPU HALT Input

3.10.6 CPU Debug Port

The Virtex-4 FX12 LC development board provides a CPU Debug header for connection of a debug probe (such as the Wind River visionProbe-II™) to the PowerPC processor.

The Virtex-4 FX12 LC development board provides a dedicated CPU Debug connector that can be used to download code into the Virtex-4 integrated PowerPC processor memory. This JTAG port can also be used as the processor debug port. The figure below shows the pin assignments for the CPU Debug connector. The FPGA general-purpose I/O pins are used for this interface.

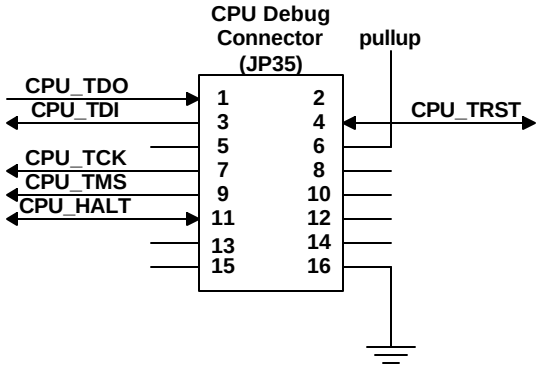


Figure 13 - CPU Debug Port Connector

Table 15 – CPU Debug Interface Signals

Signal Name	Virtex-4™ Pin #	Description
CPU_TCK	AD14	CPU Debug Clock Input
CPU_TDI	AC14	CPU Debug Data Input
CPU_TMS	AA15	CPU Debug TMS Input
CPU_TDO	AA14	CPU Debug Data Output
CPU_TRST	AB14	CPU Debug Reset Input
CPU_HALT	AC15	CPU HALT Input

3.10.7 The JP36 Jumper

The JP36 jumper allows the Platform Flash CCLK clock input to be driven after the FPGA configuration. If a jumper is installed on pins 1-2, an FPGA I/O pins is used to drive the CCLK signal. If a jumper is installed on pins 2-3, CLKOUT of the Platform Flash is used to drive the CCLK input after the FPGA configuration. The JP36 jumper allows the Platform Flash unused space to be used for user data after the FPGA configuration.

3.11 Voltage Regulators

The following figure shows the voltage regulators that are used on Virtex-4 FX12 LC development board to provide various on-board voltage sources. As shown in the following figure, a connector is used to provide the main 5.0V voltage to the board. This voltage source is provided to all on-board regulators to generate the 1.2V, 2.5V, and 3.3V voltages.

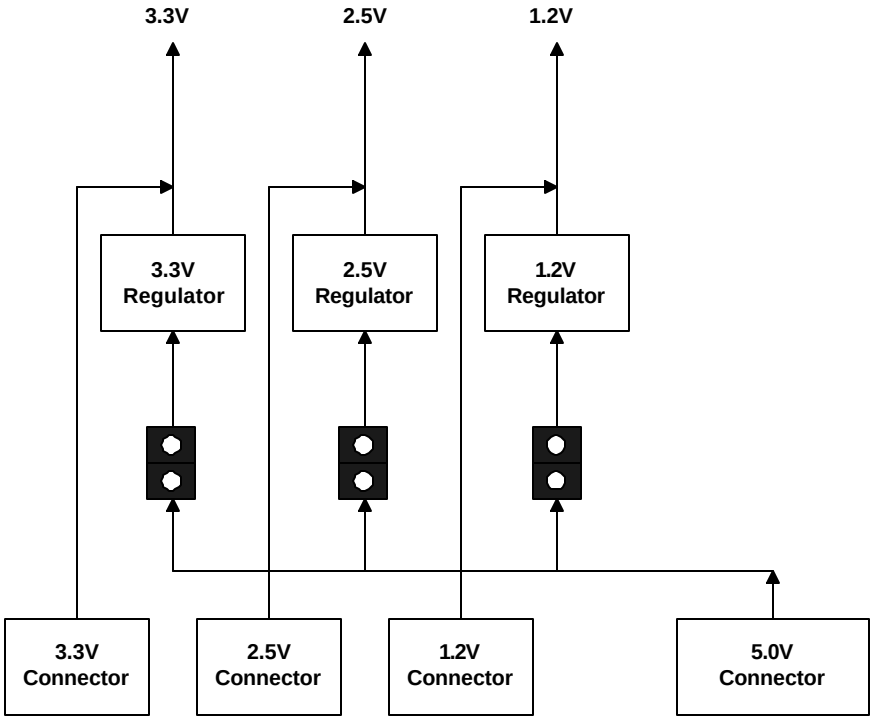


Figure 14 - Voltage Regulators

The following table shows the power provided on the development board for the on-board voltage sources. A 32.5W power adapter (5V @ 6.5A) is used to provide power to the on-board regulators. The following table shows typical power usage on the Virtex-4 FX12 LC development board.

Table 16 – Typical Power

Voltage	Current (A)	Power (W)	Comments
1.2V	2.0	2.4	FPGA Core voltage
2.5V	2.0	5.0	FPGA I/O voltage, P160 supply voltage
3.3V	3	9.9	FPGA I/O voltage, P160 supply voltage.
Total Power		**17.3**	

For the on-board digital voltages (1.2V, 2.5V, and 3.3V), if the current provided by the on-board regulator is not sufficient for some applications, the user can directly drive the voltage source and bypass the on-board regulators.

3.12 Bank I/O Voltage

The following table shows the Virtex-4 bank I/O voltages on the Virtex-4 FX12 LC development board.

Table 17 – I/O Bank Voltages

Bank #	I/O Voltage
0	2.5V
1	2.5V
2	2.5V
3	2.5V
4	3.3V
5	2.5V
6	3.3V
7	3.3V
8	3.3V
9	NC
10	NC

3.13 P160 Expansion Module Signal Assignments

The following tables show the Virtex-4 pin assignments to the P160 Expansion Module connectors (JX1 & JX2) located on the Virtex-4 FX12 LC development board.

Table 18 – P160 Connector Pin Assignments

Virtex-4 FPGA Pin #	I/O Connector Signal Name	JX1 Pin #		I/O Connector Signal Name	Virtex-4 FPGA Pin #
NC	TCK	A1	B1	FPGA.BITSTREAM	NC
	GND	A2	B2	SM.DOUT/BUSY	NC
NC	TMS	A3	B3	FPGA.CCLK	NC
	Vin	A4	B4	DONE	NC
NC	TDI	A5	B5	INITn	NC
	GND	A6	B6	PROGRAMn	NC
NC	TDO	A7	B7	NC	NC

	3.3V	A8	B8	LIOB8	AB18
AC10	LIOA9	A9	B9	LIOB9	AA19
	GND	A10	B10	LIOB10	AB20
AF10	LIOA11	A11	B11	LIOB11	AB21
	2.5V	A12	B12	LIOB12	AB22
AF11	LIOA13	A13	B13	LIOB13	AA20
	GND	A14	B14	LIOB14	Y21
AF12	LIOA15	A15	B15	LIOB15	Y22
	Vin	A16	B16	LIOB16	AC18
AE12	LIOA17	A17	B17	LIOB17	AD19
	GND	A18	B18	LIOB18	AC19
AE13	LIOA19	A19	B19	LIOB19	AD20
	3.3V	A20	B20	LIOB20	AC20
AB10	LIOA21	A21	B21	LIOB21	AD21
	GND	A22	B22	LIOB22	AC21
AD10	LIOA23	A23	B23	LIOB23	AD22
	2.5V	A24	B24	LIOB24	AC22
AD11	LIOA25	A25	B25	LIOB25	AD23
	GND	A26	B26	LIOB26	AC23
AD16	LIOA27	A27	B27	LIOB27	AC24
	Vin	A28	B28	LIOB28	AB23
AC17	LIOA29	A29	B29	LIOB29	AB24
	GND	A30	B30	LIOB30	AA23
W20	LIOA31	A31	B31	LIOB31	AA24
	3.3V	A32	B32	LIOB32	Y23
AD12	LIOA33	A33	B33	LIOB33	Y24
	GND	A34	B34	LIOB34	W23
AD17	LIOA35	A35	B35	LIOB35	W24
	2.5V	A36	B36	LIOB36	W22
W19	LIOA37	A37	B37	LIOB37	W21
	GND	A38	B38	LIOB38	V22
AB17	LIOA39	A39	B39	LIOB39	V21
	Vin	A40	B40	LIOB40	V20

Table 19 - P160 Connector Pin Assignments

Virtex-4 FPGA Pin #	**I/O Connector Signal Name**	**JX2 Pin #**		**I/O Connector Signal Name**	**Virtex-4 FPGA Pin #**
AF9	RIOA1	A1	B1	**GND**	
AE9	RIOA2	A2	B2	RIOB2	AC9
AF8	RIOA3	A3	B3	**Vin**	
AF7	RIOA4	A4	B4	RIOB4	AD8
AE7	RIOA5	A5	B5	**GND**	
AF6	RIOA6	A6	B6	RIOB6	AC8
AE6	RIOA7	A7	B7	**3.3V**	
AF5	RIOA8	A8	B8	RIOB8	AD7
AF4	RIOA9	A9	B9	**GND**	
AE4	RIOA10	A10	B10	RIOB10	AC7
AF3	RIOA11	A11	B11	**2.5V**	
AE3	RIOA12	A12	B12	RIOB12	AD6
AD2	RIOA13	A13	B13	**GND**	

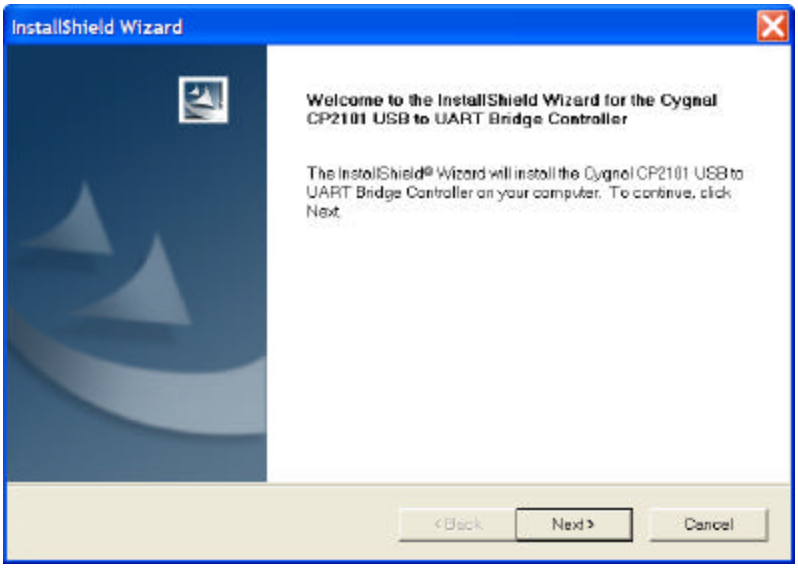
AD1	RIOA14	A14	B14	RIOB14	AC6
AC2	RIOA15	A15	B15	**Vin**	
AC1	RIOA16	A16	B16	RIOB16	AD5
AB2	RIOA17	A17	B17	**GND**	
AB1	RIOA18	A18	B18	RIOB18	AC5
AA1	RIOA19	A19	B19	**3.3V**	
Y2	RIOA20	A20	B20	RIOB20	AD4
Y1	RIOA21	A21	B21	**GND**	
W2	RIOA22	A22	B22	RIOB22	AD3
W1	RIOA23	A23	B23	**2.5V**	
AA10	RIOA24	A24	B24	RIOB24	AC4
AA9	RIOA25	A25	B25	**GND**	
AA8	RIOA26	A26	B26	RIOB26	AC3
AB9	RIOA27	A27	B27	**Vin**	
AB7	RIOA28	A28	B28	RIOB28	AB4
AA7	RIOA29	A29	B29	**GND**	
AB6	RIOA30	A30	B30	RIOB30	AB3
AB5	RIOA31	A31	B31	**3.3V**	
Y6	RIOA32	A32	B32	RIOB32	AA4
Y5	RIOA33	A33	B33	**GND**	
W6	RIOA34	A34	B34	RIOB34	AA3
W5	RIOA35	A35	B35	**2.5V**	
W7	RIOA36	A36	B36	RIOB36	Y3
V5	RIOA37	A37	B37	**GND**	
V6	RIOA38	A38	B38	RIOB38	Y4
V7	RIOA39	A39	B39	**Vin**	
W4	RIOA40	A40	B40	RIOB40	W3

4 Revisions

V1.0	Initial release for Rev 1 board	April 21, 2005
V1.1	Added JP36 description	May 27, 2006

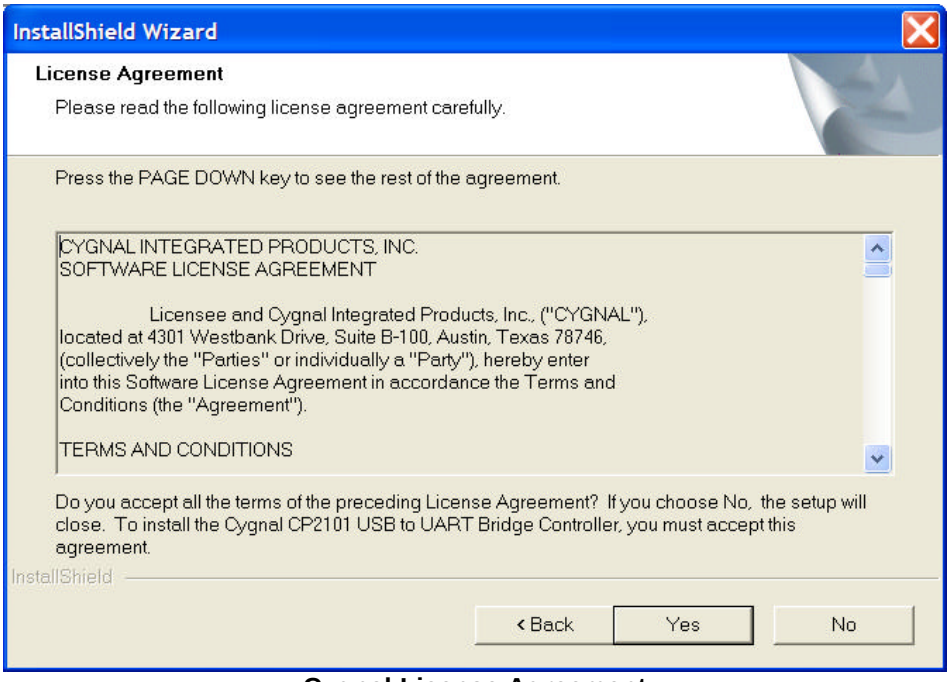
Appendix A

1. Double-click CP2101_Drivers.exe.



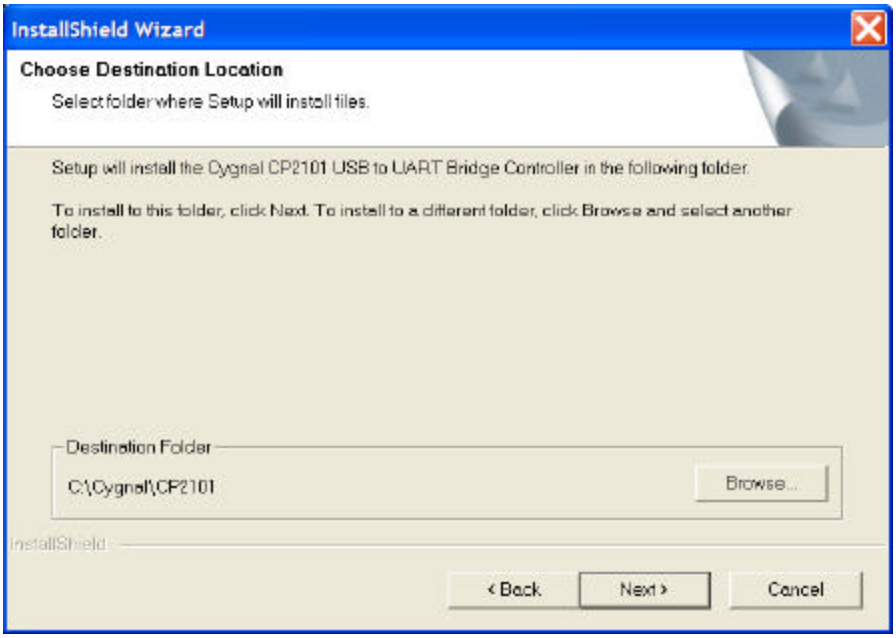
Launching CP2101 Driver Installation

2. Click Next.
3. Read the license agreement and then click Yes.



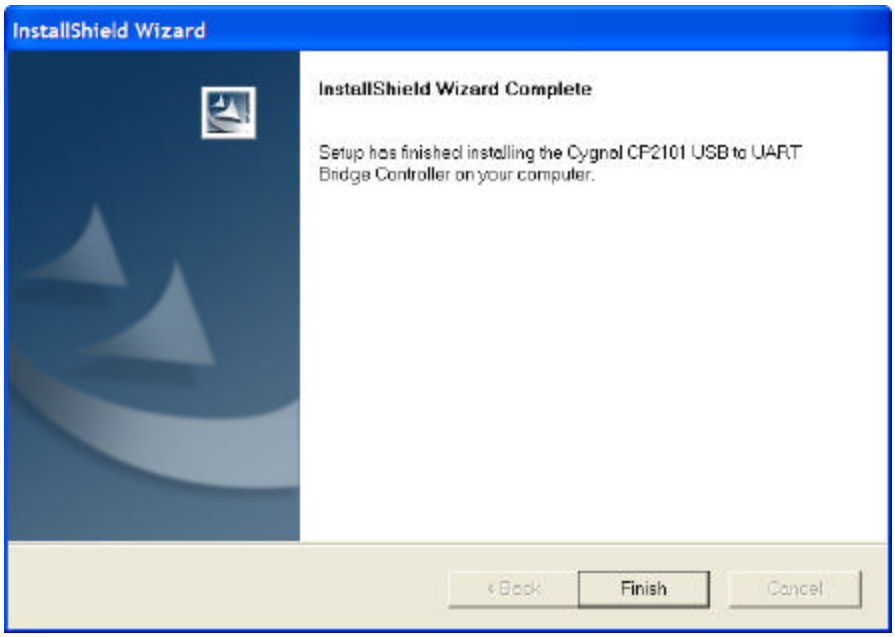
Cygnal License Agreement

4. Browse to an acceptable installation directory, then click Next.



CP2101 Destination Location

5. The drivers are extracted to the selected directory. Click Finish once the extraction completes.



CP2101 Installation Successful

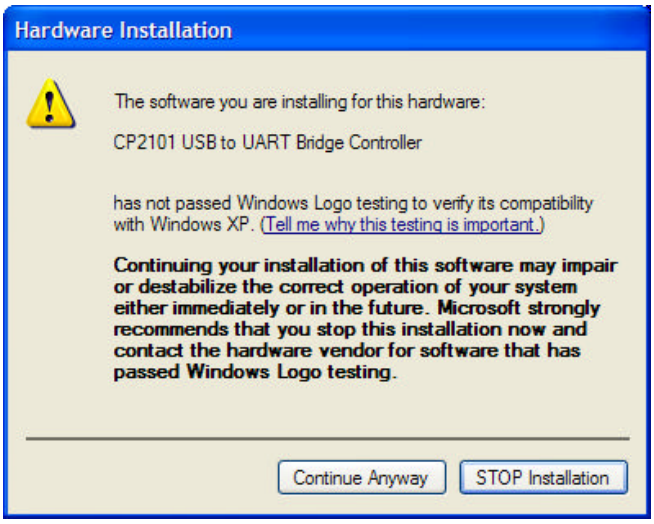
6. To finish the installation, plug the USB cable into the board and a USB port on the PC.

7. Turn the board power switch to the ON position.

8. The **Found New Hardware Wizard** launches. Click the radio button to **Install the software automatically (Recommended)** and then click Next.

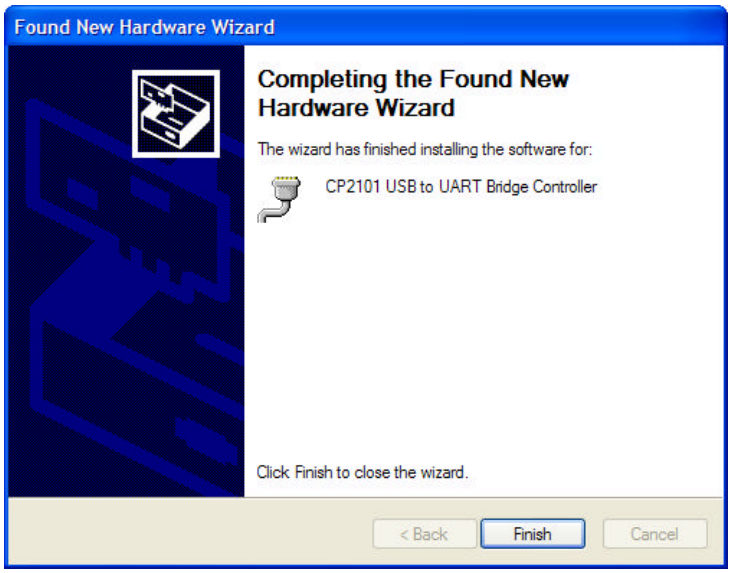
Found New Hardware Wizard

9. The driver installation begins. If installing on WindowsXP, a warning is received stating that Windows Logo testing has not passed, as shown below. Click **Continue Anyway**.



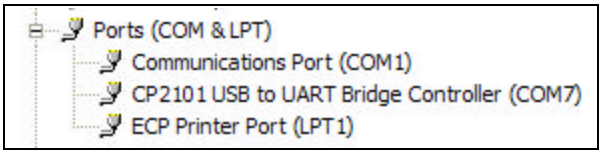
Windows Logo Testing Not Passed

10. The driver installation completes at this point. Click Finish in the **Found New Hardware Wizard**.



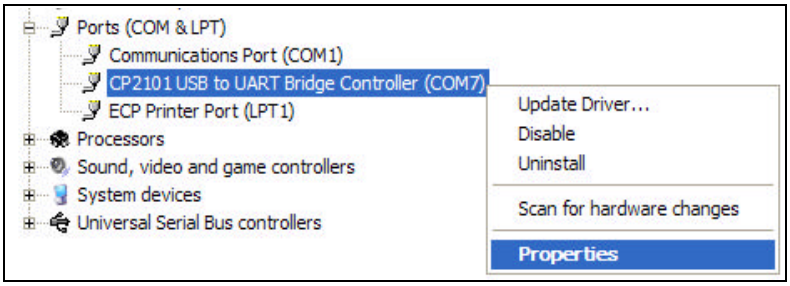
CP2101 Driver Installation Complete

11. Open the Device Manager (Control Panel → System → Hardware tab → Device Manager).
12. Under the **Ports** heading, a new device shows up, called **CP2101 USB to UART Bridge Controller**.



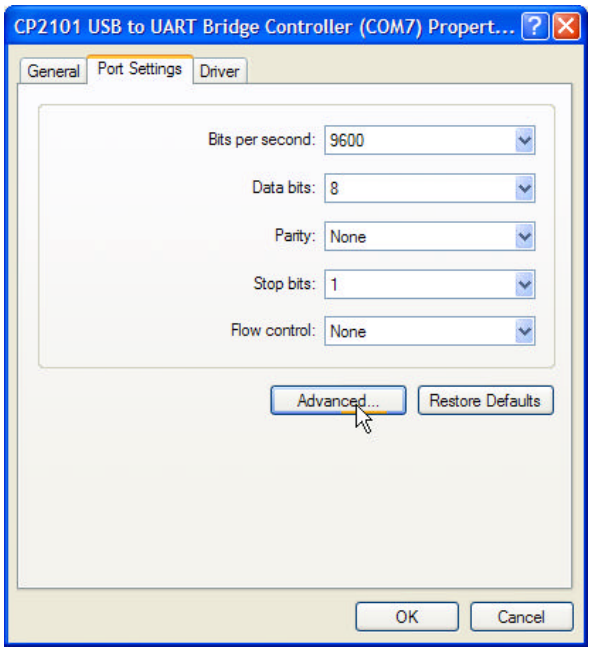
CP2101 Recognized as COM Port

13. If the CP2101 does not show up under ports, it may show up under "Other Devices" with a yellow exclamation mark. In this case, unplug the USB cable, run the setup manually (C:\Cygnal\CP2101\WIN\Setup.exe), and then plug the USB cable back in.
14. The O/S automatically assigns a COM Port number, typically between COM3 and COM7. For consistency, the COM number will be manually changed. Right click on **CP2101 USB to UART Bridge Controller** and select **Properties**.



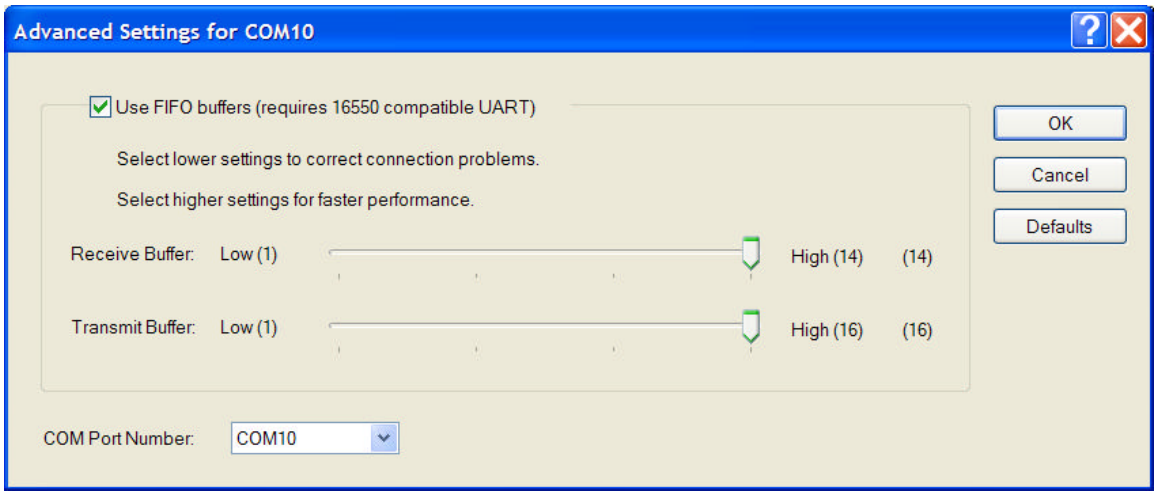
COM Port Properties

15. Change to the **Port Settings** tab and select **Advanced**.



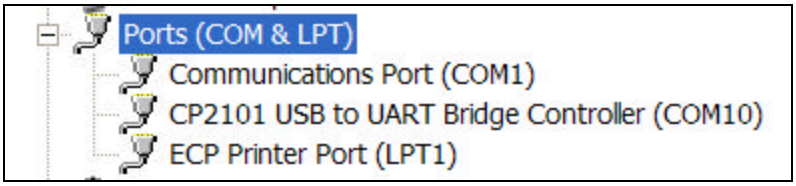
Port Settings – Advanced

16. Select COM10 in the **COM Port Number** field, then click OK twice.



Changing the COM Port Number

17. Close the Device Manager, and then re-open it. Under **Ports**, the CP2101 USB to UART Bridge Controller is now assigned to COM10, as shown below.



CP2101 Assigned to COM10