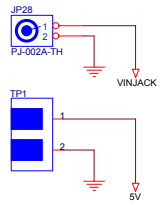
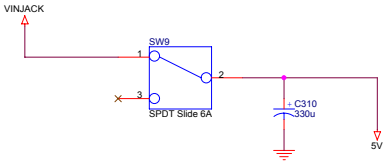
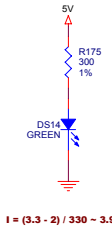
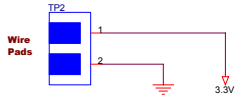
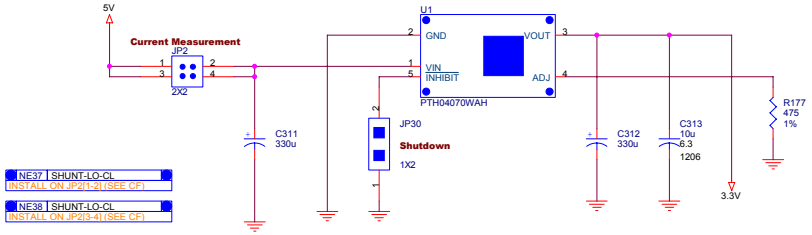
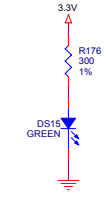
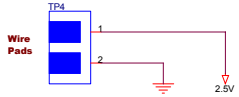
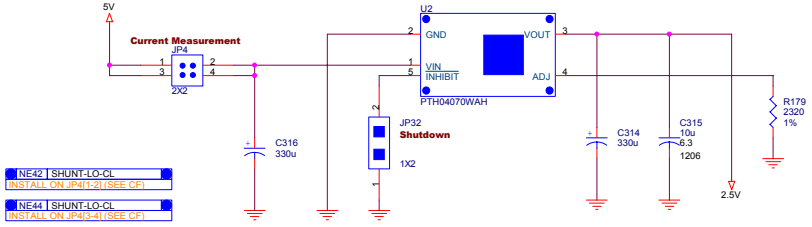
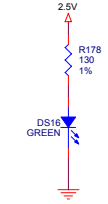
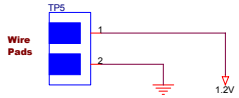
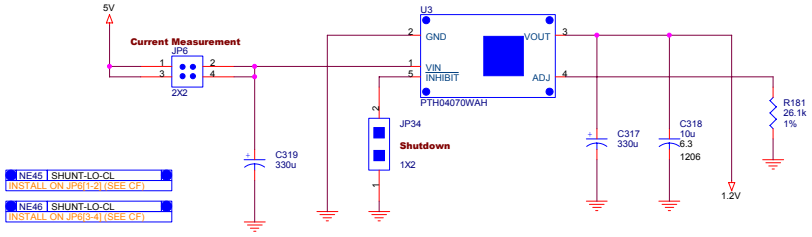
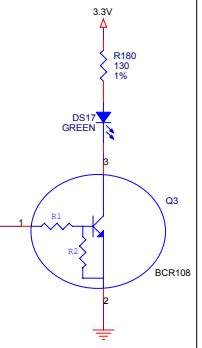
V4FX12LC

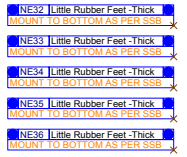
REV1

BOARD NAME :	**VIRTEX-4 FX12 LC DEVELOPMENT BOARD**
BOARD PART NUMBER :	**DS-BD-V4FX12LC**
BOARD REVISION :	**1**

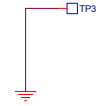
Memec Board	MemecBoard Calgary, Alberta Canada	BOARD TITLE VIRTEX-4 FX12 LC DEVELOPMENT BOARD	PAGE TITLE TITLE PAGE	LAST MODIFIED Friday, March 04, 2005	SIZE	C	DESIGNER	JBE	REVISION	1	SHEET	1	of	13

VOLTAGE	CURRENT	ALTERNATE PADS	REGULATION	LED
VIN (5V)	3A			
3.3V	3A			
2.5V	3A			
1.2V	3A			

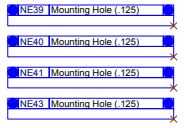
RUBBER FEET



GROUND TEST LOOPS

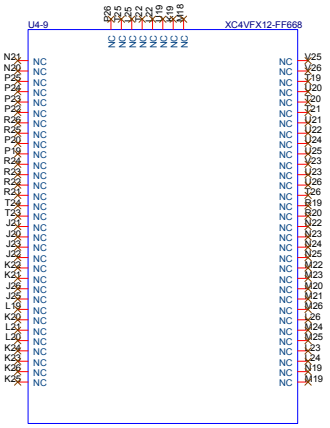


MOUNTING HOLES



MemecBoard Calgary, Alberta Canada	BOARD TITLE: VIRTEX-4 FX12 LC DEVELOPMENT BOARD	PAGE TITLE: POWER	LAST MODIFIED: Friday, March 04, 2005	SIZE	C	DESIGNER	JBE	REVISION	1	SHEET	2	of 13

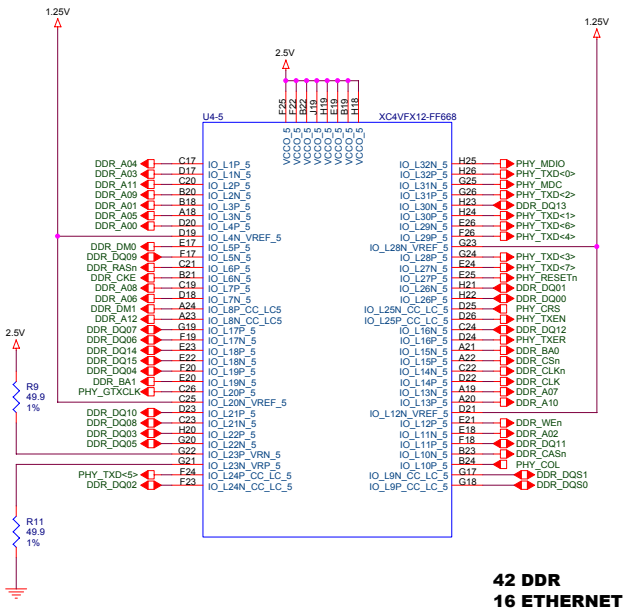
BANK 9 - NC



64 NC

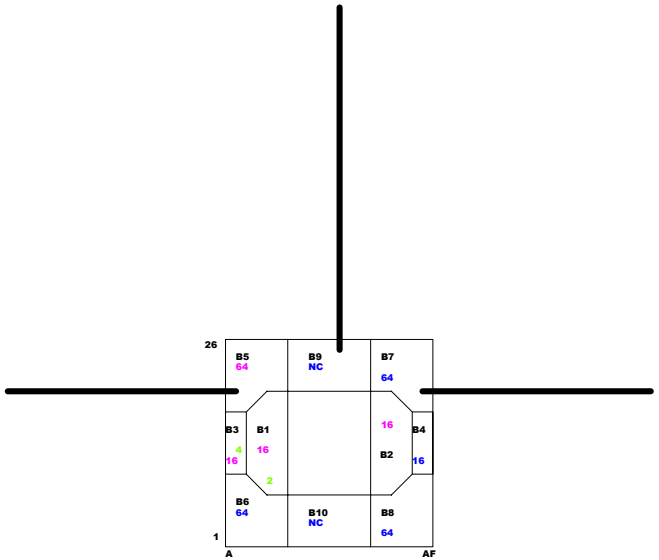
BANK 5 - ETHERNET & DDR

** - DQS SIGNALS MUST BE ON CC PINS



64 IO

42 DDR
16 ETHERNET
2 DCI
4 VREF



BANK 7 - JX1 & SAM

64 IO

35 JX1
29 SAM

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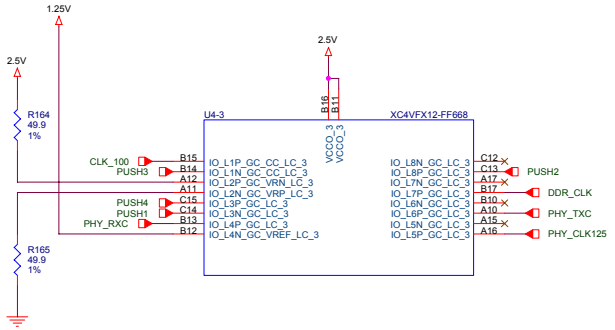
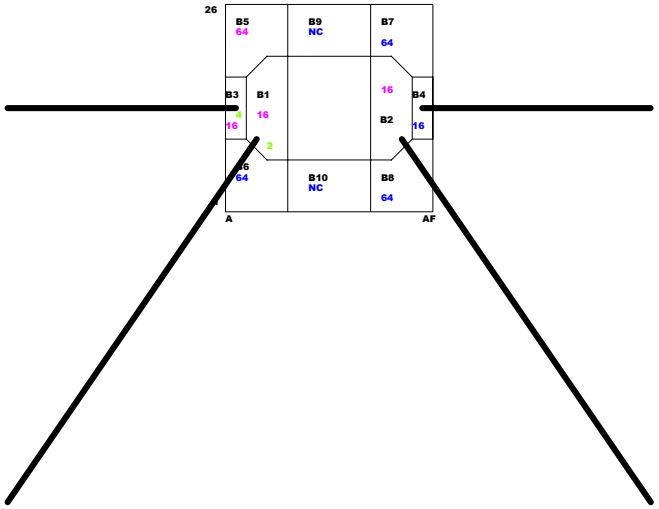
BANK 3 - DDR & ETHERNET & CLOCK & SWITCH



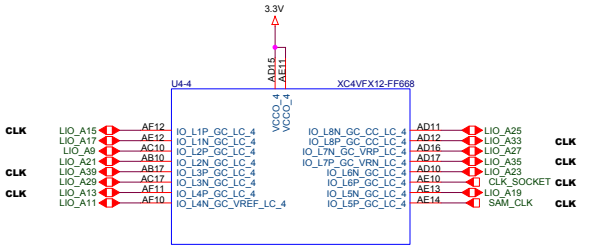
1 DDR*
1 CAN*
3 ETHERNET
4 SWITCHES
4 NC
2 DCI
1 VREF

16 IO

* - DDR CLOCK FEEDBACK AND CLOCK SOURCE MUST BE ON SAME SIDE OF FPGA



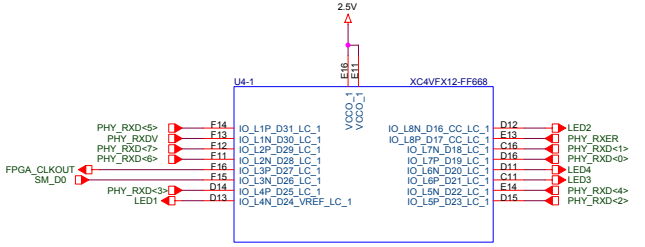
BANK 4 - JX1 & SAM & CLOCK



14 JX1
1 SAM
1 SOCKET

16 IO

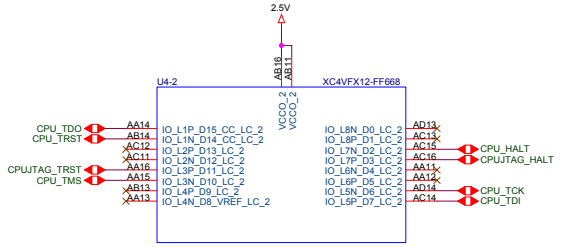
BANK 1 - ETHERNET & LED & CONFIG



4 LED
10 ETHERNET
2 CONFIG

16 IO

BANK 2 - CPU JTAG & CPU DEBUG



2 CPU JTAG
6 CPU DEBUG
8 NC

16 IO

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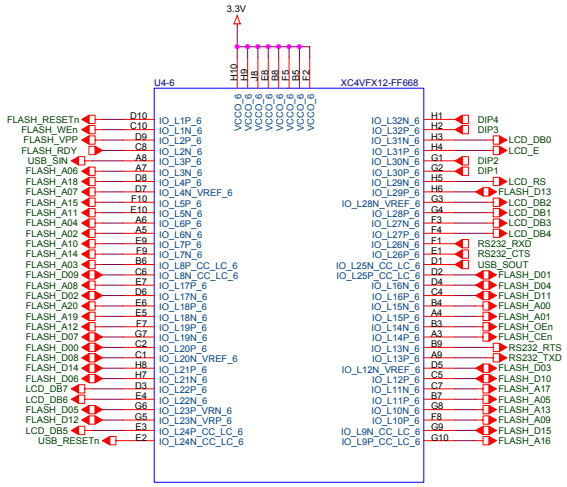
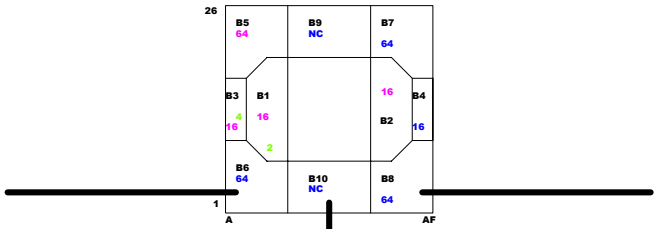
BANK 6 - FLASH & SWITCHES & LCD & RS232 & USB

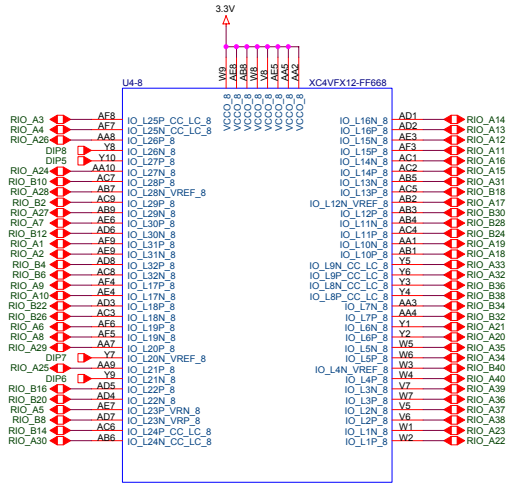


43 FLASH
4 SWITCHES
10 LCD
4 RS232
3 USB

64 IO



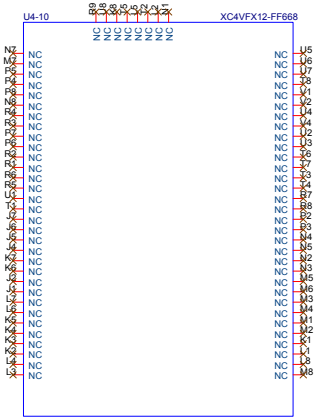
BANK 8 - JX2 & SWITCH



60 JX2
4 SWITCH

64 IO

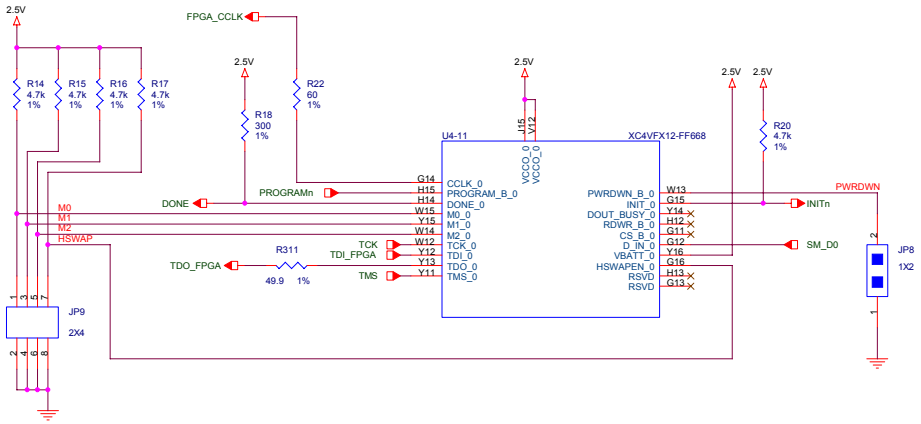
BANK 10 - NC



64 NC

Memec Board	MemecBoard Calgary, Alberta Canada	BOARD TITLE: VIRTEX-4 FX12 LC DEVELOPMENT BOARD	PAGE TITLE: FPGA SECTION 3	LAST MODIFIED: Friday, March 04, 2005	SIZE: C	DESIGNER: JBE	REVISION: 1	SHEET: 5 of 13

CONFIGURATION



NE15 | SHUNT-LO-CL
INSTALL ON JP9[1-2]

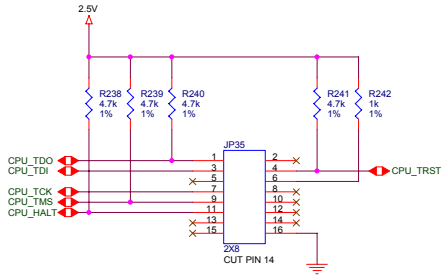
NE16 | SHUNT-LO-CL
INSTALL ON JP9[3-4]

NE17 | SHUNT-LO-CL
INSTALL ON JP9[5-6]

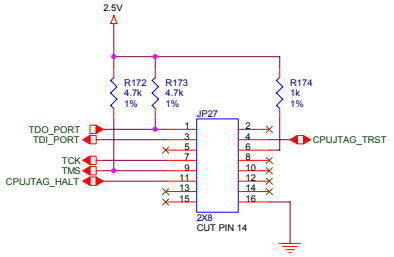
Mode	Pull-ups	0	1	2	3
Master-serial	No	■	■	■	
Slave Serial	No	□	□	■	
Master SelectMAP	Yes	□	□	□	
Slave SelectMAP	No	■	□	□	
Boundary-scan	No	□	■	□	
Pull-ups ON					■
Pull-ups OFF					□

■ Indicates jumper installed ('0')
□ Indicates jumper removed ('1')

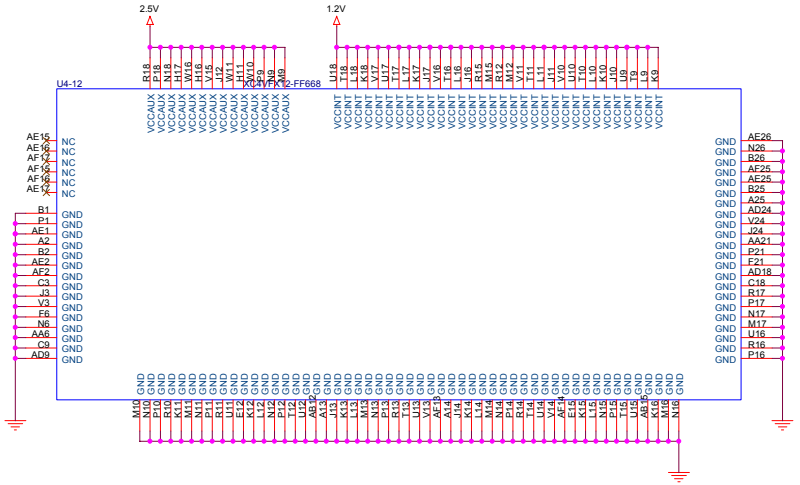
CPU DEBUG PORT



CPU JTAG PORT

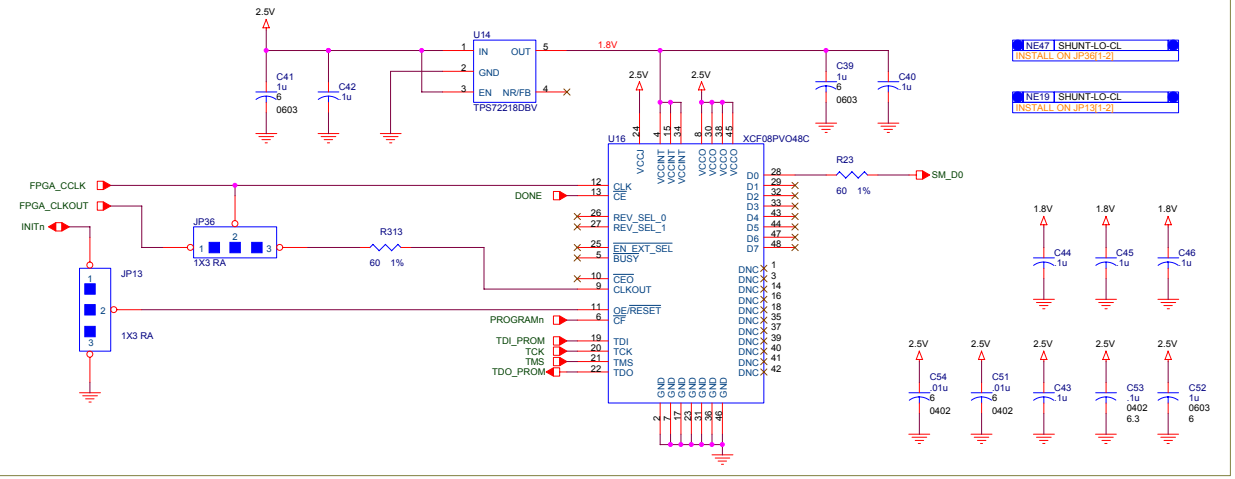


POWER

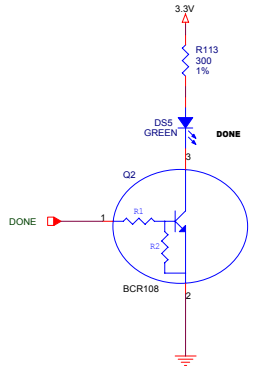


Memec Board	MemecBoard Calgary, Alberta Canada	BOARD TITLE: VIRTEX-4 FX12 LC DEVELOPMENT BOARD	PAGE TITLE: FPGA AUX	LAST MODIFIED: Friday, March 04, 2005	SIZE: C	DESIGNER: JBE	REVISION: 1	SHEET: 6 of 13

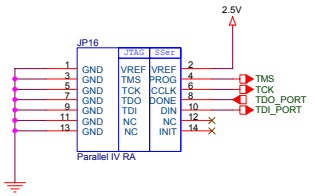
PROM (PLATFORM FLASH)



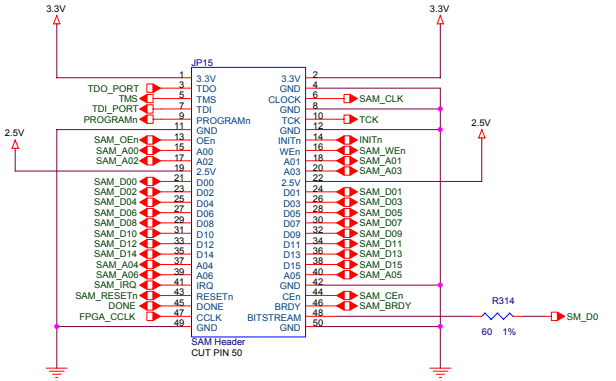
PROGRAMMING DONE LED



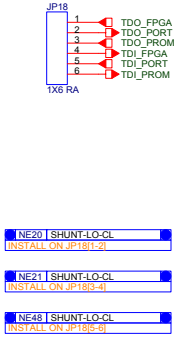
PARALLEL IV PORT - FPGA/CPLD



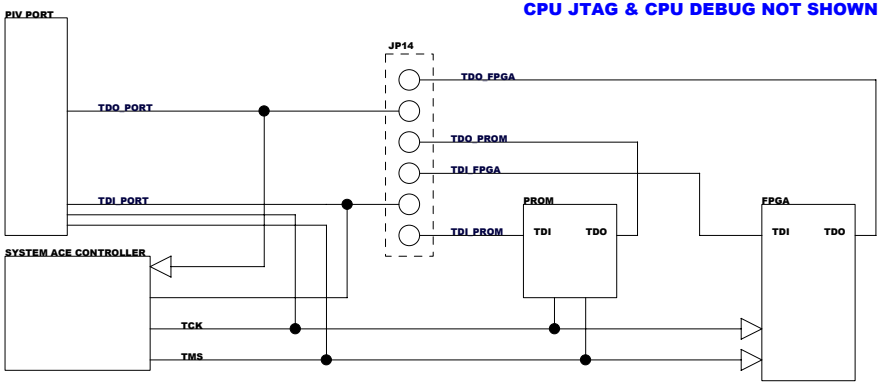
SAM HEADER



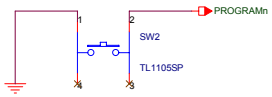
JTAG CHAIN SELECTOR



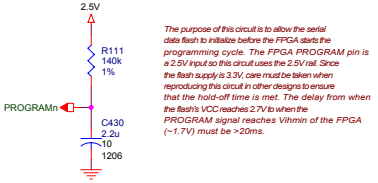
JTAG CHAIN DIAGRAM



PROGRAM PUSHBUTTON



PROGRAM HOLD-OFF CIRCUIT



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FPGA IO Decoupling

BANK6 - 8 PINS

3.3V: C177 .01u 6 0402; C178 .01u 6 0402; C179 .01u 6 0402; C180 .01u 6 0402; C191 1u 6.3 0402; C192 1u 6.3 0402; C193 1u 6 0603; +C189 330u

BANK3 - 2 PINS

2.5V: C181 .01u 6 0402; C182 1u 6.3 0402; C183 1u 6 0603; 1.25V: C302 1u 6.3 0402

BANK1 - 2 PINS

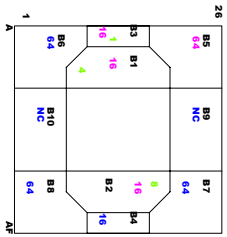
2.5V: C194 .01u 6 0402; C195 1u 6.3 0402; C196 1u 6 0603; +C188 330u

BANK5 - 8 PINS

2.5V: C184 .01u 6 0402; C185 .01u 6 0402; C186 .01u 6 0402; C187 .01u 6 0402; C197 1u 6.3 0402; C198 1u 6.3 0402; C199 1u 6 0603; 1.25V: C374 .01u 6 0402; C375 1u 6.3 0402; +C190 330u

BANK10 - NC

BANK9 - NC



BANK8 - 8 PINS

3.3V: C220 .01u 6 0402; C221 .01u 6 0402; C222 .01u 6 0402; C223 .01u 6 0402; C234 1u 6.3 0402; C235 1u 6.3 0402; C236 1u 6 0603; +C232 330u

BANK2 - 2 PINS

2.5V: C224 .01u 6 0402; C225 1u 6.3 0402; C226 1u 6 0603

BANK4 - 2 PINS

3.3V: C237 .01u 6 0402; C238 1u 6.3 0402; C239 1u 6 0603; +C231 330u

BANK7 - 8 PINS

3.3V: C227 .01u 6 0402; C228 .01u 6 0402; C229 .01u 6 0402; C230 .01u 6 0402; C240 1u 6.3 0402; C241 1u 6.3 0402; C242 1u 6 0603; +C233 330u

FPGA Aux Decoupling — 14 PINS

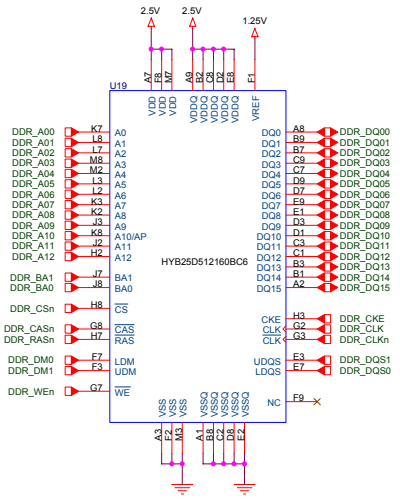
2.5V: C243 .01u 6 0402; C244 .01u 6 0402; C245 .01u 6 0402; C246 .01u 6 0402; C247 .01u 6 0402; C248 .01u 6 0402; C249 .01u 6 0402; C250 1u 6.3 0402; C251 1u 6.3 0402; C252 1u 6.3 0402; C253 1u 6 0603; C254 1u 6 0603; C255 10u 6.3 1206; +C256 330u 6.3

FPGA Core Decoupling — 32 PINS

1.2V: C257 .01u 6 0402; C258 .01u 6 0402; C259 .01u 6 0402; C260 .01u 6 0402; C261 .01u 6 0402; C262 .01u 6 0402; C263 .01u 6 0402; C264 .01u 6 0402; C265 .01u 6 0402; C266 .01u 6 0402; C267 .01u 6 0402; C268 .01u 6 0402; C269 .01u 6 0402; C270 .01u 6 0402; C271 .01u 6 0402; C272 .01u 6 0402; C273 .01u 6 0402; C274 .01u 6 0402; C275 .01u 6 0402; C276 .01u 6 0402; C277 .01u 6 0402; C278 .01u 6 0402; C279 .01u 6 0402; C280 .01u 6 0402; C281 1u 6.3 0402; C282 1u 6.3 0402; C283 1u 6.3 0402; C284 1u 6.3 0402; C285 1u 6 0603; C286 1u 6 0603; C287 10u 6.3 1206; C288 10u 6.3 1206; +C289 330u; +C290 330u

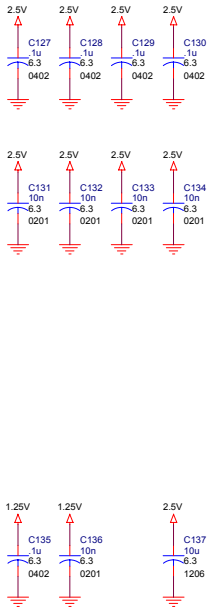
MemecBoard, Calgary, Alberta Canada	BOARD TITLE: VIRTEX-4 FX12 LC DEVELOPMENT BOARD	PAGE TITLE: FPGA DECOUPLING	LAST MODIFIED: Friday, March 04, 2005	SIZE: C	DESIGNER: JBE	REVISION: 1	SHEET: 8 of 13

DDR

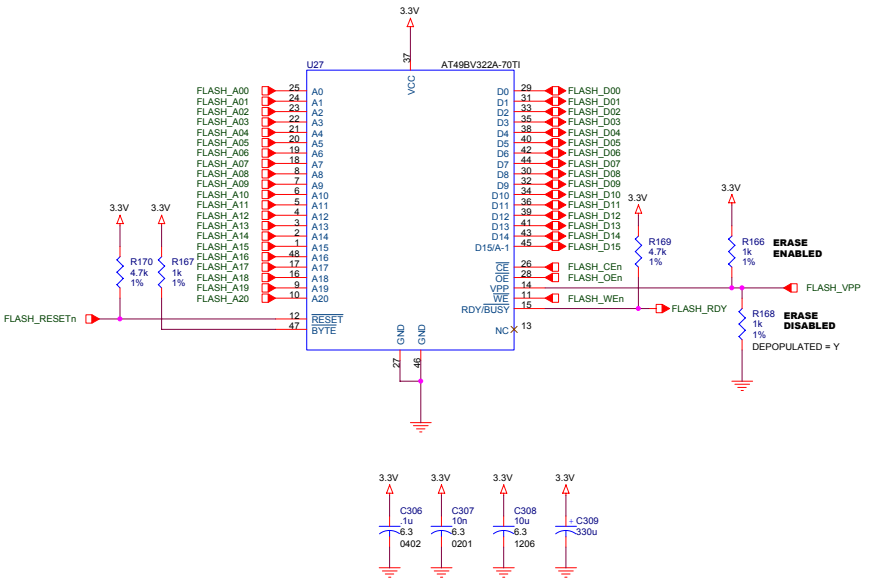


42 IO

DECOUPLING

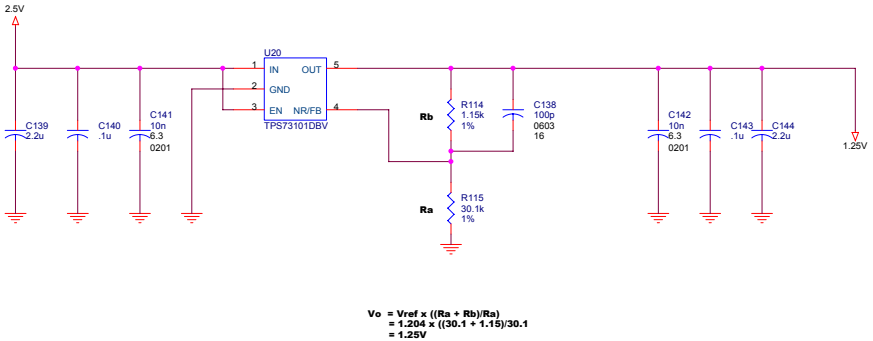


FLASH



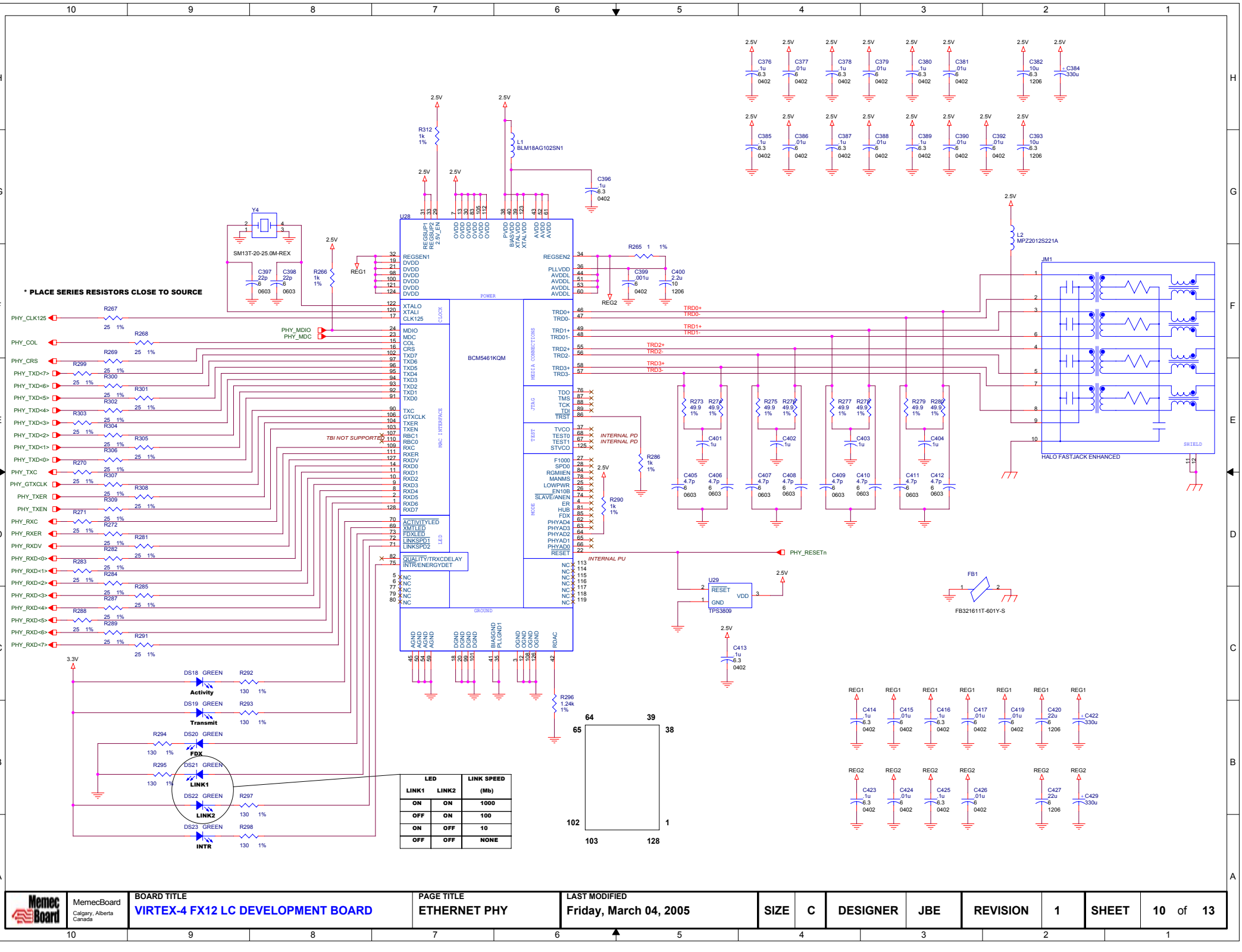
44 IO

1.25V



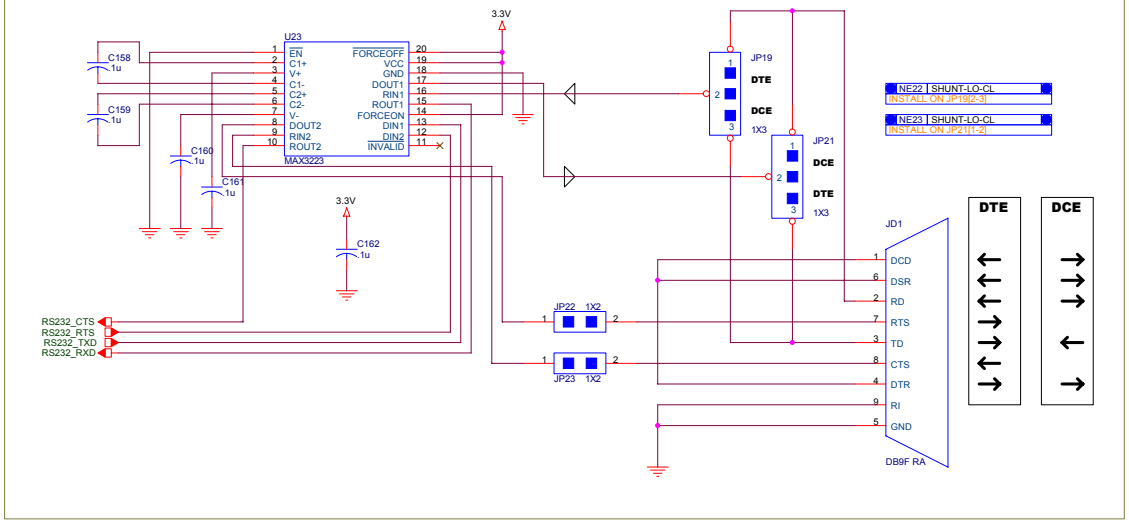
Vo = Vref x ((Ra + Rb)/Ra)
= 1.204 x ((30.1 + 1.15)/30.1
= 1.25V

Memec Board	MemecBoard Calgary, Alberta Canada	BOARD TITLE: VIRTEX-4 FX12 LC DEVELOPMENT BOARD	PAGE TITLE: DDR & FLASH	LAST MODIFIED: Friday, March 04, 2005	SIZE	C	DESIGNER	JBE	REVISION	1	SHEET	9 of 13

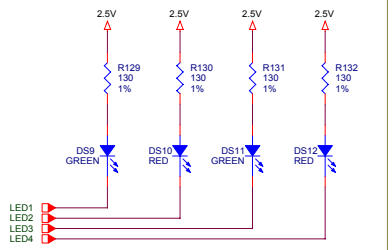


Memec Board	MemecBoard Calgary, Alberta Canada	BOARD TITLE: VIRTEX-4 FX12 LC DEVELOPMENT BOARD	PAGE TITLE: ETHERNET PHY	LAST MODIFIED: Friday, March 04, 2005	SIZE	C	DESIGNER	JBE	REVISION	1	SHEET	10	of 13

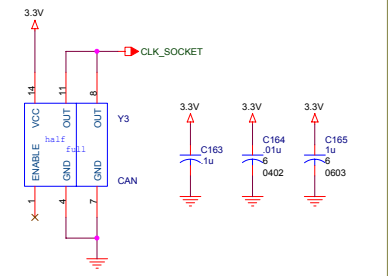
SERIAL PORT



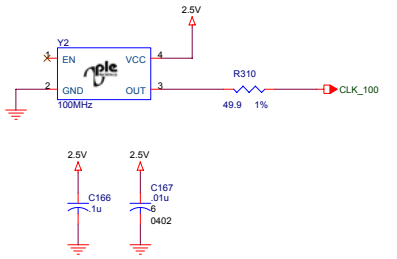
LEDs



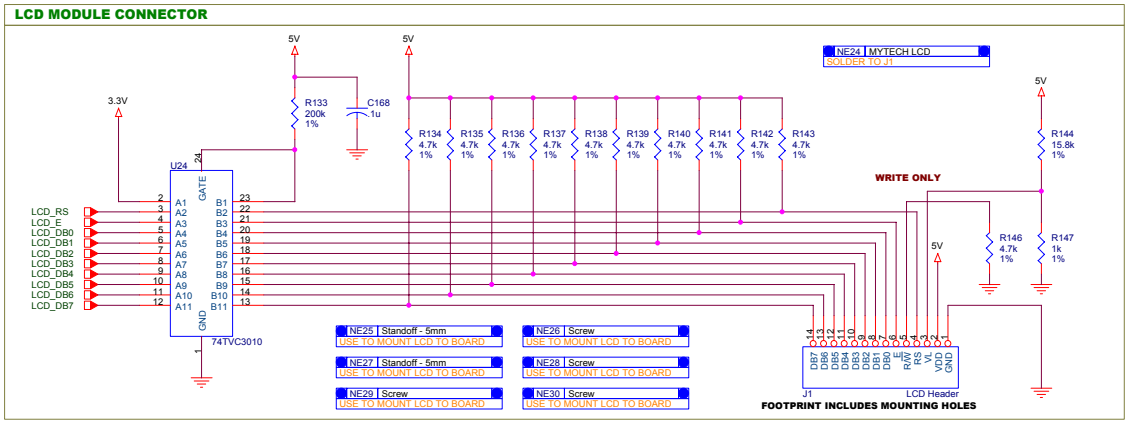
CLOCK SOCKET



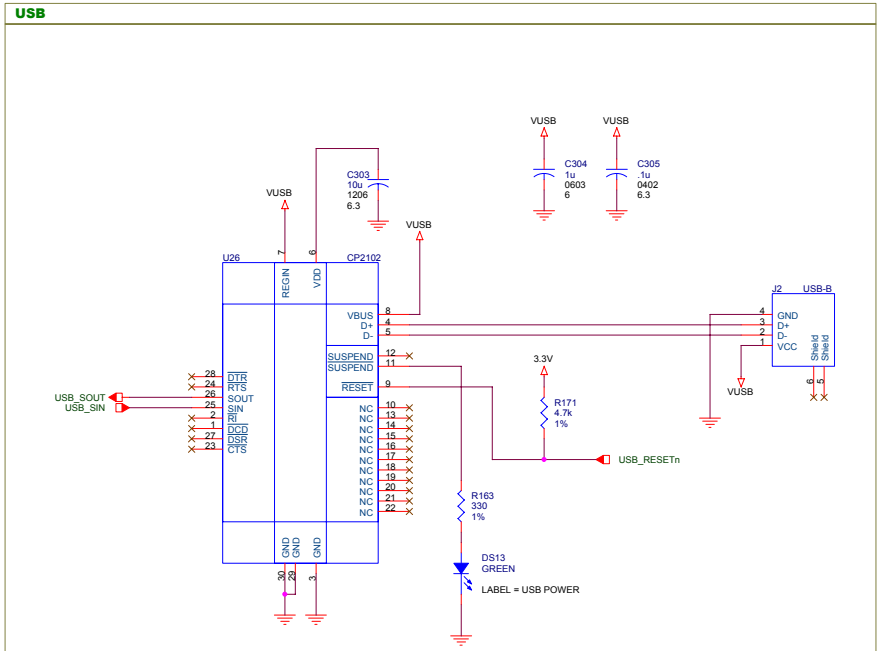
100MHz CLOCK



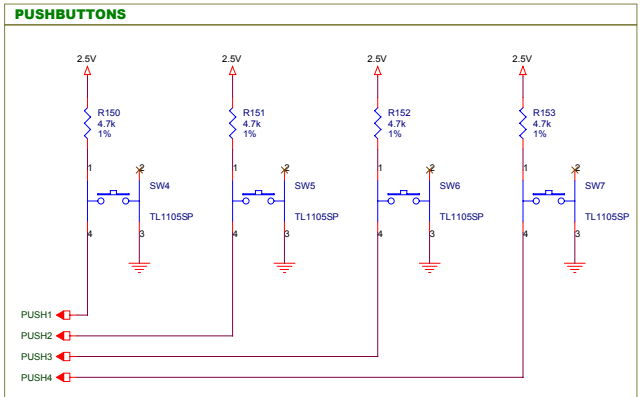
LCD MODULE CONNECTOR



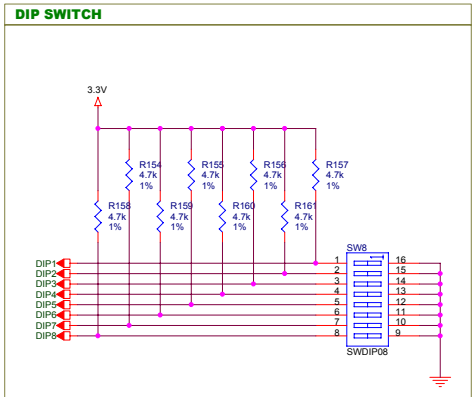
USB



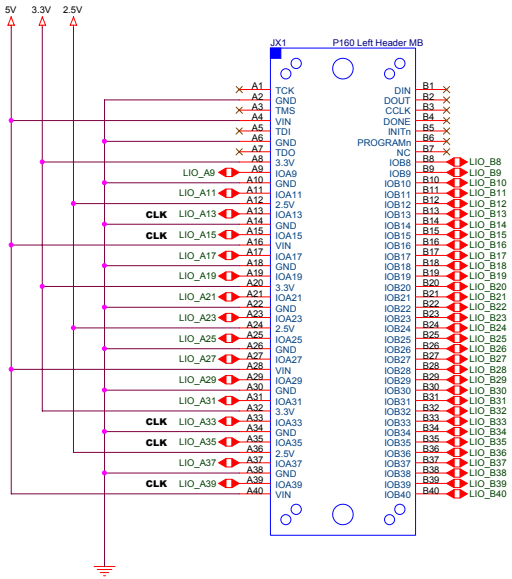
PUSHBUTTONS

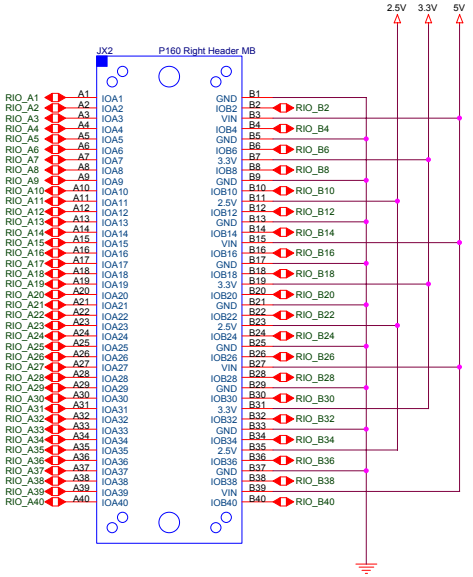


DIP SWITCH



Memec Board	MemecBoard Calgary, Alberta Canada	BOARD TITLE: VIRTEX-4 FX12 LC DEVELOPMENT BOARD	PAGE TITLE: USER IO & CLOCKS	LAST MODIFIED: Friday, March 04, 2005	SIZE: C	DESIGNER: JBE	REVISION: 1	SHEET: 11 of 13

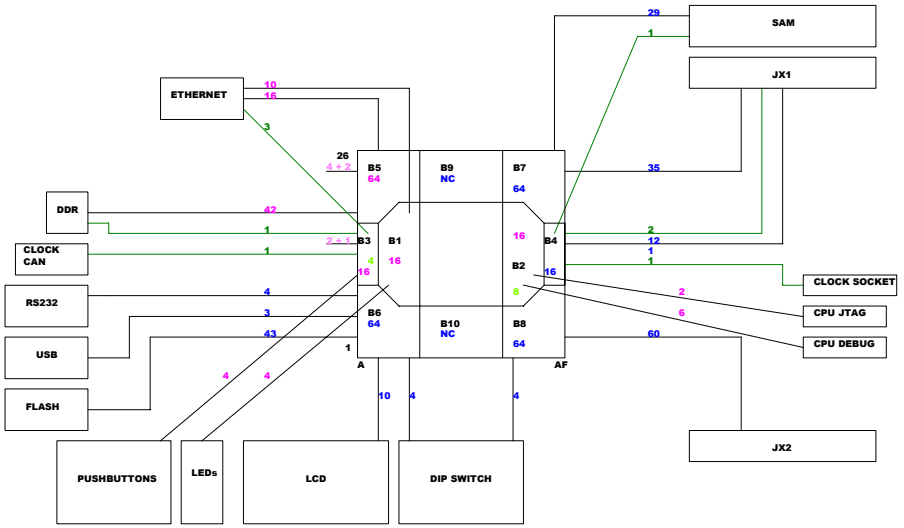




MemecBoard Calgary, Alberta Canada	BOARD TITLE VIRTEX-4 FX12 LC DEVELOPMENT BOARD	PAGE TITLE P160	LAST MODIFIED Friday, March 04, 2005	SIZE	C	DESIGNER	JBE	REVISION	1	SHEET	12 of 13

REV A	REV 1
FIRST RELEASE	ADDED 2.5V PULL-UP TO PHY'S 2.5V_EN
	CHANGED CLOCK CAN TO 2.5V VCC
	ADDED SERIES TERMINATION TO CLK_100
	ADDED SERIES TERMINATION TO TDO_FPGA
	REMOVED 100 OHM PULL-UP FROM TDO_FPGA
	ADDED CCLK SELECT JUMPER
	ADDED D0 CONNECTION TO FPGA IO
	REMOVED _2V5 FROM P160 NETNAMES
	MOVED PUSHBUTTONS FROM BANK8 TO BANK3
	MOVED FOUR DIP SWITCH FROM BANK6 TO BANK8
	MOVED USB AND RS232 SIGNALS FROM BANK3 TO BANK6
	CHANGED DIP SWITCH PULL-UP VOLTAGE TO 3.3V
	ADDED PROGRAM HOLD-OFF CIRCUIT
	REMOVED SDF CIRCUIT & CONNECTOR
	REMOVED INIT_PROGRAM
	ADDED FIFTH RUBBER FOOT

PLACEMENT



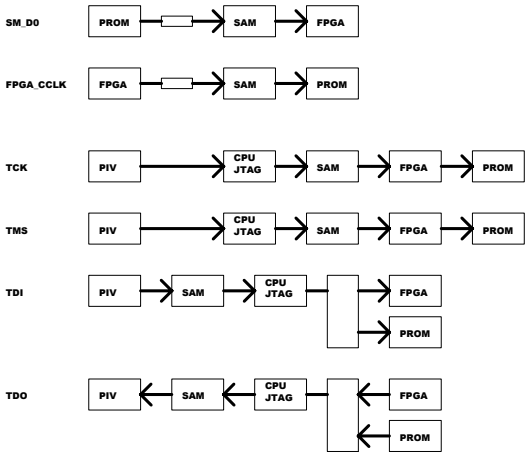
BANK	IO	CLK
1	16	-
2	16	-
3	16	-
4	16	-
5	64	-
6	64	-
7	64	-
8	64	-
9	0	-
10	0	-
TOTAL	320	-

* - all IO on BANKs 3 & 4 can be used as global clock inputs
* - "N" GCLK PINS CAN ONLY BE USED AS A PAIR WITH THE "P" PIN

DEVICE	IO	CLK
CLOCKs	-	2
RS232	4	-
DDR	51	1
FLASH	43	-
CPU JTAG	2	-
CPU DEBUG	6	-
CONFIGURE	2	-
LCD	10	-
JX1	47	2
JX2	60	-
USB	3	-
ETHERNET	27	2
LEDs	4	-
SWITCHES	12	-
SAM	29	1
UNUSED	13	-
TOTAL	312 + 8	= 320

ORANGE = 2.5V/3.3V IO
PINK = 2.5V IO
BLUE = 3.3V IO
GREEN = CLOCK
LIME = UNUSED

CONFIG SIGNAL PCB ROUTING



Memec Board	MemecBoard Calgary, Alberta Canada	BOARD TITLE: VIRTEX-4 FX12 LC DEVELOPMENT BOARD	PAGE TITLE: HISTORY & PLACEMENT	LAST MODIFIED: Friday, March 04, 2005	SIZE: C	DESIGNER: JBE	REVISION: 1	SHEET: 13 of 13