Zigang Xiao (Ivan)

Curriculum Vitae (as of February 18, 2014)

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Objectives & Interests

I am a PhD student looking for summer intern (2014) as a software engineer or research scientist, preferably the backend positions where I can utilize my expertise in Software Development, Machine Learning, Computer Vision or Design Automation.

Education

8/2010-1/2015 (expected) **Ph.D. Candidate**, Department of Electrical and Computer Engineering, University of Illinois at Urbana-Champaign (UIUC), Urbana, IL, USA. [GPA: **3.87/4.0**]

8/2008-8/2010

Master of Philosophy, Department of Computer Science and Engineering, The Chinese University of Hong Kong (CUHK), Hong Kong. [GPA: **3.9/4.0**]

9/2004-7/2008

Bachelor of Science, Department of Computer Science, Sun Yat-Sen University (SYSU), Guangzhou, China. [GPA: **3.9/4.0**, Ranking: **1/200**, graduated with outstanding honor]

Professional Skills

- Languages (proficient): C/C++, Matlab, Python, Bash scripting
- Languages (prior experience): Java, Obj-C, Ruby, Lua, JavaScript & HTML, x86 asm
- Softwares: gcc, gdb, make, cmake, git, vim, awk, sed, grep, Visual Studio, Eclipse
- Operating systems: Linux, OS X, Windows

Industrial Experience

5/2013-8/2013

R&D Engineer Intern, *Synopsys Inc.*, 700 E Middlefield Rd, Mountain View, CA 94043. I worked in Zroute Team, Implementation Group and involed in the router development for IC Compiler.

5/2012-8/2012

CAD Engineer Intern, *NVIDIA Corporation*, 2701 San Tomas Expy, Santa Clara, CA 95050. I worked in DFT/CAD Team and involved in developing internal tools for scan chain flow.

3/2008-6/2008

Software Engineer Intern, *Ericsson Mobile Data Applications Tech R&D*, Guangzhou, China. Prototyping PKI/CA system.

Teaching Experience

1/2013-current

Teaching Assistant, Department of CS, UIUC, Urbana, IL.

MOOC course: VLSI CAD: Logic to Layout. Available online at www.coursera.org/course/vlsicad. Taught by Prof. Rob Rutenbar, head of CS department. More than 17, 000 students registered in 2013.

1/2012-current

Teaching Assistant, Department of ECE, UIUC, Urbana, IL.

- ECE 425 (FA 12/13), Intro to VLSI Sys. Design - ECE 411 (SP '11), Computer Architecture

8/2008-8/2010

Teaching Assistant, Department of CSE, CUHK, Hong Kong.

- CSC 3120 (SP '10), Compiler Construction
- CSC 3190 (FA '09), Discrete Math and Algos
- CSC 4430 (SP '08), Computer Networks
- CSC 3150 (FA '08), Intro to Operating System

Research Experience & Selected Projects

current Direct Self-Assembly (DSA) Template Verification, Research, C++, Matlab, 2000 lines.

We utilized various computer vision and machine learning techniques to build a DSA template classifier that can achieve up to 85% accuracy. This is the first work for the related problem.

current **Self-Aligned Double Patterning layout decomposition**, Research, C++, CGAL, 5000 lines.

- We proposed a graph-coloring based algorithm that optimally finds a no-overlay decomposition in polynomial time, while previous approaches adopted exponential time methods.
- We further proposed a shortest-path based algorithm that utilizes the characteristics of standard cell row-based layout and solves the problem efficiently in polynomial time.

1/2013–5/2013 Reference Placer, Router and Graders, for MOOC course, C++, 3000 lines.

I developed an analytical placer and a maze router as reference programs, and corresponding auto-graders.

1/2012–5/2012 Carcassonne Board Game Scorer, Course Project for Computer Vision, Matlab, 1000 lines.

I developed a program that automatically computes the score from a picture of a Carcassonne boardgame.

8/2011–12/2011 **Music Genre Classification**, *Course Project for Machine Learning*, Java, Weka, 1000 lines. I implemented an algorithm flow that automatically classifies music genres from songs.

3/2011–1/2012 Algorithms for Routing Reliability Problem, Research, C++, BGL, 2000 lines.

We developed a two-stage algorithm for Routing Reliability Problem. The 1st stage generates a set of candidate augmenting segments, The 2nd stage optimally selects the segments by dynamic programming.

11/2010–3/2011 Large-scale Powergrid Simulation, Research, C++, UMFPACK, 3000 lines.

Developed a powergrid simulator that can solve powergrid in the scale of millions of nodes in minutes.

8/2008-5/2010 Physical design algorithms for biochips, Research, C++, 3000 lines.

I designed a graph-coloring based routing algorithm that routes droplet in cross-referencing biochips without cross-contamination; and a ILP-based placement algorithm that solves 3D placement for biochips.

1/2009–1/2010 Clock Network Synthesis, Research, C++, 10000 lines.

We developed a clock network synthesis algorithm that is robust against process variation. Our team won the 2nd and 4th places in ISPD 2010 and 2009 Clock Network contest, respectively.

Selected Courses

- ECE490 Introduction to Optimization (A+) CS543 Computer Vision (A+)
- ECE425 Intro to VLSI System Design (A+)
- CS446 Machine Learning
- CS598CSC Approximation Algorithms
- ECE582 Physical VLSI Design
- CS573 Algorithms (Graduate)
- ECE552 Numerical Circuit Analysis
- UPCRC 2011 Parallel Programming Summer School
- CEG5270 CAD for Physical Design
- CEG5330 Logic Synthesis and Testing
- CSC5240 Combinatorial Search & Optimization CSC5350 Game Theory in Computer Science

Professional Service

Reviewer, IEEE Transaction on CAD of Integrated Circuits and Systems (TCAD), ACM Transactions on Design Automation of Electronic Systems (TODAES), Integration: the VLSI Journal.

Honors and Awards

- 2010 Second place in ISPD 2010 High Performance Clock Network Synthesis Contest
- 2009 Fourth place in ISPD 2009 Clock Network Synthesis Contest
- 2008 SYSU Outstanding Graduate Award, Outstanding Thesis Award
- 2008 First places in Guangdong and SYSU Computer Programming Contest (GDCPC '08, ZSUCPC '08)
- 2007, 2006, 2005 First place in Academic Excellence Award in SYSU (top 5%)
 - 2006 Third place in SYSU Computer Programming Contest (ZSUCPC '06)