Zigang Xiao (Ivan)

Curriculum Vitae (as of February 12, 2014)

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Education

8/2010–present	**Ph.D. Candidate**, Department of Electrical and Computer Engineering, University of Illinois at Urbana-Champaign (UIUC), Urbana, IL, USA. [GPA: **3.87/4.0**]
8/2008–8/2010	**Master of Philosophy**, Department of Computer Science and Engineering, The Chinese University of Hong Kong (CUHK), Hong Kong. [GPA: **3.9/4.0**]
9/2004–7/2008	**Bachelor of Science**, Department of Computer Science, Sun Yat-Sen University (SYSU), Guangzhou, China. [GPA: **3.9/4.0**, Ranking: **1/200**, with outstanding honor]

Professional Skills

- Languages (proficient): C/C++, matlab, Python, Bash scripting
- Languages (prior experience): Java, Obj-C, Ruby, Lua, JavaScript & HTML, x86 asm
- Softwares: gcc, gdb, make, cmake, git, vim, awk, sed, grep, Visual Studio, Eclipse
- Operating systems: Linux, Mac OSX, Windows

Industrial Experience

5/2013–8/2013	**R&D Engineer**, *Synopsys Inc.*, 700 E Middlefield Rd, Mountain View, CA 94043. Work in Zroute Team of Implementation Group. Research and develop of IC Compiler.
5/2012–8/2012	**CAD Engineer**, *NVIDIA Corporation*, 2701 San Tomas Expressway, Santa Clara, CA 95050. Work in DFT/CAD Team. Develop internal tools for scan chain flow.
3/2008–6/2008	**Software Designer Intern**, *Ericsson Mobile Data Applications Technology Research and Development (Guangzhou) Co., Ltd. (CGC)*, Guangzhou, China. Research and development of PKI/CA system.

Teaching Experience

1/2013–current	**Teaching Assistant**, *Department of CS, UIUC*, Urbana, IL. MOOC course: *VLSI CAD: Logic to Layout*. Available online at www.coursera.org/course/vlsicad. Taught by Prof. Rob Rutenbar, head of CS department. More than 17, 000 students registered in 2013.
1/2012–current	**Teaching Assistant**, *Department of ECE, UIUC*, Urbana, IL. - ECE 425 (FA 12/13), Intro to VLSI Sys. Design - ECE 411 (SP '11), Computer Architecture
8/2008–8/2010	**Teaching Assistant**, *Department of CSE, CUHK*, Hong Kong. - CSC 3120 (SP '10), Compiler Construction - CSC 3190 (FA '09), Discrete Math and Algos - CSC 4430 (SP '08), Computer Networks - CSC 3150 (FA '08), Intro to Operating System

Research Experience

current	**CAD for Direct Self-Assembly (DSA)**, *three conference papers published*. We proposed a methodology for DSA template verification and algorithms for DSA cut redistrubtion and DSA contact optimization problems.

current	**Self-Aligned Double Patterning layout decomposition**, *two conferences and one journal*.
	- We proposed a graph coloring based algorithm that optimally finds a no-overlay decomposition in polynomial time, while previous approaches adopted exponential time methods.
	- We further propose an algorithm that utilizes the characteristics of standard cell row-based layout and solves the problem efficiently in polynomial time.
current	**Triple patterning decomposition for row-based layout**, *two conference papers published*.
	Triple Patterning Lithography layout decomposition is NP-hard general. Nevertheless, we showed that standard cell based layout is polynomial time solvable and proposed a polynomial time algorithm that optimally finds all stitch-free decompositions. A color balancing scheme is suggested to ensure a balanced decomposition.
3/2011-1/2012	**Algorithms for Routing Reliability Problem**, *one conference paper published*.
	An efficient algorithm is proposed for Routing Reliability Problem. The experimental results show that our algorithm can improve the reliability of the networks to 94.17% on average (67.93% previously).
11/2010-3/2011	**Large-scale Powergrid Simulation**, *one conference paper published*.
	Developed a powergrid simulator that can solve powergrid up to hundreds of millions in minutes.
8/2008-5/2010	**Physical design algorithms for biochips**, *two conference and one journal papers published*.
	- A droplet routing algorithm is implemented. Our method can route all test cases successfully while previous work cannot. A 4% reduction on runtime and a 58% reduction on routing time are achieved.
	- A placement algorithm is designed and implemented. By using our routing method, an average improvement of 29% and 46% in the average routing time and cell usage can be achieved.
1/2009-1/2010	**Clock Network Synthesis**, *one conference paper published*.
	A mesh-tree hybrid clock distribution network algorithm that aim to be robust under process variation is designed and implemented. Our team won the 2nd and 4th places in ISPD 2010 and 2009 Clock Network contest, respectively.

Professional Service

Reviewer, *IEEE Transaction on CAD of Integrated Circuits and Systems (TCAD), ACM Transactions on Design Automation of Electronic Systems (TODAES), Integration: the VLSI Journal*.

Selected Courses

- ECE490 Introduction to Optimization (A+)
- CS543 Computer Vision (A+)
- ECE425 Intro to VLSI System Design (A+)
- CS446 Machine Learning
- CS598CSC Approximation Algorithms
- ECE582 Physical VLSI Design
- CS573 Algorithms (Graduate)
- ECE552 Numerical Circuit Analysis
- UPCRC 2011 Parallel Programming Summer School
- CEG5270 CAD for Physical Design
- CEG5330 Logic Synthesis and Testing
- CSC5240 Combinatorial Search & Optimization
- CSC5350 Game Theory in Computer Science

Honors and Awards

2010	Second place in ISPD 2010 High Performance Clock Network Synthesis Contest
2009	Fourth place in ISPD 2009 Clock Network Synthesis Contest
2008	Outstanding Graduate Award in SYSU
2008	Excellent Bachelor's Thesis Award in SYSU
2008	First place in Guangdong Computer Programming Contest (GDCPC '08)
2008	First place in SYSU Computer Programming Contest (ZSUCPC '08)
2007, 2006, 2005	First place in Academic Excellence Award in SYSU (top 5%)
2006	Third place in SYSU Computer Programming Contest (ZSUCPC '06)