

Zigang Xiao

Curriculum Vitae (as of October 25, 2012)

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Education

- 8/2010–present **Ph.D. Candidate**, Department of Electrical and Computer Engineering, University of Illinois at Urbana-Champaign (UIUC), Urbana, IL, USA. [GPA: **3.87/4.0**]
- 8/2008–8/2010 **Master of Philosophy**, Department of Computer Science and Engineering, The Chinese University of Hong Kong (CUHK), Hong Kong. [GPA: **3.9/4.0**]
- 9/2004–7/2008 **Bachelor of Science**, Department of Computer Science, Sun Yat-Sen University (SYSU), Guangzhou, China. [GPA: **3.9/4.0**, Ranking: **1/200**, with outstanding honor]

Research Experience

- current **Self-Aligned Double Patterning layout decomposition**, *one conference paper published*.
We propose a graph coloring based algorithm that optimally solves the problem in polynomial time, while previous approaches adopted exponential time methods.
- current **Triple patterning decomposition for row-based layout**, *one conference paper published*.
Triple Patterning Lithography layout decomposition is NP-hard general. Nevertheless, we show that standard cell based layout is polynomial time solvable. We propose a polynomial time algorithm that optimally finds all stitch-free decompositions. A color balancing scheme is suggested to ensure a balanced decomposition.
- 3/2011-1/2012 **Algorithms for Routing Reliability Problem**, *one conference paper published*.
An efficient algorithm is proposed for Routing Reliability Problem. The experimental results show that our algorithm can improve the reliability of the networks to 94.17% on average (67.93% previously).
- 11/2010-3/2011 **Large-scale Powergrid Simulation**, *one conference paper published*.
Developed a powergrid simulator that can solve powergrid up to hundreds of millions in minutes.
- 8/2008-5/2010 **Physical design algorithms for biochips**, *two conference and one journal papers published*.
 - A droplet routing algorithm is implemented. Our method can route all test cases successfully while previous work cannot. A 4% reduction on runtime and a 58% reduction on routing time are achieved.
 - A placement algorithm is designed and implemented. By using our routing method, an average improvement of 29% and 46% in the average routing time and cell usage can be achieved.
 - Two conference papers and one journal paper were published.
- 1/2009-1/2010 **Clock Network Synthesis**, *one conference paper published*.
A mesh-tree hybrid clock distribution network algorithm that aim to be robust under process variation is designed and implemented. Our team won the 2nd and 4th places in ISPD 2010 and 2009 Clock Network contest, respectively. The result was published in ICCAD '10. My contributions:
 - Design and implement the block-aware rectilinear routing for the clock network and mesh-tree topology.
 - Write automation scripts of result evaluation.

Teaching Experience

- 1/2012–current **Teaching Assistant**, *Department of ECE, UIUC, Urbana, IL*.
 - ECE 425 (Fall 2012), Introduction to VLSI System Design
 - ECE 411 (Spring 2011), Computer Architecture

- 8/2008–8/2010 **Teaching Assistant**, *Department of CSE, CUHK*, Hong Kong.
- CSC 3120 (Spring 2010), Compiler Construction
 - CSC 3190 (Fall 2009), Introduction to Discrete Mathematics and Algorithms
 - CSC 4430 (Spring 2008), Data Communication and Computer Networks
 - CSC 3150 (Fall 2008), Introduction to Operating Systems

Industrial Experience

- 5/2012–8/2012 **CAD Engineer**, *NVIDIA Corporation*, 2701 San Tomas Expressway, Santa Clara, CA 95050.
Work in DFT/CAD Team. Develop internal tools for scan chain flow.
- 3/2008–6/2008 **Software Designer Intern**, *Ericsson Mobile Data Applications Technology Research and Development (Guangzhou) Co., Ltd. (CGC)*, Guangzhou, China.
Research and development of PKI/CA system.

Professional Service

- 2011 **Reviewer**, *IEEE Transaction on CAD of Integrated Circuits and Systems (TCAD)*.

Programming Languages and Computer Skills

- Languages (proficient): C/C++, matlab, Python, Bash scripting
- Languages (prior experience): Java, Obj-C, Ruby, Lua, JavaScript & HTML, x86 asm
- Libraries: Boost, Weka, CGAL, CUDA, Intel TBB, OpenMP, OpenGL
- Softwares: gcc, gdb, make, cmake, git, vim, awk, sed, grep, Visual Studio, Eclipse
- Operating systems: Linux, Mac OSX, Windows

Selected Projects

- Pwntcha (fork): A de-captcha program originally designed by Sam Hocevar. It is used to break captchas in websites such as paypal, slashdot. Implemented in C with OpenCV.
- zspice: A lightweight circuit simulator. Reads HSPICE file, supports DC, transient and small signal analysis. Solving a DC circuit of 10k elements uses less than 0.01s. Implemented in C++ with UMFPAK.

Selected Courses

- ECE490 Introduction to Optimization (A+) - CS543 Computer Vision (A+)
- ECE425 Intro to VLSI System Design (A+) - CS446 Machine Learning
- CS598CSC Approximation Algorithms - ECE582 Physical VLSI Design
- CS573 Algorithms (Graduate) - ECE552 Numerical Circuit Analysis
- UPCRC 2011 Parallel Programming Summer School
- CEG5270 CAD for Physical Design - CEG5330 Logic Synthesis and Testing
- CSC5240 Combinatorial Search & Optimization - CSC5350 Game Theory in Computer Science

Honors and Awards

- 2010 Second place in ISPD 2010 High Performance Clock Network Synthesis Contest
- 2009 Fourth place in ISPD 2009 Clock Network Synthesis Contest
- 2008 Outstanding Graduate Award in SYSU
- 2008 Excellent Bachelor's Thesis Award in SYSU
- 2008 First place in Guangdong Computer Programming Contest (GDCPC '08)
- 2008 First place in SYSU Computer Programming Contest (ZSUCPC '08)

2007, 2006, 2005 First place in Academic Excellence Award in SYSU (top 5%)
2006 Third place in SYSU Computer Programming Contest (ZSUCPC '06)

Publications

- [1] Q. Ma, **Xiao, Z.**, and M.D.F. Wong. Algorithmic study on the routing reliability problem. In *Proceedings of IEEE International Symposium on Quality Electronic Design (ISQED'12)*, 2012. (**Best Paper Award Nomination**).
- [2] Ting Yu, **Xiao, Z.**, and M.D.F. Wong. Efficient parallel power grid analysis via additive schwarz method. In *International Conference On Computer-Aided Design (ICCAD'12)*, 2012.
- [3] H. Tian, H. Zhang, Q. Ma, **Xiao, Z.**, and M.D.F. Wong. A polynomial time triple patterning algorithm for cell based row-structure layout. In *International Conference On Computer-Aided Design (ICCAD'12)*, 2012.
- [4] **Xiao, Z.**, Y. Du, H. Zhang, and M.D.F. Wong. A polynomial time exact algorithm for self-aligned double patterning layout decomposition. In *Proceedings of the 2012 ACM international symposium on International Symposium on Physical Design*, pages 17–24. ACM, 2012.
- [5] **Xiao, Z.** and E.F.Y. Young. Placement and routing for cross-referencing digital microfluidic biochips. *Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on*, 30(7):1000–1010, july 2011.
- [6] Q. Yang, **Xiao, Z.**, and David YL Wu. Improving redundancy addition and removal using unreachable states. In *Proceeding of International Symposium on Circuits and Systems, ISCAS'10*, May 2010.
- [7] L. Xiao, **Xiao, Z.**, Y. Jiang, Z. Qian, H. Tian, and E.F.Y. Young. Local clock skew minimization using blockage-aware mixed tree-mesh clock network. In *International Conference On Computer-Aided Design (ICCAD'10)*, 2010.
- [8] **Xiao, Z.** and E.F.Y. Young. Droplet-routing-aware module placement for cross-referencing biochips. In *Proceeding of International Symposium on Physical Design, ISPD'10*, March 2010.
- [9] **Xiao, Z.** and E.F.Y. Young. Crossrouter: A droplet router for cross-referencing digital microfluidic biochips. In *Proceeding of 15th Asia and South Pacific Digital Automation Conference, ASP-DAC'10*, January 2010.