PREPARED BY: DATE	SHARP	SPEC No. LCY-W-07806C
		FILE No.
APPROVED BY: DATE	MOBILE LIQUID CRYSTAL DISPLAY GROUP SHARP CORPORATION	ISSUE . Nov.20.2007
		PAGE Pages 29
		APPLICABLE DIVISION MOBILE LCD CHINA DESIGN CENTER WUXI SHARP

SPECIFICATION

DEVICE SPECIFICATION for

TFT LCD Module

(320 × RGB × 240 dots)

Model No.

LQ035Q1DG01

☐CUSTOMER'S APPROVAL

DATE _____

BY _____

PRESENTED BY K. Yamamoto

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RECORDS OF REVISION			DOC. First issue	Nov. 20. 2007
			Model No.	LQ035Q1DG01
			Spec. No.	LCY-W-07806C

DATE	REF.PAGE PARAGRAPH DRAWING No.	REVISED NO.	SUMMARY	CHECK AND APPROVAL
2007.8.24	—	—	First Issue	K.Yamamoto
2007.8.29	19	1	Viewing angle range change	K.Yamamoto
2007.11.12	4	2	Change symbol name of pin 52	K.Yamamoto
	4		Add notice 2	
	6		Add VDD/AVDD in 6-1.TFT LCD Panel Driving	
	7		Change Register setting ; gamma setting	
	11,12		Add formula of setting for control signal	
2007.11.20	7	3	Change register setting	K-Yamamoto

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1. Applicable Scope

This specification is applicable to TFT-LCD Module “LQ035Q1DG01”.

2. General Description

This module is a color active matrix LCD module incorporating amorphous silicon TFT (Thin Film Transistor). It is composed of a color TFT-LCD panel, driver IC, Input FPC, and a back light unit.

Graphics and texts can be displayed on a 320 × RGB × 240 dots panel with about 262k colors by supplying 18bit data signals (6bit × RGB), four timing signals, 3wires 9bit serial interface signals, logic (Typ. +3.3V), analog (Typ. +3.3V) supply voltages for TFT-LCD panel driving and supply voltage for back light.

3. Mechanical (Physical) Specifications

Item	Specifications	Unit
Screen size	8.8 (3.5” type) diagonal	cm
Active area	70.56 (H) × 52.92 (V)	mm
Pixel format	320 (H) × 240 (V)	pixel
	1 Pixel = R+G+B dots	-
Pixel pitch	0.2205 (H) × 0.2205 (V)	mm
Pixel configuration	R,G,B vertical stripes	-
Display mode	Normally white	-
Unit outline dimensions *	76.9(W) × 63.9 (H) × 3.5 (D)	mm
Mass	Approx. 36.1	g

*The above-mentioned table indicates module sizes without some projections and FPC.
For detailed measurements and tolerances, please refer to 18. Outline Dimensions.

4. Input Terminal Names and Functions

Recommendation CN：KYOCERA ELCO 6240 series(54pin/0.5mm pitch/Bottom contact)

Pin No.	Symbol	I/O	Description	Remarks
1	LED_C (-)	-	Power supply for LED (Low voltage)	
2	LED_C (-)	-	Power supply for LED (Low voltage)	
3	LED_A(+)	-	Power supply for LED (High voltage)	
4	LED_A(+)	-	Power supply for LED (High voltage)	
5	C6	-	Capacitor connection	
6	C5	-	Capacitor connection	
7	M	-	Non connection	Note 1
8	RESET	I	System reset	
9	CS	I	Chip select	
10	SCL	I	Clock input pin in serial mode	
11	SDI	I	Data input pin serial mode	
12	NC	-	Non connection	Note 1
13	NC	-	Non connection	Note 1
14	B0	I	BLUE data signal (LSB)	
15	B1	I	BLUE data signal	
16	B2	I	BLUE data signal	
17	B3	I	BLUE data signal	
18	B4	I	BLUE data signal	
19	B5	I	BLUE data signal (MSB)	
20	NC	-	Non connection	Note 1
21	NC	-	Non connection	Note 1
22	G0	I	GREEN data signal (LSB)	
23	G1	I	GREEN data signal	
24	G2	I	GREEN data signal	
25	G3	I	GREEN data signal	
26	G4	I	GREEN data signal	
27	G5	I	GREEN data signal (MSB)	
28	NC	-	Non connection	Note 1
29	NC	-	Non connection	Note 1
30	R0	I	RED data signal (LSB)	
31	R1	I	RED data signal	
32	R2	I	RED data signal	
33	R3	I	RED data signal	
34	R4	I	RED data signal	
35	R5	I	RED data signal(MSB)	
36	HSYNC	I	Line synchronization signal	
37	VSYNC	I	Frame synchronization signal	
38	DOTCLK	I	Dot-clock signal	
39	AVDD	-	Voltage input pin for analog	Note 2
40	AVDD	-	Voltage input pin for analog	Note 2
41	VDD	-	Voltage input pin for logic I/O	Note 2

42	VDD	-	Voltage input pin for logic I/O	Note 2
43	C4	-	Capacitor connection	
44	VGL	-	Voltage input VGOFF	Note 3
45	VGL	-	Voltage input VGOFF	Note 3
46	C3	-	Capacitor connection	
47	VGH	-	Voltage input VGON	Note 3
48	C2	-	Capacitor connection	
49	C1	-	Capacitor connection	
50	NC	-	Non connection	Note 1
51	NC	-	Non connection	Note 1
52	DEN	-	Data enable signal	
53	GND	-	Ground	
54	GND	-	Ground	

Note 1) An NC pins OPEN in FPC.

Note 2) Connect VDD to AVDD

Note 3) No use.

5. Absolute Maximum Ratings

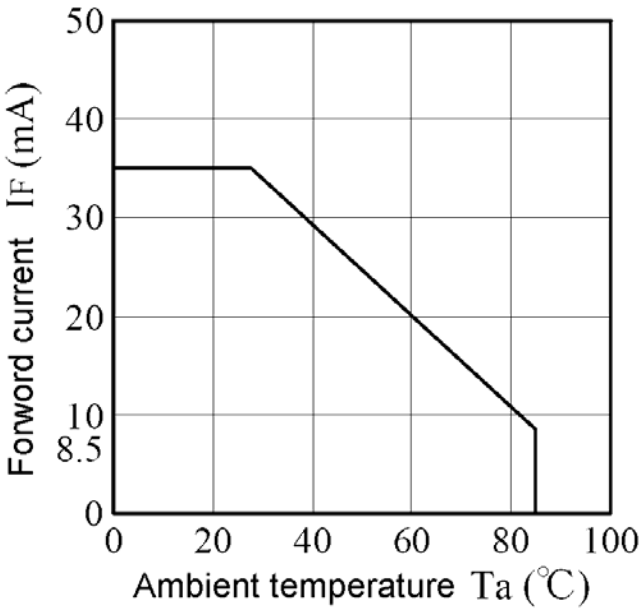
Item	Symbol	Conditions	Rated value	Unit	Remarks
Input voltage	VI	Ta = 25°C	-0.3 ~ VDD +0.3	V	Note 1
Analog power supply voltage	AVDD	Ta = 25°C	AGND-0.3 ~ +5.0	V	
Temperature for storage	Tstg	-	-20 ~ +70	°C	Note 2
Temperature for operation	Topr	-	-0 ~ +60	°C	Note 3
LED input electric current	I_{LED}	Ta = 25°C	35	mA	Note 4
LED electricity consumption	P_{LED}	Ta = 25°C	130	mW	Note 4

Note 1) RESB, CSB, SDI, SCK, B5~B0, G5~G0, R5~R0, VSYNC, HSYNC, DOTCLK

Note 2) Humidity: 80%RH Max. (Ta≦40°C)
Maximum bulb temperature under 39°C (Ta>40°C) See to it that no dew will be condensed.

Note 3) Panel surface temperature prescribes.
(Reliability is examined at ambient temperature of 50°C.)

Note 4) Power consumption of one LED (Ta = 25°C). (use 7 pieces LED)
Ambient temperature and the maximum input are fulfilling the following operating conditions.



Ambient temperature and the maximum input

6. Electrical Characteristics

6-1. TFT LCD Panel Driving

Ta = 25°C

Item		Symbol	Min.	Typ.	Max.	Unit	Remarks
Power supply	DC voltage	VDD/AVDD	+3.0	+3.3	+3.6	V	
	DC Current	I_{VDD} +I_{AVDD}	-	11.0	15.0	mA	Note 1
Permissive input ripple voltage		V_{RFAVDD} V_{RFVDD}	-	-	(100)	mVp-p	Note 2
Logic Input Voltage	High	V_{IH}	0.8 VDD	-	VDD	V	Note 3
	Low	V_{IL}	0	-	0.2 VDD	V	Note 3
Logic input Current		I_{IH} / I_{IL}	-1	-	1	μA	Note 3

Note 1) VDD = AVDD = +3.3V

Current situation for I_{VDDIO}: Black & White checker flag pattern

Current situation for I_{AVDD}: All black pattern

Note 2) VDD = AVDD = +3.3V

Note 3) RESB, CSB, SDI, SCK, B5~B0, G5~G0, R5~R0, VSYNC, HSYNC, DOTCLK

6-2. Register Setting△2

This register setting is for DOTCLK=5MHz. If LCD module is moved other frequency, please conform display quality.

	Reg. #	Register	Data (Gamma 2.2)	Remark
	R01 h	Driver output control	2AEF h	
	R02 h	LCD drive AC control	0300 h	
	R03 h	Power control (1)	7A7E h	
	R0B h	Frame cycle control	DC00 h	
	R0C h	Power control (2)	0005 h	
	R0D h	Power control (3)	0002 h	
	R0E h	Power control (4)	2C00 h	
	R0F h	Gate scan starting Position	0000 h	
	R16 h	Horizontal Porch	9F86 h	Note1
	R17 h	Vertical Porch	0002 h	Note2
△3	R1E h	Power control (5)	0000 h	
	R2E h	3 Gamma	B945 h	
	R30 h	Gamma control (1)	0000 h	
	R31 h	Gamma control (1)	0007 h	
	R32 h	Gamma control (1)	0300 h	
	R33 h	Gamma control (1)	0007 h	
	R34 h	Gamma control (1)	0705 h	
	R35 h	Gamma control (1)	0007 h	
	R36 h	Gamma control (1)	0707 h	
	R37 h	Gamma control (1)	0700 h	
	R3A h	Gamma control (2)	001F h	
	R3B h	Gamma control (2)	0F01 h	
△3	R28 h	External command	0006 h	
△3	R2C h	External command	C88C h	

Note 1)

Horizontal Porch (R16h) (POR = 9F86h)

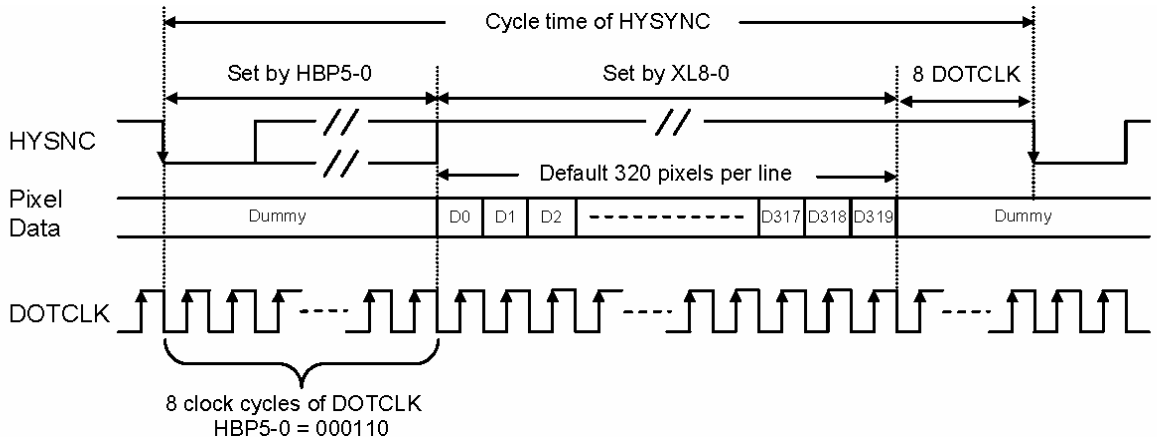
R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	XL8	XL7	XL6	XL5	XL4	XL3	XL2	XL1	XL0	0	HBP5	HBP4	HBP3	HBP2	HBP1	HBP0
POR		1	0	0	1	1	1	1	1	1	0	0	0	0	1	1	0

XL7-0: Set the number of valid pixel per line.

XL8	XL7	XL6	XL5	XL4	XL3	XL2	XL1	XL0	No. of pixel per line
0	0	0	0	0	0	0	0	0	1
0	0	0	0	0	0	0	0	1	2
0	0	0	0	0	0	0	1	0	3
:	:	:	:	:	:	:	:	:	: Step = 1 :
1	0	0	1	1	1	1	1	0	319
1	0	0	1	1	1	1	1	1	320
1	0	1	*	*	*	*	*	*	Reserved
1	1	*	*	*	*	*	*	*	Reserved

HBP5-0: Set the delay period from falling edge of HSYNC signal to first valid data. The pixel data exceed the range set by XL8-0 and before the first valid data will be treated as dummy data.

HBP5	HBP4	HBP3	HBP2	HBP1	HBP0	No. of clock cycle of DOTCLK
0	0	0	0	0	0	2
0	0	0	0	0	1	3
0	0	0	0	1	0	4
0	0	0	0	1	1	5
0	0	0	1	0	0	6
0	0	0	1	0	1	7
0	0	0	1	1	0	8
0	0	0	1	1	1	9
0	0	1	0	0	0	10
:	:	:	:	:	:	: Step = 1 :
1	1	1	1	1	0	64
1	1	1	1	1	1	65



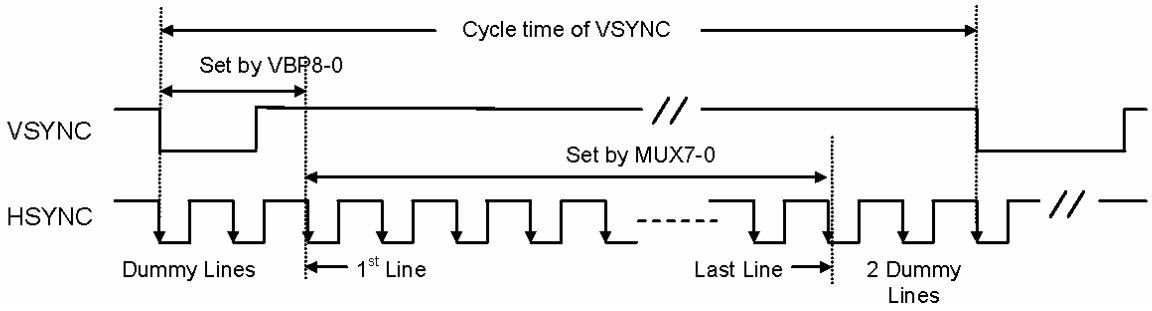
Note 2)

Vertical Porch (R17h) (POR = 0002h)

R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	VBP8	VBP7	VBP6	VBP5	VBP4	VBP3	VBP2	VBP1	VBP0
POR		0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

VBP7-0: Set the delay period from falling edge of VSYNC to first valid line. The line data within this delay period will be treated as dummy line.

VBP8	VBP7	VBP6	VBP5	VBP4	VBP3	VBP2	VBP1	VBP0	No. of clock cycle of HSYNC
0	0	0	0	0	0	0	0	0	0 (only allow when CAD=0)
0	0	0	0	0	0	0	0	1	1
0	0	0	0	0	0	0	1	0	2
0	0	0	0	0	0	0	1	1	3
0	0	0	0	0	0	1	0	0	4
				:					: Step = 1 :
1	0	0	1	1	1	1	1	0	319
1	0	0	1	1	1	1	1	1	320
1	0	1	*	*	*	*	*	*	Reserved
1	1	*	*	*	*	*	*	*	Reserved



6-3. Back light driving

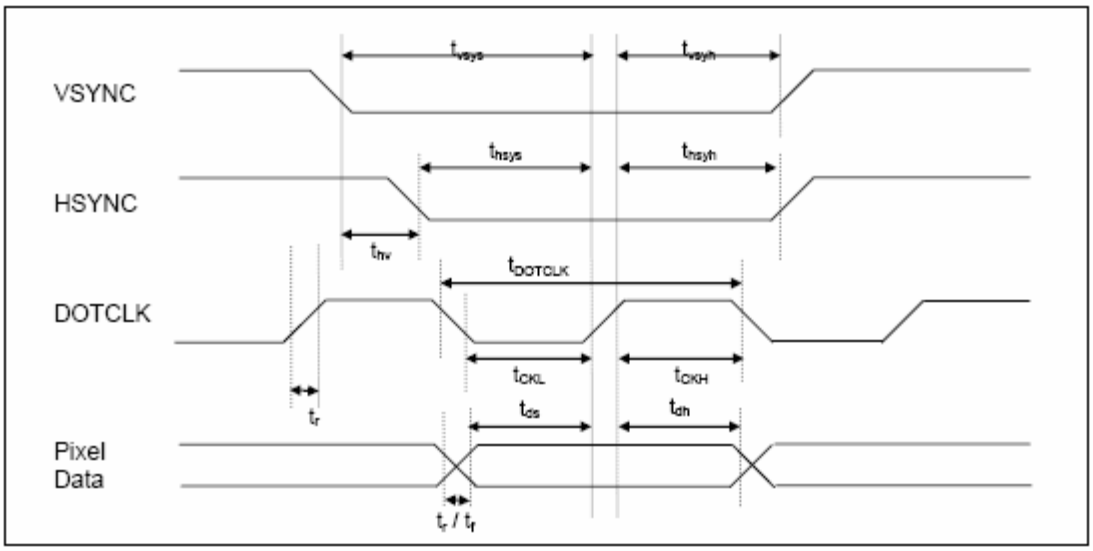
The back light system has 7 LEDs

[GM4BW63367A] made by SHARP

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
Rated Voltage	V_{BL}	-	22.4	24.5	V	
Rated Current	I_L	-	20	-	mA	Ta=25°C
Power consumption	W_L	-	448	-	mW	

7. Timing characteristics of input signals

7-1. Pixel Clock Timing

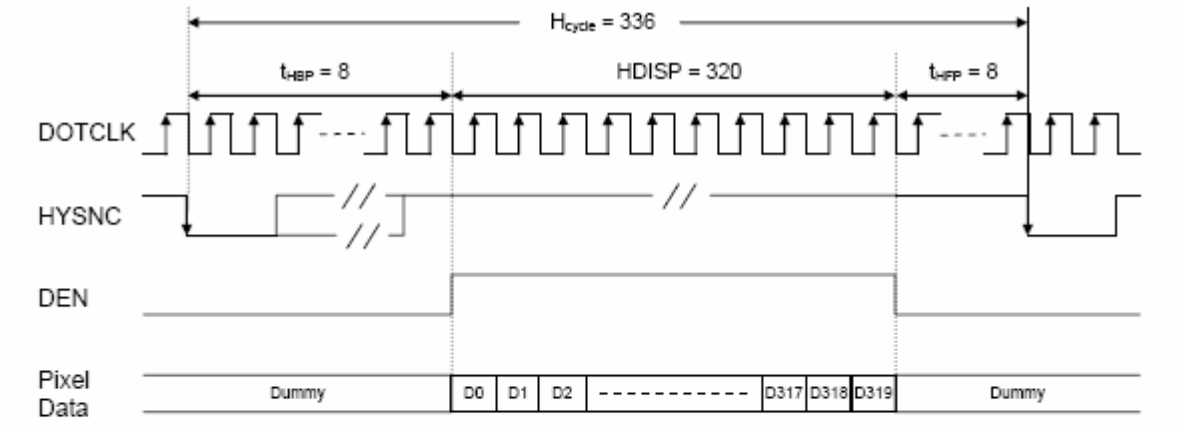


Pixel Clock Timing

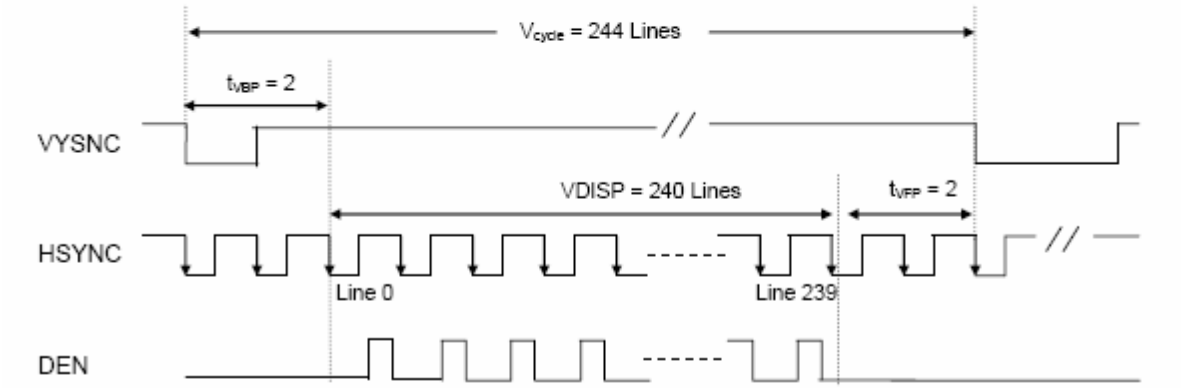
Characteristics	Symbol	Min	Typ	Max	Units
DOTCLK Frequency	f_{DOTCLK}	-	5.0	8.0	MHz
DOTCLK Period	t_{DOTCLK}	125	200	-	nSec
Vertical Sync Setup Time	t_{vsys}	20	-	-	nSec
Vertical Sync Hold Time	t_{vsyh}	20	-	-	nSec
Horizontal Sync Setup Time	t_{hsys}	20	-	-	nSec
Horizontal Sync Hold Time	t_{hsyh}	20	-	-	nSec
Phase difference of Sync Signal Falling Edge	t_{hv}	0	-	320	t_{DOTCLK}
DOTCLK Low Period	t_{CKL}	62	-	-	nSec
DOTCLK High Period	t_{CKH}	62	-	-	nSec
Data Setup Time	t_{ds}	40	-	-	nSec
Data hold Time	t_{dh}	40	-	-	nSec
Reset pulse width	t_{RES}	10	-	-	uSec
Rise / Fall time	t_r / t_f	20	-	100	nSec

Note: External clock source must be provided to DOTCLK pin of SSD2116Z. The driver will not operate if absent of the clocking signal.

7-2. Data Transaction Timing in Normal Operating Mode (262k color)



a) Horizontal Data Transaction Timing



b) Vertical Data Transaction Timing

Characteristics	Symbol	Min	Typ	Max	Unit
DOTCLK Frequency	f_{DOTCLK}	-	5.0	8.0	MHz
DOTCLK Period	t_{DOTCLK}	125	200	-	nSec
Horizontal Frequency (Line)	f_H	-	14.9	-	kHz
Vertical Frequency (Refresh)	f_V	-	60.1	-	Hz
Horizontal Back Porch	t_{HBP}	-	8	-	t_{DOTCLK}
Horizontal Front Porch	t_{HFP}	-	8	-	t_{DOTCLK}
Horizontal Data Start Point	t_{HBP}	-	8	-	t_{DOTCLK}
Horizontal Blanking Period	$t_{HBP}+t_{HFP}$	-	16	-	t_{DOTCLK}
Horizontal Display Area	HDISP	-	320	-	t_{DOTCLK}
Horizontal Cycle	H_{cycle}	-	336	-	t_{DOTCLK}
Vertical Back Porch	t_{VBP}	-	2	-	Line
Vertical Front Porch	t_{VFP}	-	2	-	Line
Vertical Data Start Point	t_{VBP}	-	2	-	Line
Vertical Blanking Period	$t_{VBP}+t_{VFP}$	-	4	-	Line
Vertical Display Area	VDISP	-	240	-	Line
Vertical Cycle	V_{cycle}	-	244	-	Line

⚠ The formula of setting for control signals: f_{DOTCLK}, t_{HBP}, t_{HFP}, t_{VBP}, t_{VFP}

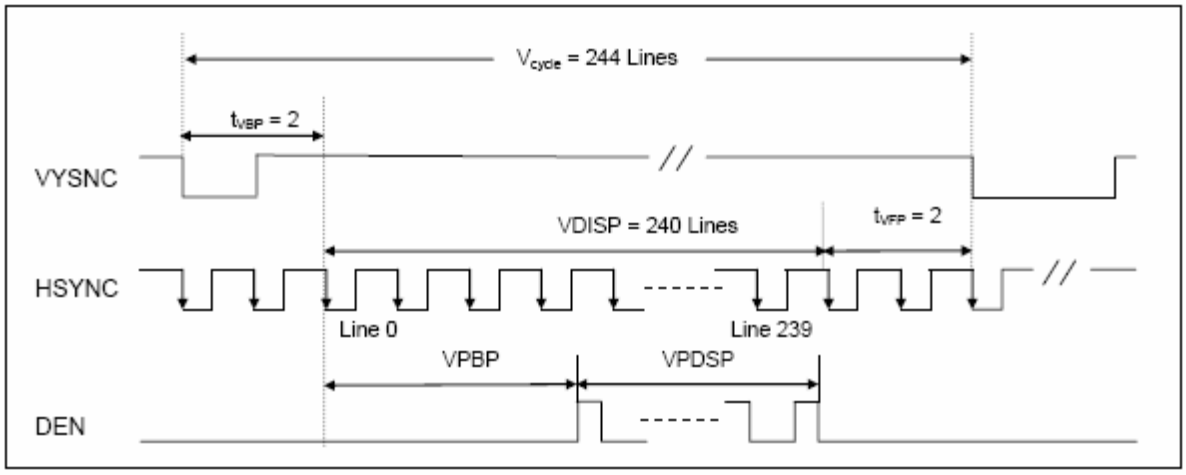
fv=60±5Hz

fv= f_{DOTCLK}/(V_{cycle}X H_{cycle})

V_{cycle}=240+ t_{VBP} + t_{VFP}

H_{cycle}=320+ t_{HBP}+ t_{HFP} ≦512

7-3. Synchronization Signals Timing in Power Save Mode (8 color)



Characteristics	Symbol	Min	Typ	Max	Units
DOTCLK Frequency	f_{DOTCLK}	-	5.0	8.0	MHz
DOTCLK Period	t_{DOTCLK}	125	200	-	nSec
Horizontal Frequency (Line)	f_H	-	14.9	-	kHz
Vertical Frequency (Refresh)	f_V	55	60	65	Hz
Vertical Partial Back Porch	VPBP	0	-	239	Line
Vertical Active Area	VPDSP	1	-	240	Line
Vertical Back Porch	t_{VBP}	-	2	-	Line
Vertical Front Porch	t_{VFP}	-	2	-	Line
Vertical Display Area	VDISP	-	240	-	Line
Vertical Cycle	V_{cycle}	-	244	-	Line

△2

Note: When entered to 8-color display mode, the RGB graphic data through the interface pins RR5, GG5 and BB5 are valid within the Vertical Active Area. Data "0" will be displayed outside the Vertical Active Area.

Synchronization Signals Timing in Power Save Mode (8 color)

△2 The formula of setting for control signals: f_{DOTCLK}, t_{HBP}, t_{HFP}, t_{VBP}, t_{VFP}

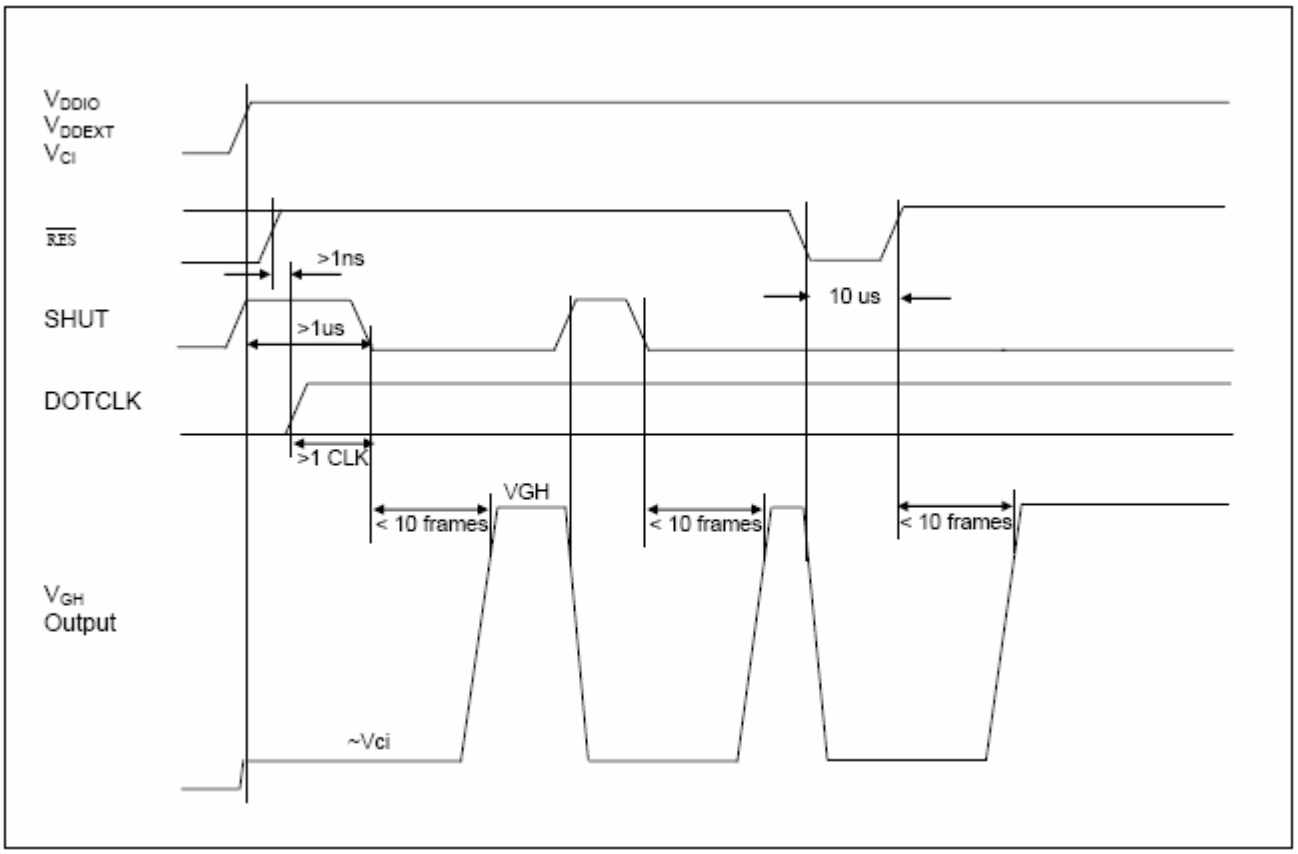
fv=60±5Hz

fv= f_{DOTCLK}/(V_{cycle}X H_{cycle})

V_{cycle}=240+ t_{VBP} + t_{VFP}

H_{cycle}=320+ t_{HBP}+ t_{HFP} ≦512

7-4. V_{GH} Output against SHUT & RESB



VGH Output against SHUT & RESB

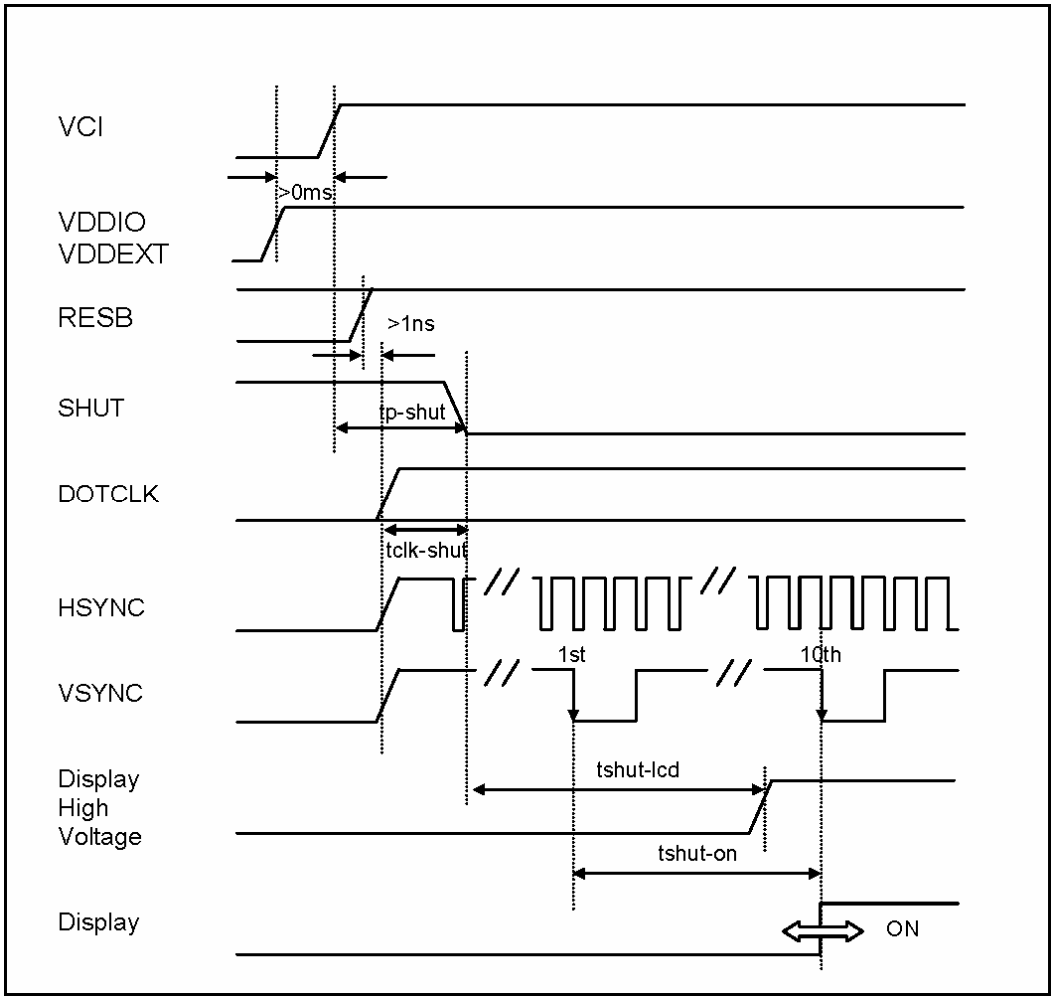
Note1: **The minimum cycle time of SHUT is 10 + 2 frames.**

Note2: **DOTCLK must be provided for boosting of V_{GH}. The above timing diagram assumed voltages and DOTCLK are continuous supplied after power on.**

Note3: **V_{GH} will be forced to V_{CI} at the low stage of $\overline{RES}$.**

Note4: **The minimum pulse width of RESET is 10us.**

7-5. Power Up Sequence

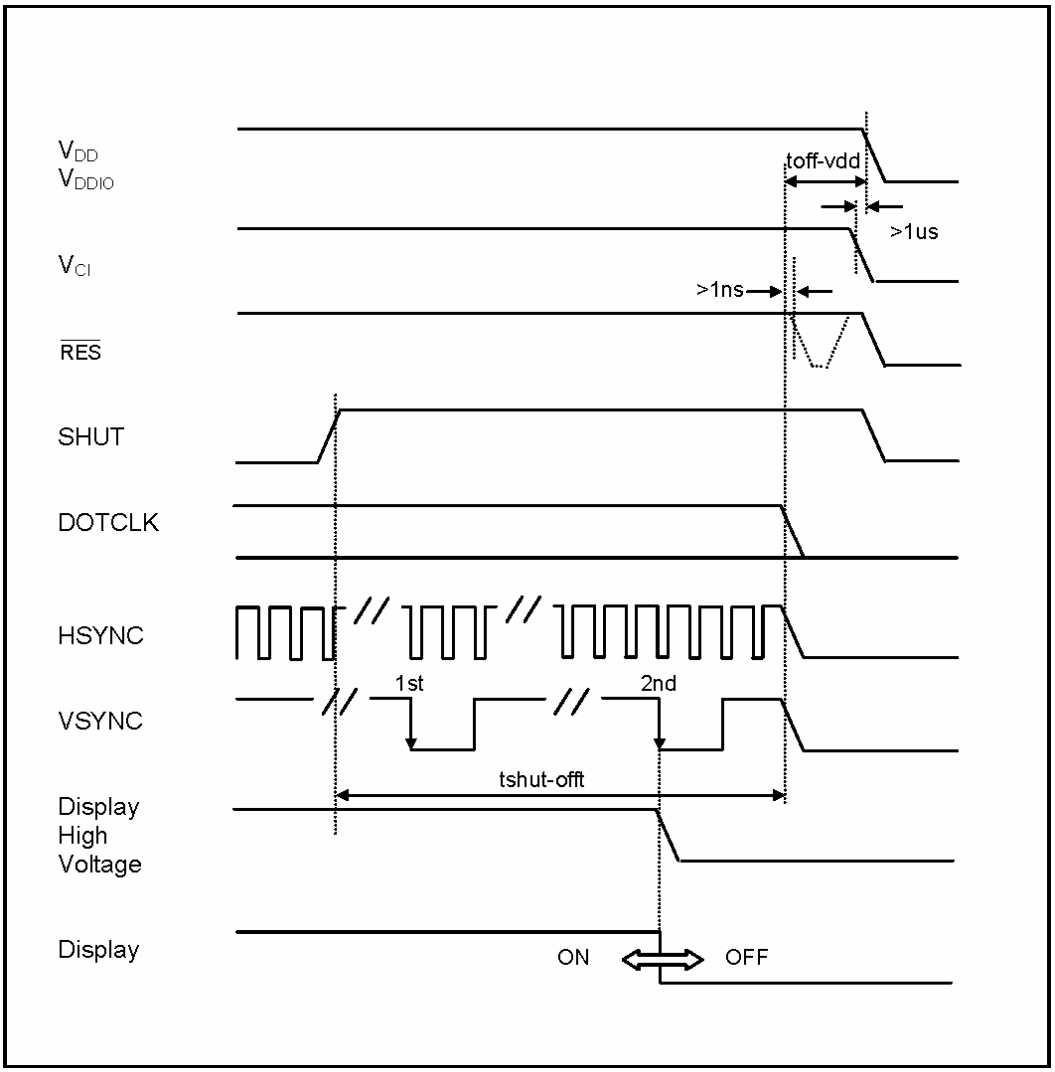


Characteristics	Symbol	Min	Typ	Max	Units
V_{DDEXT} / V_{DDIO} on to falling edge of SHUT	tp-shut	1	-	-	µsec
DOTCLK	tclk-shut	1	-	-	clk
Falling edge of SHUT to LCD power on	tshut-lcd	-	-	164	msec
Falling edge of SHUT to display start	tshut-on	-	-	10	frame
-- 1 line: 336 clk -- 1 frame: 244 line -- DOTCLK = 5.0MHz		-	164	-	msec

Note1: It is necessary to input DOTCLK before the falling edge of SHUT.

Note2: Display starts at 10th falling edge of VSTNC after the falling edge of SHUT.

7-6. Power Down Sequence



Characteristics	Symbol	Min	Typ	Max	Units
Rising edge of SHUT to display off -- 1 line: 336 clk -- 1 frame: 244 line -- DOTCLK = 5.0 MHz	tshut-off	2	-	-	frame
		32.8	-	-	msec
Input-signal-off to V_{DDEXT} / V_{DDIO} off	toff-vdd	1	-	-	µsec

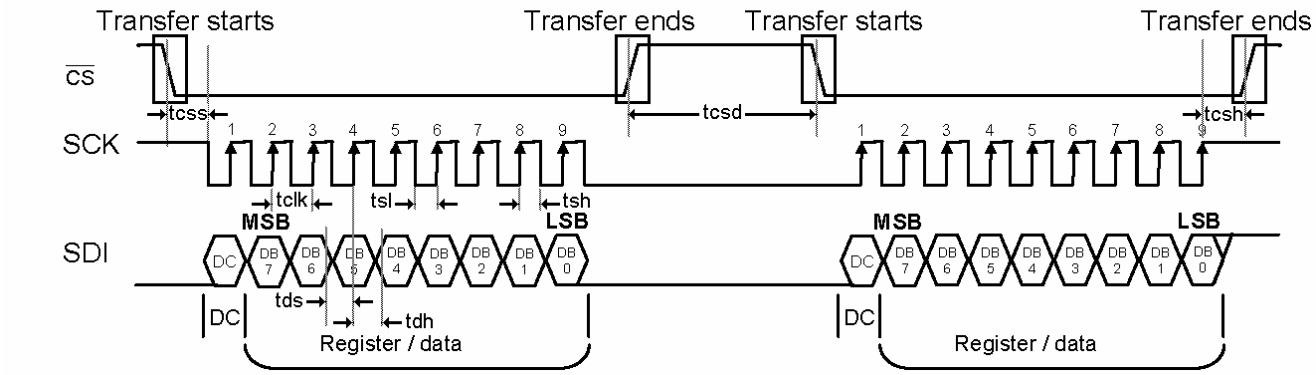
Note1: DOTCLK must be maintained at lease 2 frames after the rising edge of SHUT.

Note2: Display become off at the 2nd falling edge of VSTNC after the falling edge of SHUT.

Note3: If RESET signal is necessary for power down, provide it after the 2-frames-cycle of the SHUT period.

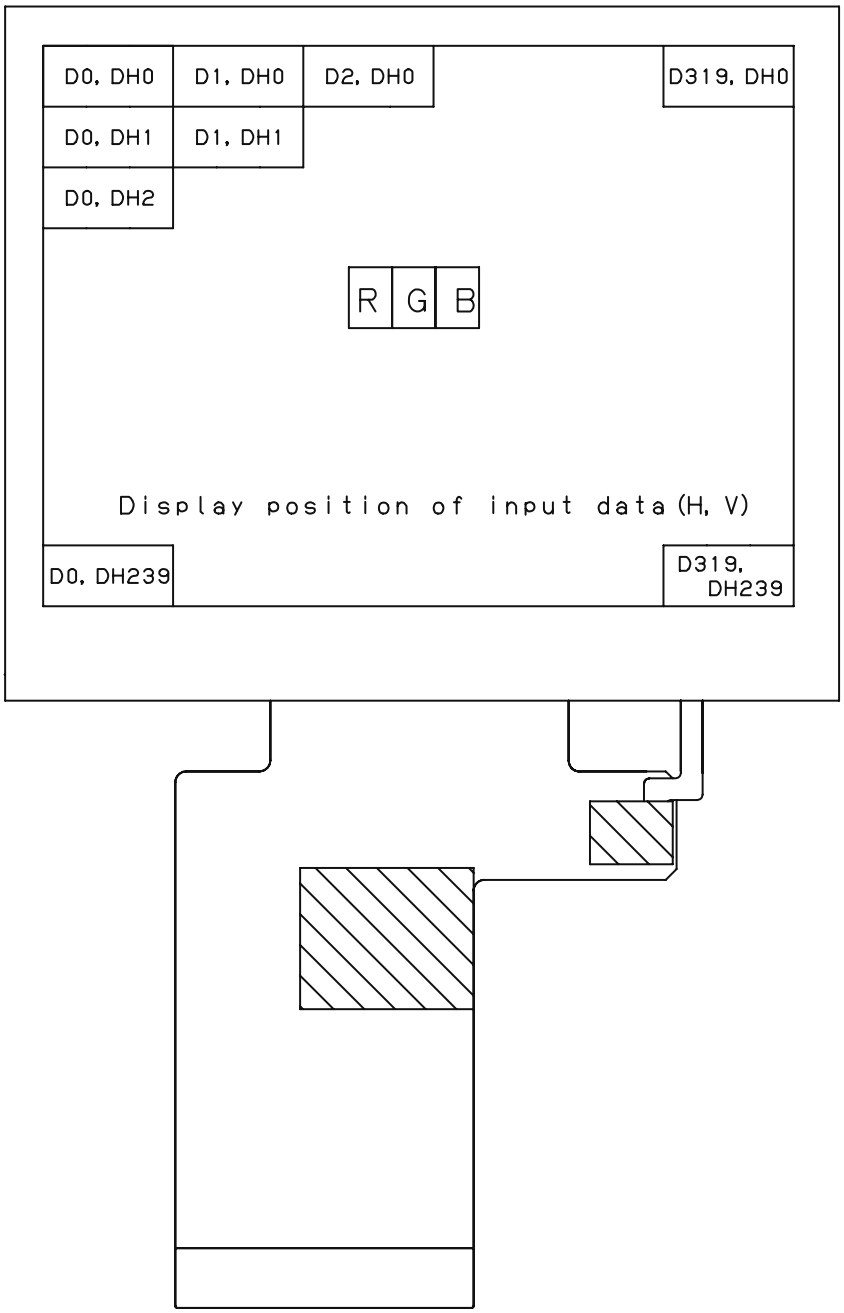
7-7. SPI Interface Timing Diagram & Transaction Example (9 bit)

The clock synchronized serial peripheral interface (SPI) using the chip select line (CSB), serial transfer clock line (SCK), serial input data (SDI). The serial data transfer starts at the falling edge of CSB input and ends at the rising edge of CSB. DC bit determinate the data of SDI which is register or data.



Characteristics	Symbol	Min	Typ	Max	Units
Serial Clock Frequency	fclk	-	-	20	MHz
Serial Clock Cycle Time	tclk	50	-	-	nsec
Clock Low Width	tsl	25	-	-	nsec
Clock High Width	tsh	25	-	-	nsec
Chip Select Setup Time	tcss	0	-	-	nsec
Chip Select Hold Time	tcsh	10	-	-	nsec
Chip Select High Delay Time	tcsd	20	-	-	nsec
Data Setup Time	tds	5	-	-	msec
Data Hold Time	tdh	10	-	-	nsec

7-8. Input Data Signals and Display Position on the screen



Please refer to Input Terminal Names and Functions

8. Input Signals, Basic Display Colors and Gray Scale of Each Color

	Colors & Gray Scale	Gray Scale	Date signal																	
			R0	R1	R2	R3	R4	R5	G0	G1	G2	G3	G4	G5	B0	B1	B2	B3	B4	B5
			LSB					MSB	LSB					MSB	LSB					MSB
Basic Color	Black	—	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue	—	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
	Green	—	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
	Cyan	—	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
	Red	—	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	Magenta	—	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1
	Yellow	—	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0
	White	—	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale of Red	Black	GS0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	⇧	GS1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Darker	GS2	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	⇧	↓				↓						↓						↓		
	⇩	↓				↓						↓						↓		
	Brighter	GS61	1	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	⇩	GS62	0	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	Red	GS63	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
Gray Scale of Green	Black	GS0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	⇧	GS1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
	Darker	GS2	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
	⇧	↓				↓						↓						↓		
	⇩	↓				↓						↓						↓		
	Brighter	GS61	0	0	0	0	0	0	1	0	1	1	1	1	0	0	0	0	0	0
	⇩	GS62	0	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0
	Green	GS63	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
Gray Scale of Blue	Black	GS0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	⇧	GS1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
	Darker	GS2	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
	⇧	↓				↓						↓						↓		
	⇩	↓				↓						↓						↓		
	Brighter	GS61	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	1
	⇩	GS62	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1
	Blue	GS63	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1

0: Low level voltage, 1: High level voltage

Each basic color can be displayed in 64 gray scales from 6 bit data signals.
According to the combination of 18 bit data signals, the 262k color display can be achieved on the screen.

9. Optical Characteristics ⚠1

Ta = 25°C, VDD/AVDD = +3.3V

Parameter		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Viewing angle range (Without Wide View)	Horizontal	θ21	CR＞10	-	60	-	deg.	【Note1,4】
		θ22		-	60	-	deg.	
	Vertical	θ11		-	40	-	deg.	
		θ12		-	60	-	deg.	
Contrast ratio		CR	Optimum viewing angle	100	300	-	-	【Note2,4】
Response Time	Rise	Tr	θ=0°	-	30	45	ms	【Note3,4】
	Decay	Td		-	30	45	ms	
Chromaticity of White		x		0.27	0.32	0.37	-	【Note4】
		y		0.28	0.33	0.38	-	
Luminance of white		X_{L1}		240	340	-	cd/m²	I_{LED}=20mA 【Note6】
Uniformity		U		70	80	-	%	【Note5】

* The optical characteristics measurements are operated under a stable luminescence (I_{LED} = 20mA) and a dark condition. (Refer to Fig.9-1)

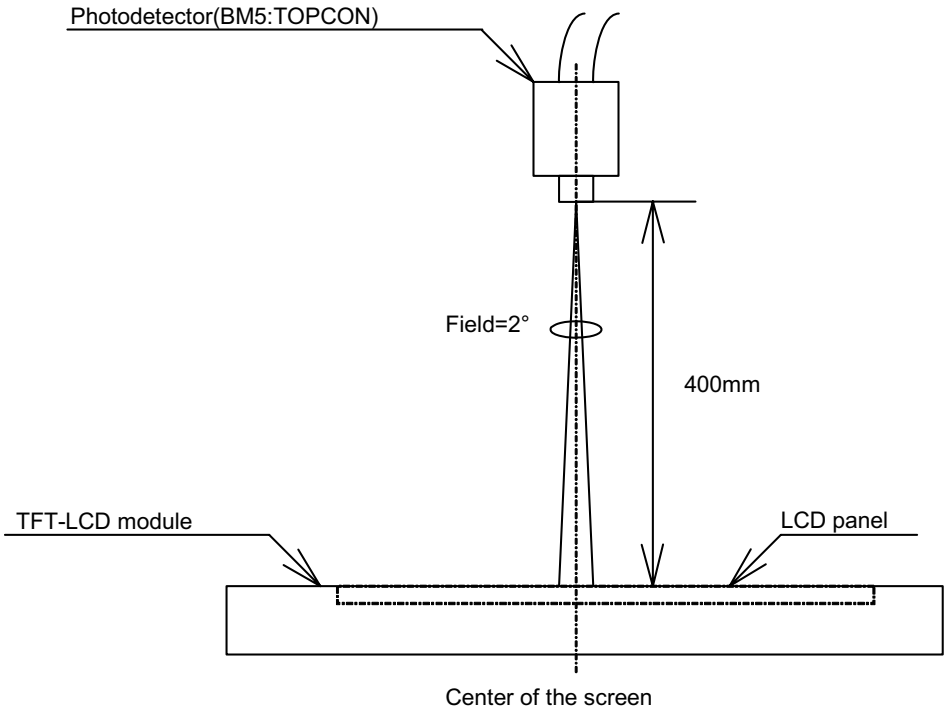
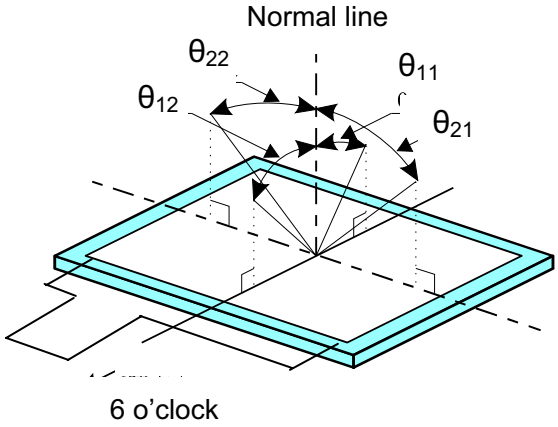


Fig.9-1 Optical characteristics measurement method

【 Note 1 】Definitions of viewing angle range



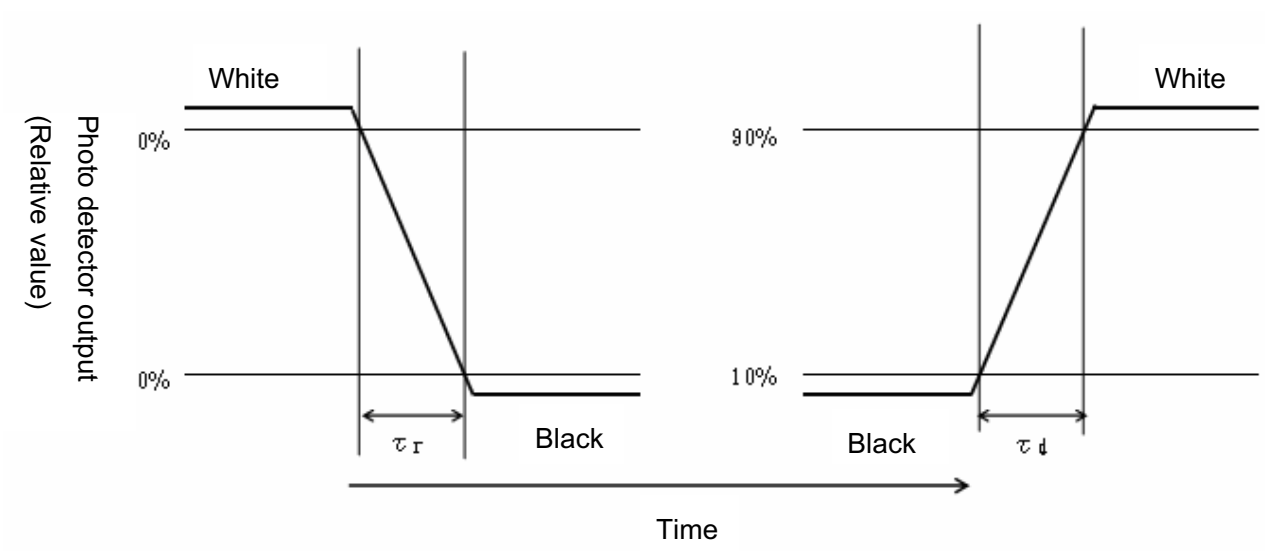
【 Note 2 】Definition of contrast ratio

The contrast ratio is defined as the following

$$\text{Contrast ratio (CR)} = \frac{\text{Luminance (brightness) with all pixels white}}{\text{Luminance (brightness) with all pixels black}}$$

【 Note 3 】Definition of response time

The response time is defined as the following figure and shall be measured by switching the input signal for “Black” and “White”

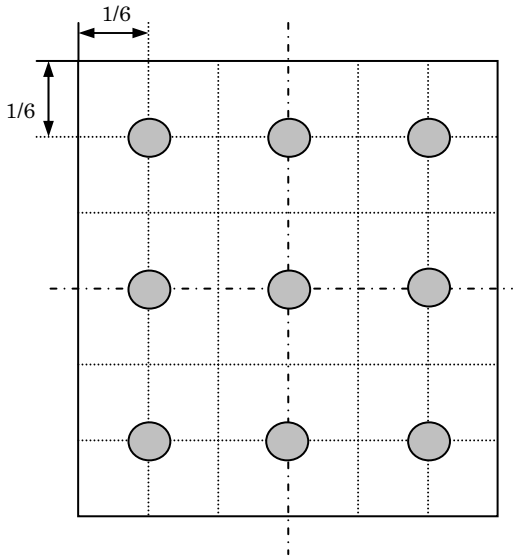


【 Note 4 】This shall be measured at center of the screen.

【 Note 5 】Definition of Uniformity

$$\text{Uniformity} = \frac{\text{Minimum Brightness}}{\text{Maximum Brightness}} \times 100\,(\%)$$

The brightness should be measured on the 9-point as shown in the right figure.



【 Note 6 】This shall be measured on the 9-point as shown in the right figure.

$$\text{Luminance of white} = \frac{\text{Summation of the 9 - point Brightness}}{9}$$

10. Handling of modules

10-1. Inserting the FPC into its connector and pulling it out

1) Be sure to turn off the power supply and the signals when inserting or disconnecting the cable.
2) Please insert for too much stress not to join FPC in the case of insertion of FPC.

10-2. About handling of FPC

1) The bending radius of the FPC should be more than 1.4mm, and it should be bent evenly.
2) Do not dangle the LCD module by holding the FPC, or do not give any stress to it.

10-3. Mounting of the module

1) The module should be held on to the plain surface. Do not give any warping or twisting stress to the module.
2) Please consider that GND can ground a modular metal portion etc. so that static electricity is not charged to a module.

10-4. Cautions in assembly / Handling pre cautions

As the polarizer can be easily scratched, be most careful in handling it.

1) Work environments in assembly.
   Working under the following environments is desirable:
   a) Implement more than 1MΩ conductive treatment (by placing a conductive mat or applying conductive paint) on the floor or tiles.
   b) No dusts come in to the working room. Place an adhesive, anti-dust mat at the entrance of the room.
   c) Humidity of 50 to 70% and temperature of 15 to 27°C are desirable.
   d) All workers wear conductive shoes, conductive clothes, conductive fingerstalls and grounding belts without fail.
   e) Use a blower for electrostatic removal. Set it in a direction slightly tilt downward so that each Module can be well subjected to its wind. Set the blower at an optimum distance between the blower and the module.
2) How the remove dust on the polarizer
   a) Blow out dust by the use of an N2 blower with antistatic measures taken. Use of an ionized air Gun is recommendable.
   b) When the panel surface is soiled, wipe it with soft cloth.
3) In the case of the module's metal part (shield case) is stained, wipe it with a piece of dry, soft cloth.
   If rather difficult, give a breath on the metal part to clean better.

4) If water dropped, etc. remains stuck on the polarizer for a long time, it is apt to get discolored or cause stains. Wipe it immediately.
5) As a glass substrate is used for the TFT-LCD panel, if it is dropped on the floor or hit by something hard, it may be broken or chipped off.
6) Since CMOS LSI is used in this module, take care of static electricity and take the human earth into consideration when handling.

10-5. Others

1) Regarding storage of LCD modules, avoid storing them at direct sunlight-situation.
   You are requested to store under the following conditions:
   (Environmental conditions of temperature/humidity for storage)
   a) Temperature: 0 to 40°C
   b) Relative humidity : 95% or less
      As average values of environments (temperature and humidity) for storing, use the following control guidelines:
      Summer season: 20 to 35°C, 85% or less Winter season: 5 to 15°C, 85% or less
      If stored under the conditions of 40°C and 95% RH, cumulative time of storage must be less than 240 hours.
2) If stored at temperatures below the rated values, the inner liquid crystal may freeze, causing cell destruction. At temperatures exceeding the rated values for storage, the liquid crystal may become isotropic liquid, making it no longer possible to come back to its original state in some cases.
3) If the LCD is broken, do not drink liquid crystal in the mouth. If the liquid crystal adheres to a hand or foot or to clothes, immediately cleanse it with soap.
4) If a water drop or dust adheres to the polarizer, it is apt to cause deterioration. Wipe it immediately.
5) Be sure to observe other caution items for ordinary electronic parts and components.

11. Reliability test items

No.	Test item	Conditions
1	High temperature storage test	Ta = 70°C 240h
2	Low temperature storage test	Ta = -25°C 240h
3	High temperature & high humidity operation test	Ta = 40°C ; 95%RH 240h (No condensation)
4	High temperature operation test	Ta = 60°C 240h (The panel temp. must be less than 50°C)
5	Low temperature operation test	Ta = -0°C 240h
6	Vibration test (non- operating)	Frequency range: 10 to 55Hz Stroke: 1.5mm Sweep time: 1minutes Test period: 2 hours for each direction of X,Y,Z
7	Shock test	Direction: ±X, ±Y, ±Z, Time: Third for each direction. Impact value: 980m/s², Action time 6ms
8	Thermal shock test	Ta=-10°C to 70°C /10 cycles (30 min) (30min)
9	Electro static discharge test	±200V· 200pF(0Ω) to Terminals(Contact) (1 time for each terminals) ±4kV・150pF(330Ω) to Housing bezel(Contact) ±8kV・150pF(330Ω) to Housing bezel(in Air)

【Note】Ta = Ambient temperature, Tp = Panel temperature

【Check items】

(a)Test No.1 to No.8

In the standard condition, there shall be no practical problems that may affect the display function.

12. Display Grade

The standard regarding the grade of color LCD displaying modules should be based on the delivery inspection standard.

13. Delivery Form

13-1. Carton storage conditions

1) Carton piling-up: Max 8 rows

2) Environments

Temperature: 0～40°C

Humidity: 65% RH or less (at 40°C)

There should be no dew condensation even at a low temperature and high humidity.

3) Packing form: As shown in 15. LCD module packing carton

※Cartons are weak against damp, and they are apt to be smashed easily due to the compressive pressure applied when piled up. The above environmental conditions of temperature and humidity are set in consideration of reasonable pile-up for storage.

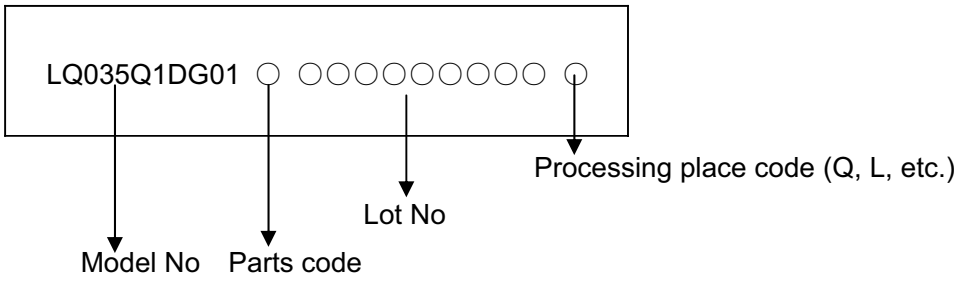
13-2. Packing composition

Name	quantity	Note
Carton size	1	575×360×225 (mm)
Tray	12	Material: Electrification prevention polypropylene
(The number of Module)	120	12 unit/tray: 120 unit/carton
Electrification prevention bag	2	Material: Electrification prevention polyethylene 680mm(length)×500mm(depth)×50μm(thin)

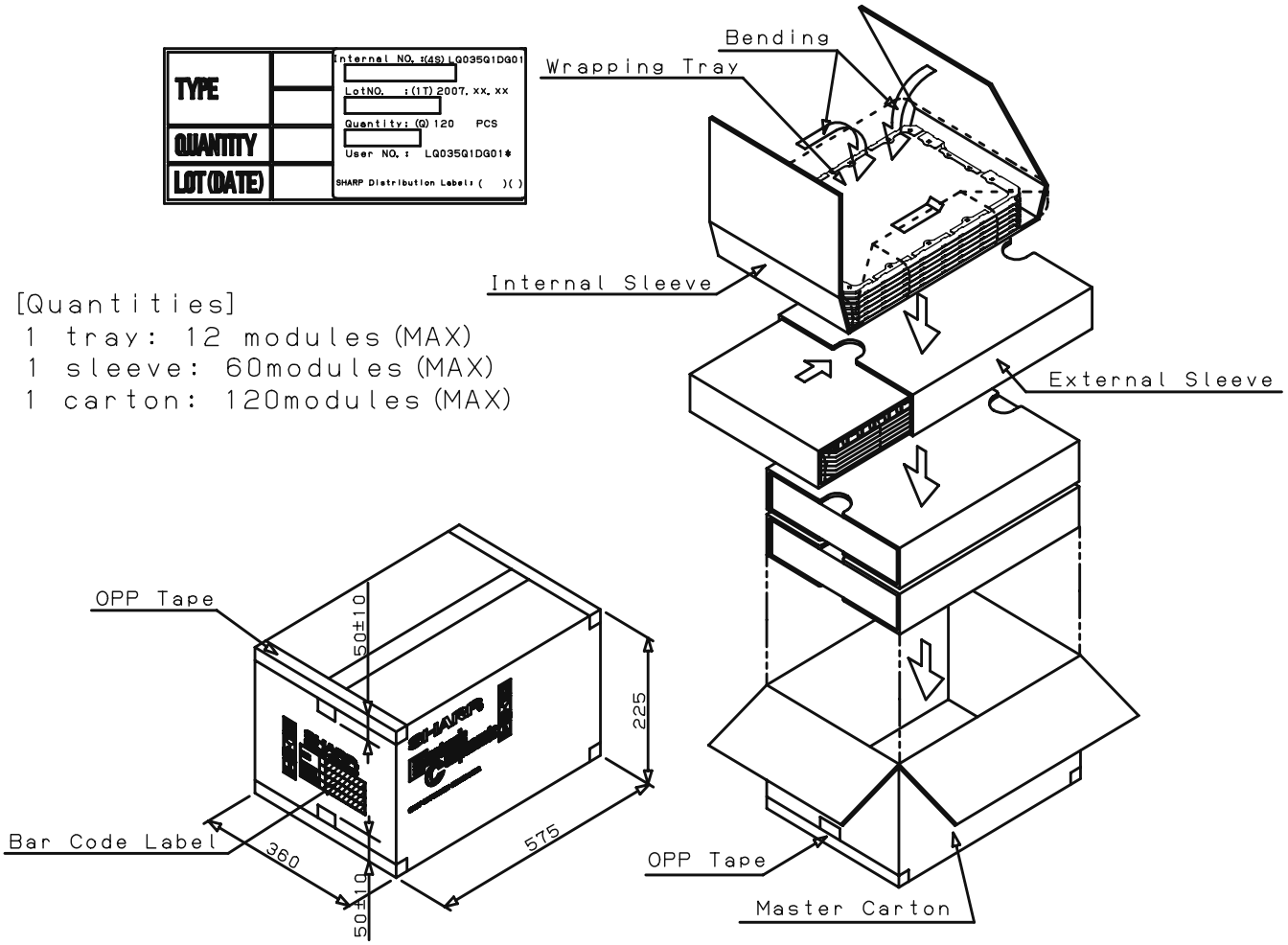
Carton weight (120 modules): Approx. 9.8kg

14. Lot No. marking

The lot No. will be printed on every module by ink-jet. The indication style is shown as below drawing.



15. LCD module packing carton



16. Others

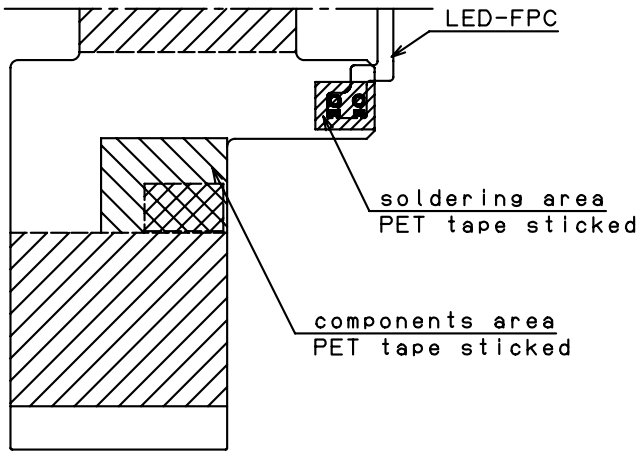
1 Disassembling the module can cause permanent damage and you should be strictly avoided.

2 Please be careful that you don't keep the screen displayed fixed pattern image for a long time, since retention may occur.

3 If you pressed down a liquid crystal display screen with your finger and so on, the alignment disorder of liquid crystal will occur. And then It will become display fault.
Therefore, be careful not to touch the screen directly, and to consider not stressing to it.

4 If any problem arises regarding the items mentioned in this specification sheet or otherwise, it should be discussed and settled mutually in a good faith for remedy and/or improvement.

17.Sticking position of insulated tape in soldering area and components area



Do not stick out of the eage of FPC

18. Outline Dimensions