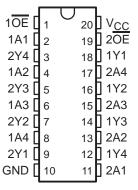
SCAS414L - NOVEMBER 1992 - REVISED APRIL 1999

- EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process
- Typical V_{OLP} (Output Ground Bounce)
 <0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot) >2 V at V_{CC} = 3.3 V, T_A = 25°C
- Power Off Disables Outputs, Permitting Live Insertion
- Supports Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltage With 3.3-V V_{CC})
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- Package Options Include Shrink Small-Outline (DB), Plastic Small-Outline (DW), and Thin Shrink Small-Outline (PW) Packages

DB, DW, OR PW PACKAGE (TOP VIEW)



description

This octal buffer/line driver is operational at 1.5-V to 3.6-V V_{CC} , but designed specifically for 1.65-V to 3.6-V V_{CC} operation.

The SN74LVC244A is organized as two 4-bit line drivers with separate output-enable (\overline{OE}) inputs. When \overline{OE} is low, the device passes data from the A inputs to the Y outputs. When \overline{OE} is high, the outputs are in the high-impedance state.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74LVC244A is characterized for operation from -40°C to 85°C.

FUNCTION TABLE (each buffer)

INPU	JTS	OUTPUT
OE	Α	Y
L	Н	Н
L	L	L
Н	Χ	Z

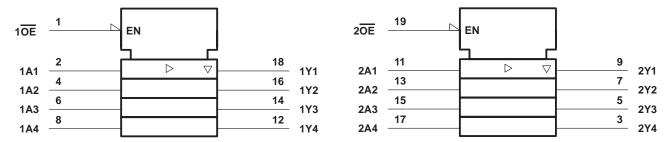


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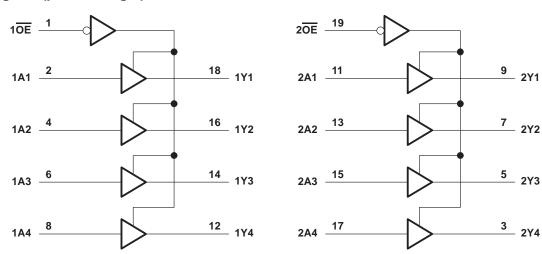


logic symbol[†]



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V _{CC}	–0.5 V to 6.5 V
Input voltage range, V _I (see Note 1)	–0.5 V to 6.5 V
Voltage range applied to any output in the high-impedance or power-off state, VO	
(see Note 1)	–0.5 V to 6.5 V
Voltage range applied to any output in the high or low state, VO	
(see Notes 1 and 2)	–0.5 V to V_{CC} + 0.5 V
Input clamp current, I _{IK} (V _I < 0)	–50 mA
Output clamp current, I _{OK} (V _O < 0)	–50 mA
Continuous output current, I _O	±50 mA
Continuous current through V _{CC} or GND	±100 mA
Package thermal impedance, θ _{JA} (see Note 3): DB package	115°C/W
DW package	97°C/W
PW package	128°C/W
Storage temperature range, T _{Stq}	–65°C to 150°C

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
 - 2. The value of V_{CC} is provided in the recommended operating conditions table.
 - 3. The package thermal impedance is calculated in accordance with JESD 51.



recommended operating conditions (see Note 4)

			MIN	MAX	UNIT	
V/00	Supply voltage	Operating	1.65	3.6	V	
Vcc	Supply voltage	Data retention only	1.5		V	
		V _{CC} = 1.65 V to 1.95 V	0.65 × V _{CC}			
VIН	High-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7		V	
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2			
		V _{CC} = 1.65 V to 1.95 V		0.35 × V _{CC}		
VIL	Low-level input voltage	V _{CC} = 2.3 V to 2.7 V		0.7	V	
		V _{CC} = 2.7 V to 3.6 V		0.8		
٧ _I	Input voltage	-	0	5.5	V	
\/ -	Output voltage	High or low state	0	Vcc	V	
VO		3 state	0	5.5	V	
		V _{CC} = 1.65 V		-4		
1	High-level output current	V _{CC} = 2.3 V		-8		
ЮН		V _{CC} = 2.7 V		-12	mA	
		V _{CC} = 3 V		-24		
I _{OL} Low-leve		V _{CC} = 1.65 V		4		
	Low-level output current	V _{CC} = 2.3 V		8	1	
		V _{CC} = 2.7 V		12	mA	
		V _{CC} = 3 V		24		
T _A	Operating free-air temperature	-	-40	85	°C	

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CO	Vcc	MIN	TYP [†]	MAX	UNIT	
	I _{OH} = -100 μA	1.65 V to 3.6 V	V _{CC} -0.	2			
	$I_{OH} = -4 \text{ mA}$	1.65 V	1.2				
\/a	I _{OH} = -8 mA		2.3 V	1.7			V
VOH	10 m A		2.7 V	2.2			·
	$I_{OH} = -12 \text{ mA}$		3 V	2.4			
	I _{OH} = -24 mA	I _{OH} = -24 mA					
	I _{OL} = 100 μA		1.65 V to 3.6 V			0.2	
	I _{OL} = 4 mA	1.65 V			0.45	V	
VoL	I _{OL} = 8 mA	2.3 V			0.7		
	I _{OL} = 12 mA	2.7 V			0.4		
	I _{OL} = 24 mA		3 V			0.55	
lį	V _I = 0 to 5.5 V		3.6 V			±5	μΑ
l _{off}	V_I or $V_O = 5.5 V$		0			±10	μΑ
loz	$V_{O} = 0 \text{ to } 5.5 \text{ V}$		3.6 V			±10	μΑ
	$V_I = V_{CC}$ or GND			10		μΑ	
lcc	$3.6 \text{ V} \le \text{V}_{\text{I}} \le 5.5 \text{ V}^{\ddagger}$	IO = 0	3.6 V				
ΔlCC	One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND		2.7 V to 3.6 V			500	μΑ
Ci	V _I = V _{CC} or GND	3.3 V		4		pF	
Co	$V_O = V_{CC}$ or GND	3.3 V		5.5		pF	

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C. ‡ This applies in the disabled state only.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 1.5 V	V _{CC} = 1.8 V	V _{CC} =		V _{CC} =	2.7 V	V _{CC} =	3.3 V 3 V	UNIT
	(INFOT)	(001701)	TYP	TYP	MIN	MAX	MIN	MAX	MIN	MAX	
^t pd	А	Υ	5.75	12	1	7.9		6.9	1.5	5.9	ns
t _{en}	ŌĒ	Υ	6.59	13.1	1	9.6		8.6	1.5	7.6	ns
t _{dis}	ŌĒ	Υ	5.7	14.6	1	7.8		6.8	1.5	6.5	ns

operating characteristics, T_A = 25°C

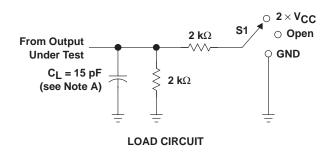
PARAMETER		TEST CONDITIONS	V _{CC} = 1.8 V TYP	V _{CC} = 2.5 V TYP	V _{CC} = 3.3 V	UNIT	
Cont	Power dissipation capacitance	Outputs enabled	f = 10 MHz	43	43	44	pF
C _{pd}	per buffer/driver	Outputs disabled	1 = 10 WHZ	1	1	2	þг



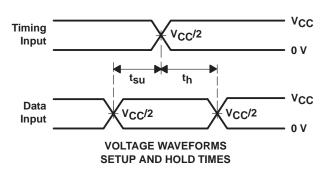
VCC

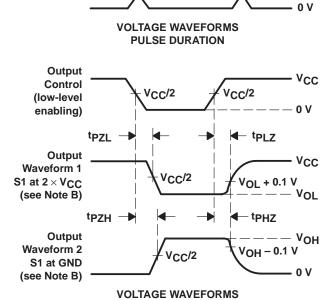
V_{CC}/2

PARAMETER MEASUREMENT INFORMATION $V_{CC} = 1.5 \text{ V}$



TEST	S 1
t _{pd}	Open
tPLZ/tPZL	2×V _{CC}
tPHZ/tPZH	GND

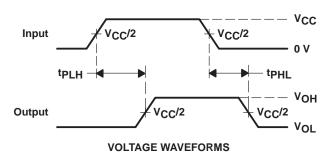




ENABLE AND DISABLE TIMES

V_{CC}/2

Input



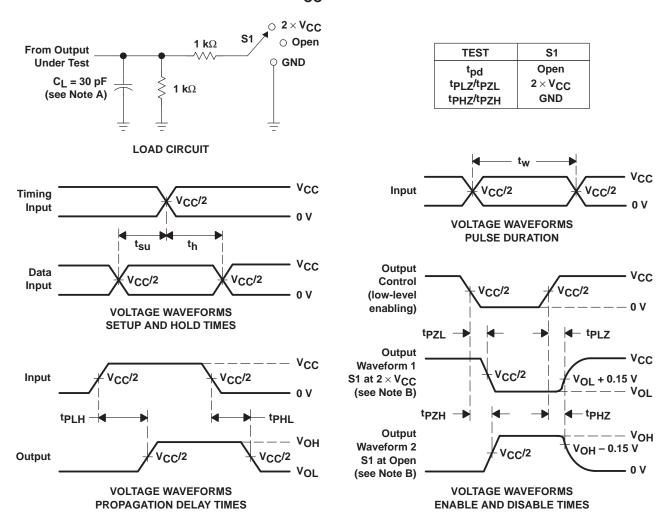
PROPAGATION DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_f \leq 2$ ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION V_{CC} = 1.8 V



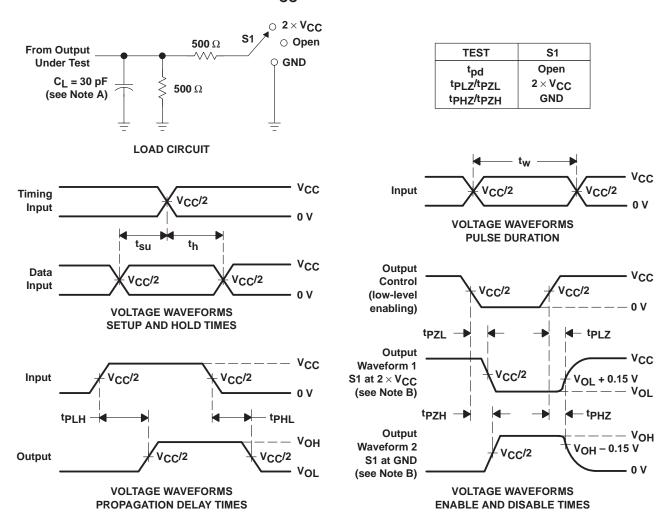
NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_Q = 50 \Omega$, $t_f \leq 2$ ns. $t_f \leq 2$ ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 2. Load Circuit and Voltage Waveforms



PARAMETER MEASUREMENT INFORMATION $V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$

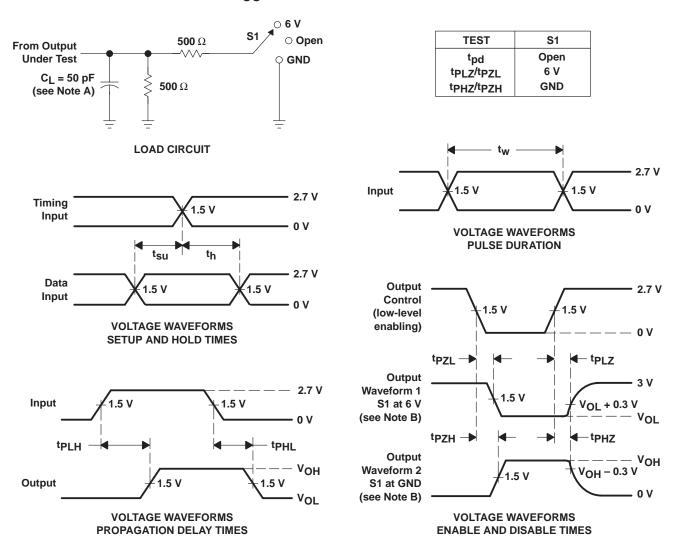


NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_f \leq 2$ ns. $t_f \leq 2$ ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 3. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION V_{CC} = 2.7 V AND 3.3 V \pm 0.3 V



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_{O} = 50 \Omega$, $t_{f} \leq$ 2.5 ns, $t_{f} \leq$ 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 4. Load Circuit and Voltage Waveforms



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