

64K x 16 HIGH-SPEED CMOS STATIC RAM WITH 3.3V SUPPLY

NOVEMBER 2005

FEATURES

- High-speed access time: 8, 10, 12 ns
- · CMOS low power operation
 - 61LV6416: 75 mW (typical) operating current 0.5 mW (typical) standby current
 - 61LV6416L: 65 mW (typical) operating current 50 μW (typical) standby current
- TTL compatible interface levels
- Single 3.3V power supply
- Fully static operation: no clock or refresh required
- Three state outputs
- Data control for upper and lower bytes
- Industrial temperature available
- Lead-free available

DESCRIPTION

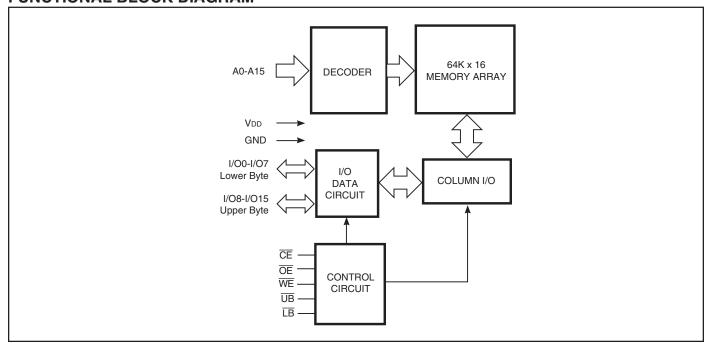
The ISSI IS61LV6416/IS61LV6416L is a high-speed, 1,048,576-bit static RAM organized as 65,536 words by 16 bits. It is fabricated using *ISSI*'s high-performance CMOS technology. This highly reliable process coupled with innovative circuit design techniques, yields access times as fast as 8 ns with low power consumption.

When \overline{CE} is HIGH (deselected), the device assumes a standby mode at which the power dissipation can be reduced down with CMOS input levels.

Easy memory expansion is provided by using Chip Enable and Output Enable inputs, \overline{CE} and \overline{OE} . The active LOW Write Enable (WE) controls both writing and reading of the memory. A data byte allows Upper Byte (UB) and Lower Byte (LB) access.

The IS61LV6416/IS61LV6416L is packaged in the JEDEC standard 44-pin 400-mil SOJ, 44-pin TSOP-II, and 48-pin mini BGA (6mm x 8mm).

FUNCTIONAL BLOCK DIAGRAM

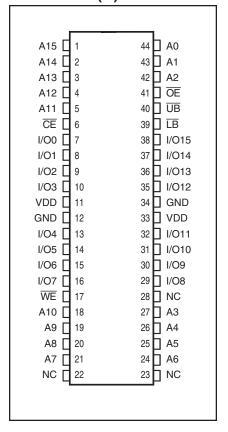


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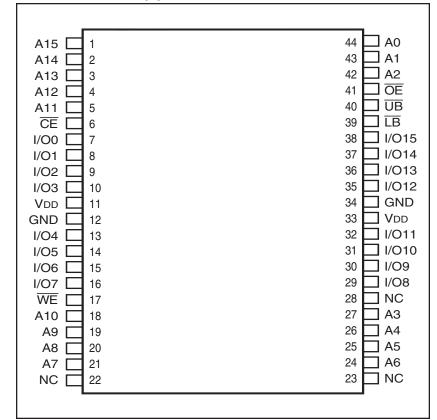


PIN CONFIGURATIONS

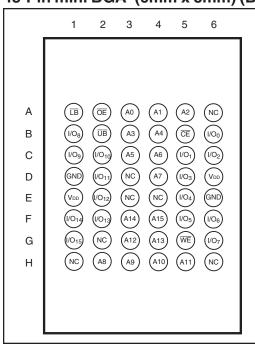
44-Pin SOJ (K)



44-Pin TSOP-II (T)



48-Pin mini BGA (6mm x 8mm) (B)



PIN DESCRIPTIONS

A0-A15	Address Inputs
I/O0-I/O15	Data Inputs/Outputs
CE	Chip Enable Input
ŌĒ	Output Enable Input
WE	Write Enable Input
LB	Lower-byte Control (I/O0-I/O7)
UB	Upper-byte Control (I/O8-I/O15)
NC	No Connection
V _{DD}	Power
GND	Ground



TRUTH TABLE

					I/O PIN						
Mode	WE	CE	ŌĒ	LB	UB	1/00-1/07	I/O8-I/O15	V _{DD} Current			
Not Selected	Х	Н	Х	Х	Х	High-Z	High-Z	ISB1, ISB2			
Output Disabled	Н	L	Н	Х	Χ	High-Z	High-Z	lcc			
	Χ	L	Χ	Н	Н	High-Z	High-Z				
Read	Н	L	L	L	Н	D ouт	High-Z	Icc			
	Н	L	L	Н	L	High-Z	Dout				
	Н	L	L	L	L	Dout	Dout				
Write	L	L	Х	L	Н	DIN	High-Z	lcc			
	L	L	Χ	Н	L	High-Z	DIN				
	L	L	Χ	L	L	DIN	DIN				

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Parameter	Value	Unit
VTERM	Terminal Voltage with Respect to GND	-0.5 to $V_{DD}+0.5$	V
Tstg	Storage Temperature	-65 to +150	°C
Рт	Power Dissipation	1.5	W
lout	DC Output Current (LOW)	20	mA

Note:

OPERATING RANGE

Range	Ambient Temperature	VDD (8,10 ns)	VDD (12 ns)
Commercial	0°C to +70°C	3.3V+10%,-5%	3.3V ± 10%
Industrial	–40°C to +85°C	3.3V+10%,-5%	3.3V ± 10%

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
Vон	Output HIGH Voltage	V _{DD} = Min., Iон = -4.0 mA	2.4	_	V
Vol	Output LOW Voltage	VDD = Min., IOL = 8.0 mA	_	0.4	V
VIH	Input HIGH Voltage		2	V _{DD} + 0.3	V
VIL	Input LOW Voltage(1)		-0.3	0.8	V
ILI	Input Leakage	GND ≤ VIN ≤ VDD	-2	2	μA
ILO	Output Leakage	GND ≤ Vo∪т ≤ VDD, Outputs Disabled	-2	2	μA

Notes:

Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

^{1.} V_{IL} (min.) = -2.0V for pulse width less than 10 ns.



IS61LV6416 POWER SUPPLY CHARACTERISTICS⁽¹⁾ (Over Operating Range)

				-8	ns	-10	ns	-12	ns	
Symbol	Parameter	Test Conditions		Min.	Max.	Min.	Max.	Min.	Max.	Unit
Icc	V _{DD} Dynamic Operating	V _{DD} = Max.,	Com.	_	140	_	120	_	100	mA
	Supply Current	IOUT = 0 mA, f = fMAX	Ind.	_	150	_	130	_	110	
			typ.(2)	_	105	_	95	_	75	
Isb1	TTL Standby Current	VDD = Max.,	Com.	_	15	_	15	_	15	mA
	(TTL Inputs)	$\frac{V_{IN} = V_{IH} \text{ or } V_{IL}}{\overline{CE}} \geq V_{IH} \; , \; \; f = 0$	Ind.	_	20	_	20	_	20	
IsB2	CMOS Standby	V _{DD} = Max.,	Com.	_	5	_	5	_	5	mA
	Current (CMOS Inputs)	$\overline{CE} \ge V_{DD} - 0.2V$,	Ind.	_	10	_	10	_	10	
	, ,	$\begin{aligned} &V_{\text{IN}} \geq V_{\text{DD}} - 0.2V, \text{ or} \\ &V_{\text{IN}} \leq 0.2V, f = 0 \end{aligned}$	typ. ⁽²⁾	_	0.5	_	0.5	_	0.5	

Note:

IS61LV6416L POWER SUPPLY CHARACTERISTICS⁽¹⁾ (Over Operating Range)

Symbol	Parameter	Test Conditions		-8 Min.	ns Max.	-10 Min.	ns Max.	Unit
lcc	VDD Dynamic Operating Supply Current	$V_{DD} = Max.$, $I_{OUT} = 0 \text{ mA}$, $f = f_{MAX}$	Com. Ind. typ. ⁽²⁾	_ _ _	100 110 75	_ _ _	95 105 70	mA
ISB1	TTL Standby Current (TTL Inputs)	$V_{DD} = Max.,$ $V_{IN} = V_{IH} \text{ or } V_{IL}$ $\overline{CE} \ge V_{IH}, f = 0$	Com. Ind.	_	15 20	_	15 20	mA
ISB2	CMOS Standby Current (CMOS Inputs)	$\begin{split} & \frac{V_{DD} = Max.,}{\overline{CE}} \geq V_{DD} - 0.2V,\\ & V_{IN} \geq V_{DD} - 0.2V, \text{ or }\\ & V_{IN} \leq 0.2V, f = 0 \end{split}$	Com. Ind. typ. ⁽²⁾	_ _ _	1 1.5 0.05	_ _ _	1 1.5 0.05	mA

CAPACITANCE(1)

Symbol	Parameter	Conditions	Max.	Unit
Cin	Input Capacitance	VIN = 0V	6	pF
Соит	Input/Output Capacitance	Vout = 0V	8	pF

Note:

^{1.} At f = fMAX, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change. 2. Typical values are measured at VDD=3.3V, Ta=25°C. Not 100% Tested.

^{1.} At f = fmax, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.

^{2.} Typical values are measured at VDD=3.3V, TA=25°C. Not 100% Tested.

^{1.} Tested initially and after any design or process changes that may affect these parameters.



AC TEST CONDITIONS

Parameter	Unit
Input Pulse Level	0V to 3.0V
Input Rise and Fall Times	3 ns
Input and Output Timing and Reference Level	1.5V
Output Load	See Figures 1a and 1b

AC TEST LOADS

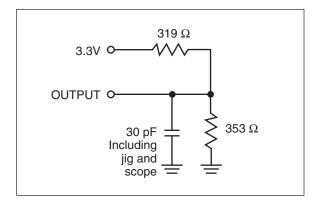


Figure 1a.

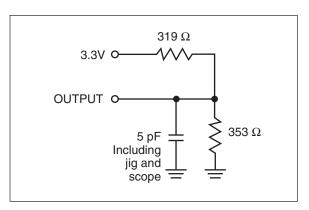


Figure 1b.

READ CYCLE SWITCHING CHARACTERISTICS⁽¹⁾ (Over Operating Range)

Symbol	Parameter	-8 : Min.	ns Max.	-10 Min.	ns Max.	-12 Min.	ns Max.	Unit
trc	Read Cycle Time	8	_	10	_	12	_	ns
taa	Address Access Time		8	_	10	_	12	ns
t oha	Output Hold Time	3	_	3	_	3	_	ns
tace	CE Access Time	_	8	_	10	_	12	ns
tDOE	OE Access Time	_	5	_	5	_	6	ns
thzoe(2)	OE to High-Z Output	_	5	_	5	_	6	ns
tlzoe(2)	OE to Low-Z Output	0	_	0	_	0	_	ns
thzce(2	CE to High-Z Output	0	4	0	5	0	6	ns
tLZCE ⁽²⁾	CE to Low-Z Output	3	_	3	_	3	_	ns
t BA	LB, UB Access Time	_	6	_	6	_	6	ns
t HZB	LB, UB to High-Z Output	0	4	0	5	0	6	ns
tlzb	LB, UB to Low-Z Output	0	_	0	_	0	_	ns

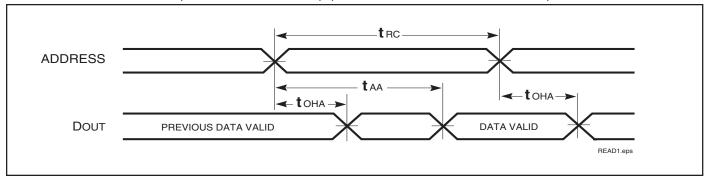
Notes:

- 1. Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading specified in Figure 1a.
- 2. Tested with the load in Figure 1b. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.
- 3. Not 100% tested.

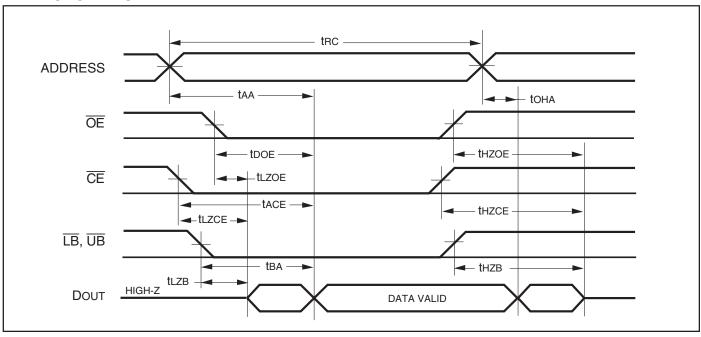


AC WAVEFORMS

READ CYCLE NO. $1^{(1,2)}$ (Address Controlled) ($\overline{CS} = \overline{OE} = V_{IL}$, \overline{UB} or $\overline{LB} = V_{IL}$)



READ CYCLE NO. 2^(1,3)



- Notes:
 1. WE is HIGH for a Read Cycle.
- 2. The device is continuously selected. \overline{OE} , \overline{CE} , \overline{UB} , or $\overline{LB} = V_{IL}$.
- 3. Address is valid prior to or coincident with $\overline{\textbf{CE}}$ LOW transition.



WRITE CYCLE SWITCHING CHARACTERISTICS(1,3) (Over Operating Range)

•			ns	-10		-12		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Unit
twc	Write Cycle Time	8	_	10	_	12	_	ns
tsce	CE to Write End	6	_	8	_	9	_	ns
taw	Address Setup Time to Write End	8	_	8	_	9	_	ns
tha	Address Hold from Write End	0	_	0	_	0	_	ns
t sa	Address Setup Time	0	_	0	_	0	_	ns
t PBW	LB, UB Valid to End of Write	7	_	8	_	9	_	ns
tpwe1/tpwe2	WE Pulse Width (OE = HIGH/LOW)	6	_	8	_	9	_	ns
tsp	Data Setup to Write End	6	_	6	_	6	_	ns
tho	Data Hold from Write End	0	_	0	_	0	_	ns
thzwe ⁽²⁾	WE LOW to High-Z Output	_	4	_	5	_	6	ns
tLzwe ⁽²⁾	WE HIGH to Low-Z Output	3	_	3	_	3	_	ns

Notes

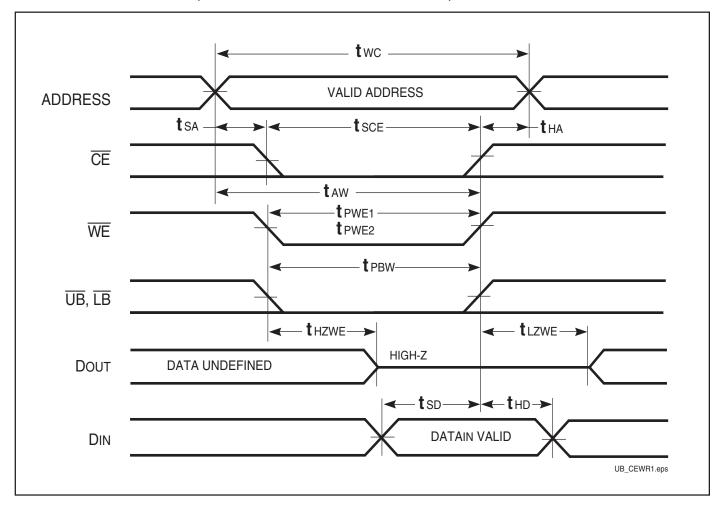
2. Tested with the load in Figure 1b. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.

^{1.} Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading specified in Figure 1a.

^{3.} The internal write time is defined by the overlap of $\overline{\textbf{CE}}$ LOW and $\overline{\textbf{UB}}$ or $\overline{\textbf{LB}}$, and $\overline{\textbf{WE}}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write.

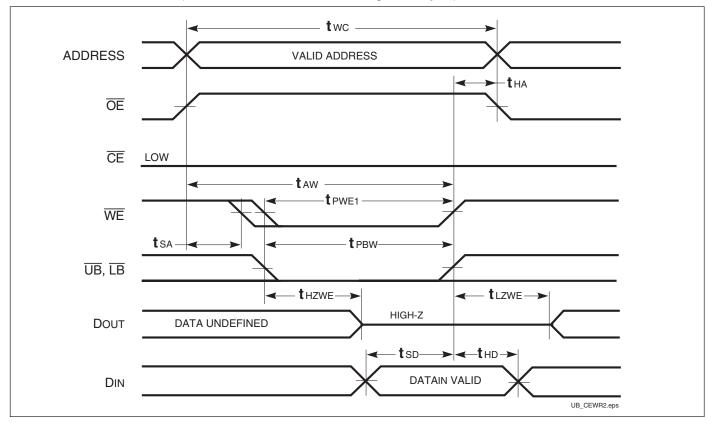


WRITE CYCLE NO. $1^{(1,2)}$ ($\overline{\text{CE}}$ Controlled, $\overline{\text{OE}}$ = HIGH or LOW)

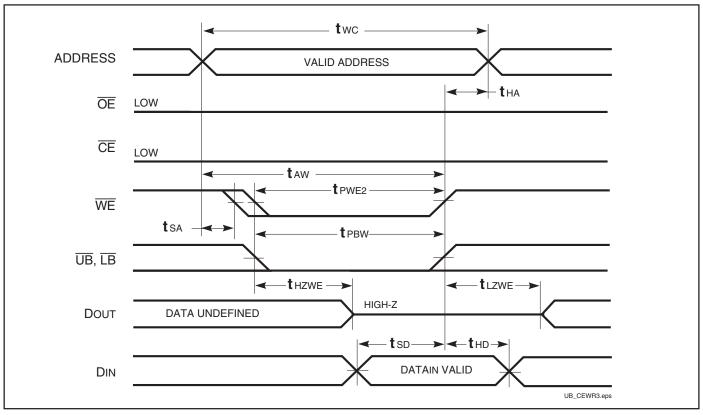




WRITE CYCLE NO. $2^{(1)}$ (WE Controlled, \overline{OE} = HIGH during Write Cycle)

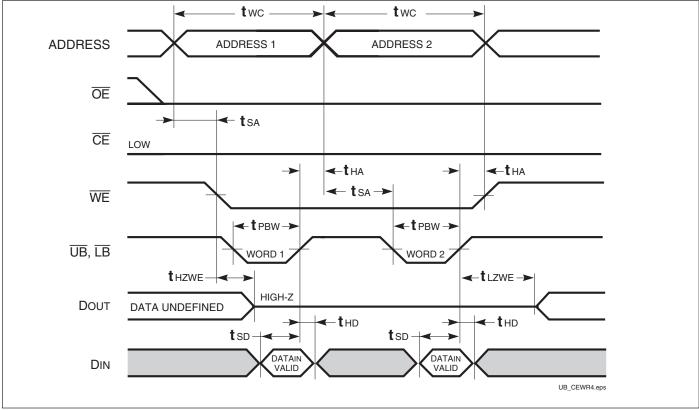


WRITE CYCLE NO. 3 (WE Controlled: OE is LOW During Write Cycle)





WRITE CYCLE NO. 4 (LB, UB Controlled, Back-to-Back Write)(1,3)



Notes:

- 1. The internal Write time is defined by the overlap of $\overline{CE} = LOW$, \overline{UB} and/or $\overline{LB} = LOW$, and $\overline{WE} = LOW$. All signals must be in valid states to initiate a Write, but any can be deasserted to terminate the Write. The tsa, tha, tsd, and the timing is referenced to the rising or falling edge of the signal that terminates the Write.
- Tested with OE HIGH for a minimum of 4 ns before WE = LOW to place the I/O in a HIGH-Z state.
 WE may be held LOW across many address cycles and the LB, UB pins can be used to control the Write function.

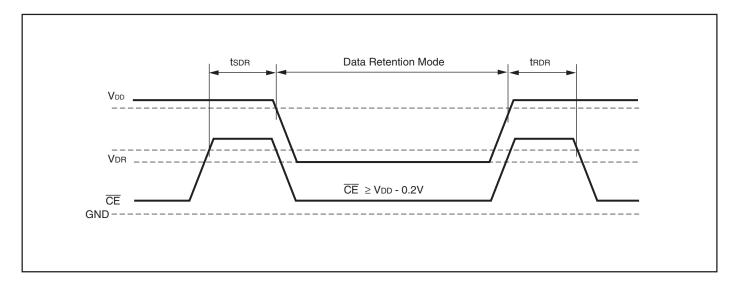


DATA RETENTION SWITCHING CHARACTERISTICS

Symbol	Parameter	Test Condition	Options	Min.	Typ. ⁽¹⁾	Max.	Unit
VDR	VDD for Data Retention	See Data Retention Waveform		2.0	_	3.6	V
IDR	Data Retention Current	$V_{DD} = 2.0V, \overline{CE} \ge V_{DD} - 0.2V$	IS61LV6416	_	0.5	10	mA
			IS61LV6416L	_	0.05	1.5	
tsdr	Data Retention Setup Time	See Data Retention Waveform		0	_	_	ns
trdr	Recovery Time	See Data Retention Waveform		t RC	_	_	ns

Note 1: Typical values are measured at VDD = 3.0V, TA = 25°C and not 100% tested.

DATA RETENTION WAVEFORM (CE Controlled)





IS61LV6416
ORDERING INFORMATION

Speed (ns)	Order Part No.	Package	Temperature Range
8	IS61LV6416-8T	Plastic TSOP	Commercial (0°C to +70°C)
8	IS61LV6416-8TL	Plastic TSOP	Commercial (0°C to +70°C), Lead-free
8	IS61LV6416-8BI	mini BGA (6mm x 8mm)	Industrial (-40°C to +85°C)
8	IS61LV6416-8TI	Plastic TSOP	Industrial (-40°C to +85°C)
8	IS61LV6416-8KL	400-mil Plastic SOJ	Commercial (0°C to +70°C), Lead-free
10	IS61LV6416-10T	Plastic TSOP	Commercial (0°C to +70°C)
10	IS61LV6416-10TL	Plastic TSOP	Commercial (0°C to +70°C), Lead-free
10	IS61LV6416-10K	400-mil Plastic SOJ	Commercial (0°C to +70°C)
10	IS61LV6416-10BI	mini BGA (6mm x 8mm)	Industrial (-40°C to +85°C)
10	IS61LV6416-10BLI	mini BGA (6mm x 8mm)	Industrial (-40°C to +85°C), Lead-free
10	IS61LV6416-10TI	Plastic TSOP	Industrial (-40°C to +85°C)
10	IS61LV6416-10TLI	Plastic TSOP	Industrial (-40°C to +85°C), Lead-free
10	IS61LV6416-10KI	400-mil Plastic SOJ	Industrial (-40°C to +85°C)
10	IS61LV6416-10KLI	400-mil Plastic SOJ	Industrial (-40°C to +85°C), Lead-free
12	IS61LV6416-12T	Plastic TSOP	Commercial (0°C to +70°C)
12	IS61LV6416-12K	400-mil Plastic SOJ	Commercial (0°C to +70°C)
12	IS61LV6416-12KL	400-mil Plastic SOJ	Commercial (0°C to +70°C), Lead-free
12	IS61LV6416-12BI	mini BGA (6mm x 8mm)	Industrial (-40°C to +85°C)

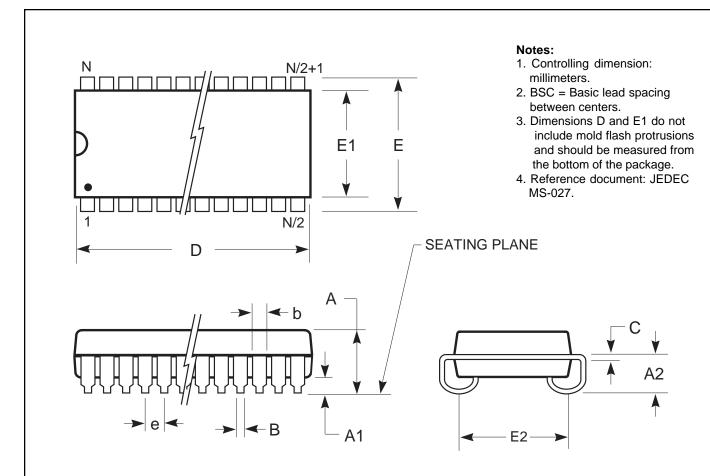
IS61LV6416L ORDERING INFORMATION

Speed (ns)	Order Part No.	Package	Temperature Range
8	IS61LV6416L-8T	Plastic TSOP	Commercial (0°C to +70°C)
8	IS61LV6416L-8BI	mini BGA (6mm x 8mm)	Industrial (-40°C to +85°C)
8	IS61LV6416L-8TI	Plastic TSOP	Industrial (-40°C to +85°C)
8	IS61LV6416L-8KI	400-mil Plastic SOJ	Industrial (-40 $^{\circ}$ C to +85 $^{\circ}$ C)
10	IS61LV6416L-10T	Plastic TSOP	Commercial (0°C to +70°C)
10	IS61LV6416L-10BI	mini BGA (6mm x 8mm)	Industrial (-40 $^{\circ}$ C to +85 $^{\circ}$ C)
10	IS61LV6416L-10TI	Plastic TSOP	Industrial (-40°C to +85°C)
10	IS61LV6416L-10KI	400-mil Plastic SOJ	Industrial (-40°C to +85°C)

PACKAGING INFORMATION



400-mil Plastic SOJ Package Code: K



	Millim	eters	Inche	es	Millim	eters	Inche	es	Millin	neters	Inch	es
Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
No. Leads	(N)	28				32	2				36	
Α	3.25	3.75	0.128	0.148	3.25	3.75	0.128	0.148	3.25	3.75	0.128	0.148
A1	0.64	_	0.025	_	0.64	_	0.025	_	0.64	_	0.025	_
A2	2.08	_	0.082	_	2.08	_	0.082	_	2.08	_	0.082	_
В	0.38	0.51	0.015	0.020	0.38	0.51	0.015	0.020	0.38	0.51	0.015	0.020
b	0.66	0.81	0.026	0.032	0.66	0.81	0.026	0.032	0.66	0.81	0.026	0.032
С	0.18	0.33	0.007	0.013	0.18	0.33	0.007	0.013	0.18	0.33	0.007	0.013
D	18.29	18.54	0.720	0.730	20.82	21.08	0.820	0.830	23.37	23.62	0.920	0.930
Е	11.05	11.30	0.435	0.445	11.05	11.30	0.435	0.445	11.05	11.30	0.435	0.445
E1	10.03	10.29	0.395	0.405	10.03	10.29	0.395	0.405	10.03	10.29	0.395	0.405
E2	9.40	BSC	0.370) BSC	9.40	BSC	0.370) BSC	9.40	BSC	0.370	BSC
е	1.27	BSC	0.05	0 BSC	1.27 E	3SC	0.050	BSC	1.27	BSC	0.050) BSC



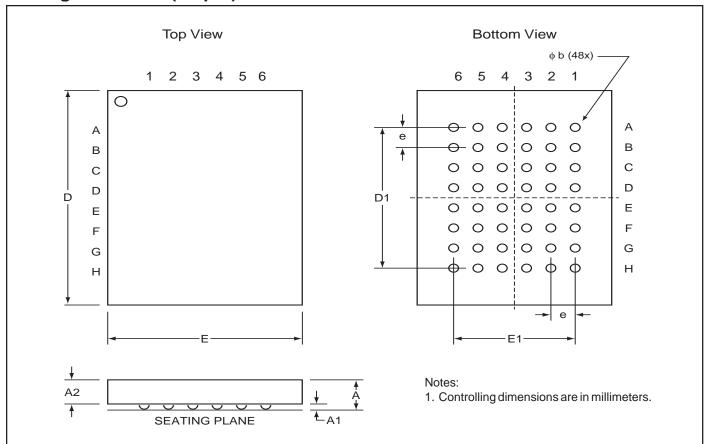
	Millimeters		Inches		Millim	Millimeters		Inches		Millimeters		Inches	
Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
No. Leads (N) 40							44						
A	3.25	3.75	0.128	0.148	3.25	3.75	0.128	0.148	3.25	3.75	0.128	0.148	
A1	0.64	_	0.025	_	0.64	_	0.025	_	0.64	_	0.025	_	
A2	2.08	_	0.082	_	2.08	_	0.082	_	2.08	_	0.082	_	
В	0.38	0.51	0.015	0.020	0.38	0.51	0.015	0.020	0.38	0.51	0.015	0.020	
b	0.66	0.81	0.026	0.032	0.66	0.81	0.026	0.032	0.66	0.81	0.026	0.032	
С	0.18	0.33	0.007	0.013	0.18	0.33	0.007	0.013	0.18	0.33	0.007	0.013	
D	25.91	26.16	1.020	1.030	27.18	27.43	1.070	1.080	28.45	28.70	1.120	1.130	
Е	11.05	11.30	0.435	0.445	11.05	11.30	0.435	0.445	11.05	11.30	0.435	0.445	
E1	10.03	10.29	0.395	0.405	10.03	10.29	0.395	0.405	10.03	10.29	0.395	0.405	
E2	9.40	BSC	0.370	BSC	9.40	BSC	0.370) BSC	9.40	BSC	0.370	BSC	
е	1.27	BSC	0.050	BSC	1.27 E	3SC	0.050	BSC	1.27	BSC	0.050) BSC	

PACKAGING INFORMATION



Mini Ball Grid Array

Package Code: B (48-pin)



mBGA - 6mm x 8mm

	MILL	IMET	ERS	INCHES					
Sym.	Min.	Тур.	Max.	Min.	Тур.	Max.			
N0. Leads		48							
A	_	_	1.20	_	_	0.047			
A1	0.24	_	0.30	0.009	_	0.012			
A2	0.60	_	_	0.024	_	_			
D	7.90	_	8.10	0.311	_	0.319			
D1	5	.25 BS	С	0.2	207 BS	SC .			
E	5.90	_	6.10	0.232	_	0.240			
E1	3	.75 BS	С	0.148 BSC					
е	0	.75 BS	С	0.030 BSC					
b	0.30	0.35	0.40	0.012	0.014	0.016			

mBGA - 8mm x 10mm

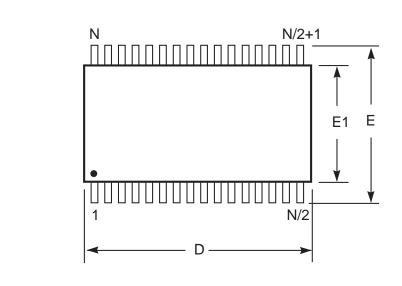
	MIL	LIME	ΓER	IN	3	
Sym.	Min.	Тур.	Max.	Min.	Тур.	Max.
N0. Leads		48				
A	_	_	1.20	_	_	0.047
A1	0.24	_	0.30	0.009		0.012
A2	0.60	_	_	0.024	_	_
D	9.90	_	10.10	0.390	_	0.398
D1	5	.25 BS	С	0.2	207 BS	SC
E	7.90	_	8.10	0.311	_	0.319
E1	3	.75 BS	С	0.1	SC SC	
е	0	.75 BS	С	0.0	SC	
b	0.30	0.35	0.40	0.012	0.014	1 0.016

PACKAGING INFORMATION



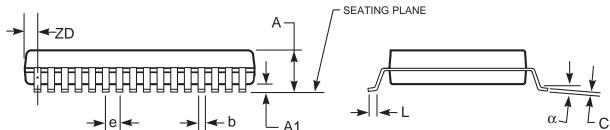
Plastic TSOP

Package Code: T (Type II)



Notes:

- Controlling dimension: millimieters, unless otherwise specified.
- 2. BSC = Basic lead spacing between centers.
- Dimensions D and E1 do not include mold flash protrusions and should be measured from the bottom of the package.
- 4. Formed leads shall be planar with respect to one another within 0.004 inches at the seating plane.



Plastic TSOP (T - Type II)													
	Millimeters		Inche	S	Millim	Millimeters		Inches		Millimeters		Inches	
Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Ref. Std.													
No. Leads (N) 32						44	1				50		
Α	_	1.20	_	0.047	_	1.20	_	0.047	_	1.20	_	0.047	
A1	0.05	0.15	0.002	0.006	0.05	0.15	0.002	0.006	0.05	0.15	0.002	0.006	
b	0.30	0.52	0.012	0.020	0.30	0.45	0.012	0.018	0.30	0.45	0.012	0.018	
С	0.12	0.21	0.005	0.008	0.12	0.21	0.005	0.008	0.12	0.21	0.005	0.008	
D	20.82	21.08	0.820	0.830	18.31	18.52	0.721	0.729	20.82	21.08	0.820	0.830	
E1	10.03	10.29	0.391	0.400	10.03	10.29	0.395	0.405	10.03	10.29	0.395	0.405	
Е	11.56	11.96	0.451	0.466	11.56	11.96	0.455	0.471	11.56	11.96	0.455	0.471	
е	1.27	BSC	0.050	BSC	0.80	BSC	0.032	BSC	0.80	BSC	0.031	BSC	
L	0.40	0.60	0.016	0.024	0.41	0.60	0.016	0.024	0.40	0.60	0.016	0.024	
ZD	0.95	REF	0.03	7 REF	0.81	REF	0.03	2 REF	0.88	REF	0.035	REF	
α	0°	5°	0°	5°	0°	5°	0°	5°	0°	5°	0°	5°	