

# **LQ065T5AR01**

## **Color TFT LCD Module**

(Model Number: LQ065T5AR01)

## **Specifications**

Spec No.: LCY-01096B

Dated: May 31. 2002

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|                        |   |  |
|------------------------|---|--|
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DEVICE SPECIFICATION FOR

**TFT – LCD    module**

**MODEL    No.    LQ065T5AR01**

CUSTOMER'S APPROVAL

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## RECORDS OF REVISION

MODEL No : LQ065T5AR01

[illegible]

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## (1) Introduction

The SHARP color TFT-LCD module is an active matrix LCD (Liquid Crystal Display) produced by making the most of Sharp's expertise in liquid-crystal and semiconductor technologies. The active device is amorphous silicon TFT (Thin Film Transistor). The module has a 16:9 aspect ratio and accepts full color video signal conforming to the NTSC and PAL systems. An outline of the module is shown in Table 1.

## (2) Features

- 16:9 aspect ratio suitable for the wide-screen systems.
- a variety of display modes can be selected without any loss of wide-screen characteristics
- The 6.5 screen produces a high resolution image that is composed of 93,600 pixel elements in a stripe arrangement.
- Wide viewing angle technology is adopted.  
(The direction which has earlier inversion of gray scale image : 6 o'clock direction.)
- External clock synchronization allows an extremely clear image to be displayed.
- TFT-active matrix-LCD drive system with high contrast
- Dual mode type [NTSC (M) and PAL(B · G) standards]
- MBK-PAL which enables the 234-scanning lines panel to display a picture with virtually 274-scanning lines.
- Reduced reflection as a result of low reflectance black matrix and an antiglare (AG) and anti-reflection (AR) polarizer being adopted.
- A thin, lightweight and compact  
①Effective area/Outline area= 82% ②Thickness= 16.0 mm③Mass= 240g(max)
- Through the use of TN-normally white mode, an image with highly natural color reproduction is realized.
- It is possible to reverse the display direction (right/left and up/down).
- Semi Self-heating Backlight that is excellent of brightness rising characteristics at low temperature in consideration of automotive application

## (3) Construction and Outline

Outline dimension of TFT-LCD module : Fig. 1

The module consists of the TFT-LCD panel, driver ICs, control PWB mounted with electronic circuits, semi self-heating backlight, frame, inverter, DC/DC for single supply voltage, front and rear shielding cases.:Fig.7

## (4) Module geometry(Mechanical specifications)

Table 1

| Parameter              | Specifications             | Units  | Remarks   |
|------------------------|----------------------------|--------|-----------|
| Display format         | 93,600                     | pixels |           |
|                        | 1200(W)×234(H)             | dots   |           |
| Active area            | 143.4 (W) ×79.326 (H)      | mm     |           |
| Screen size (Diagonal) | 16.5 [6.5" ]               | cm     |           |
| Dot pitch              | 0.1195 (W) ×0.339 (H)      | mm     |           |
| Pixel configuration    | R,G,B Stripe configuration |        |           |
| Outline dimension      | 155(W)×89.2(H)×16.0(D)     | mm     | 【Note4-1】 |
| Mass                   | 240                        | g      | Max       |

【Note4-1】 This measurement is typical,and see Fig .1 for the details.

## (5)Input/Output terminal and their descriptions

## 5-1)TFT-LCD panel driving section

Table 2

(Hi and Lo means digital input voltage)

| Pin No. | Symbol | i/o   | Description  | Remarks                    |
|---------|--------|-------|--|----------------------------|
| 1       | TEST   | i     |  |                            |
| 2       | CLKC   | i     | Selection for input/output direction of HSY, VSY, CLK+, CLK- | 【Note5-1】                  |
| 3       | HSY    | i / o | Input/Output horizontal sync. signal (low active)            | 【Note5-2】                  |
| 4       | VSY    | i / o | Input/Output vertical sync. signal (low active)              | 【Note5-3】                  |
| 5       | PWMS   | o     | Timing signal for PWM dimming of backlight                   | 【Note5-4】                  |
| 6       | NTP    | i     | Selection for NTSC or PAL                                    | 【Note5-5】                  |
| 7       | HRV    | i     | Selection for horizontal scanning direction                  | 【Note5-6】                  |
| 8       | VRV    | i     | Selection for vertical scanning direction                    | 【Note5-7】                  |
| 9       | MODS   | i     | Selection for display mode                                   | 【Note5-8】                  |
| 10      | MODW   | i     | Selection for display mode                                   | 【Note5-8】                  |
| 11      | MODN   | i     | Selection for display mode                                   | 【Note5-8】                  |
| 12      | VIN    | i     | Positive power supply voltage                                |                            |
| 13      | VBS    | i     | Composite sync.signal (low active)                           | 【Note5-9】                  |
| 14      | BRT    | i     | Brightness adjusting terminal                                | 【Note5-10】                 |
| 15      | VR1    | i     | Color video signal (Red) 1                                   | Positive (On when VSW=Hi.) |
| 16      | VG1    | i     | Color video signal (Green) 1                                 | Ditto                      |
| 17      | VB1    | i     | Color video signal (Blue) 1                                  | Ditto                      |
| 18      | GND1   | i     | Ground   |                            |
| 19      | VR2    | i     | Color video signal (Red) 2                                   | Positive (On when VSW=Lo.) |
| 20      | VG2    | i     | Color video signal (Green) 2                                 | Ditto                      |
| 21      | VB2    | i     | Color video signal (Blue) 2                                  | Ditto                      |
| 22      | GND1   | i     | Ground   |                            |
| 23      | CLK-   | i     | Clock signal (LVDS-)   | 【Note5-11】                 |
| 24      | CLK+   | i     | Clock signal (LVDS+)   | 【Note5-11】                 |
| 25      | VSW    | i     | Selection signal of two sets of video signals                | 【Note5-12】                 |
| 26      | PWMI   | i     | Input signal for backlight dimming                           | 【Note5-13】                 |
| 27      | VBL    | i     | Power supply for BackLight                                   |                            |
| 28      | VBL    | i     | Power supply for BackLight                                   |                            |
| 29      | GND2   | i     | Ground for BackLight   |                            |
| 30      | GND2   | i     | Ground for BackLight   |                            |

【Note5-1】 CLKC = "Hi": HSY and VSY terminals are the output mode.

CLKC = "Lo": CLK+, CLK-, HSY and VSY terminals are the input mode.

【Note5-2】 If CLKC="Hi", this terminal outputs horizontal sync. signal in phase with VBS.

If CLKC="Lo", this terminal will be external horizontal sync. input terminal.

【Note5-3】 If CLKC="Hi", this terminal outputs vertical sync. signal in phase with VBS.

If CLKC="Lo", this terminal will be external vertical sync. input terminal.

【Note5-4】 PWM signal is used for the PWM dimming frequency and it is possible to control the PWM signal dimming by combining both HSY and PWM signal. But, please use this PWM signal just in case of inputting standard NTSC or PAL signal.

【Note5-5】 NTP = "Hi": NTSC system

NTP = "Lo": PAL system

【Note5-6】 HRV = "Hi": Normal video

HRV = "Lo": Reversed video on horizontal direction

【Note5-7】 VRV = "Hi": Normal video

VRV = "Lo": Reversed video on vertical direction

【Note5-8】 Display mode settings are shown in Table 3.

【Note5-9】 The sync. Signal which will be input, is negative polarity, and is applicable to standard composite sync. signal, negative one, in the same pulse level.

- 【Note5-10】** Brightness is adjusted by the DC voltage supplied to this pin.  
They are adjusted to the optimum value on shipping, but, they can be re-adjusted by external circuit.
- 【Note5-11】** When CLKC="Lo", this terminal will be external clock input terminal.  
This signal should correspond to sampling timing of the horizontal direction image.  
NTP, MODS, MODW, and MODN should be "Hi" when CLKC="Lo".
- 【Note5-12】** When VSW="Hi", CH1 (VR1, VG1, VB1) is selected.  
When VSW="Low", CH2 (VR2, VG2, VB2) is selected.
- 【Note5-13】** The signal of PWMI is used for control of ON/OFF switch of backlight.  
When PWMI="Hi", the backlight is lighted. When PWMI="Low", the backlight puts the light out.  
And, PWMS signal is used for the PWMI dimming frequency and it is easy to get PWM signal dimming by combining both HSY and PWMS signal. But please use this PWMS signal just in case of inputting standard NTSC or PAL signal.



Table 3 Display Method and Characteristics

| MODS | MODW | MODN | Display mode | Characteristics  | Source                                  | example  |
|------|------|------|--------------|--|---|----------|
| H    | H    | H    | Full mode    | The picture is displayed with uniform enlargement in the horizontal direction, and the horizontal retrace line of the input signal cannot be seen. If the video sampling frequency of the image is fixed and a 4:3 video signal is displayed, the picture will be prominently oblong.  | 4:3 signal, Navigation signal           | Fig.3)-1 |
| H    | H    | L    | Wide 1 mode  | A 4:3 video signal is displayed with less feeling of incongruity than that in the full screen mode. Since the video horizontal sampling frequency is modulated in the horizontal direction, the degree of perfect roundness in the center of the screen is improved over that of the full screen mode.                                     | 4:3 signal                              | Fig.3)-2 |
| H    | L    | H    | Normal mode  | When displaying a 4:3 video signal, the displayed image is slightly less than perfectly round and the horizontal retrace line period is displayed at the two edges of the screen. With respect to the video horizontal sampling frequency, the center portion of the screen is slightly lower and the two edges become slightly higher.    | 4:3 signal                              | Fig.3)-3 |
| H    | L    | L    | Cinema mode  | A letter-box type image (16:9 signal) is displayed over the central width of the screen. In the horizontal direction, full screen display is utilized. Due to the display being extended in the vertical direction, a slightly less than perfectly round image is displayed.   | letter box type wide signal(16:9signal) | Fig.3)-4 |
| L    | H    | H    | Wide 2 mode  | In the horizontal direction, the Wide 1 display mode is employed. Due to the display being extended in the vertical direction, the portion of the picture in the center of the screen is slightly less than perfectly round. Also due to extending in the vertical direction, the upper and lower portions of the image are not displayed. | 4:3 signal                              | Fig.3)-5 |
| L    | H    | L    | test         | This mode is unusable as it is the test mode.  | —                                       | —        |
| L    | L    | H    | test         | This mode is unusable as it is the test mode.  | —                                       | —        |
| L    | L    | L    | test         | This mode is unusable as it is the test mode.  | —                                       | —        |

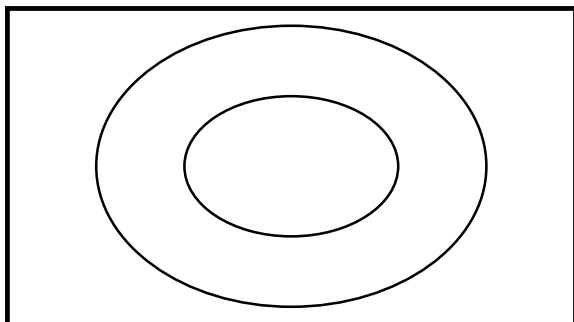


Fig.3)-1 Full mode

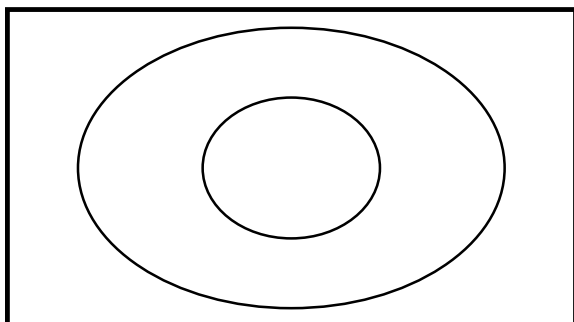


Fig.3)-2 Wide 1 mode

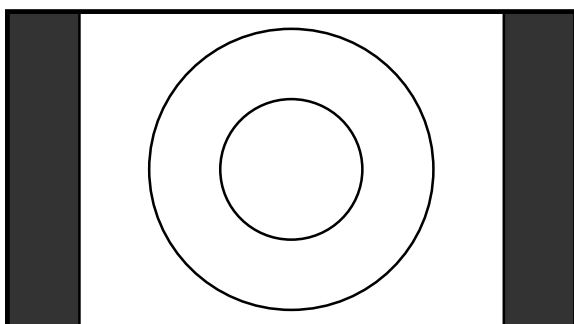


Fig.3)-3 Normal mode

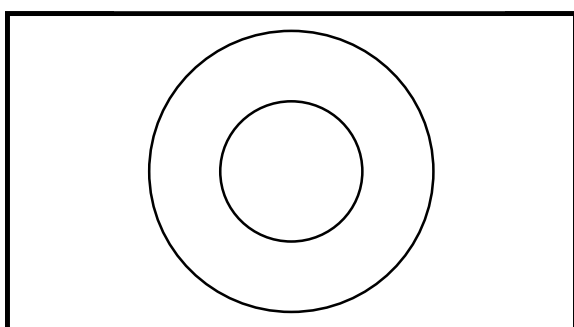


Fig.3)-4 Cinema mode

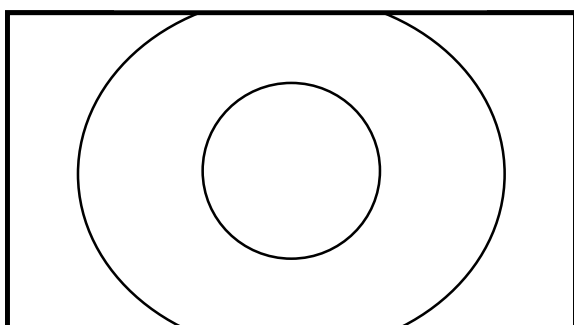


Fig.3)-5 Wide 2 mode

5-2) Functions, Modes and Terminals (Table 4)

| Mode terminals |           |                          |             |             | Sync,signal I/O terminals |                   |                         |                                  |  |
|----------------|-----------|--------------------------|-------------|-------------|---------------------------|-------------------|-------------------------|----------------------------------|--|
| CLKC           | NTP       | MODS                     | MODW        | MODN        | HSY                       | VS Y              | CLK－,<br>CLK＋           | VBS                              | Remarks                                |
| H              | H or<br>L | L<br>L<br>L              | H<br>L<br>L | L<br>H<br>L | H sync.<br>output         | V sync.<br>output | -                       | Composite<br>sync. input         | test mode                              |
| H              | H or<br>L | H                        | L           | H           | H sync.<br>output         | V sync.<br>output | -                       | Composite<br>sync. input         | NTSC or PAL mode<br>(Normal mode)      |
| H              | H or<br>L | other H or L<br>settings |             |             | H sync.<br>output         | V sync.<br>output | -                       | Composite<br>sync. input         | NTSC or PAL mode<br>(Full,Wide,Cinema) |
| L              | H         | H                        | H           | H           | H sync.<br>input          | V sync.<br>input  | Pixel<br>clock<br>input | input Hi or<br>Lo fixed<br>value | External clock<br>synchronous mode     |

(6) Absolute maximum ratings

Table 5

GND=0V、Ta=-30~+85℃

| Parameter                                      | Symbol | MIN  | MAX | Unit | Note           |
|--|--------|------|-----|------|----------------|
| Positive power supply voltage                  | VIN    | -0.3 | 9.0 | V    |                |
| Positive power supply voltage                  | VBL    | -0.3 | 9.0 | V    |                |
| Analog Input signals                           | VI A   | -    | 2.0 | Vp-p | [terminal 6-1] |
| Digital Input signals                          | VI D   | -0.3 | 5.3 | V    | [terminal 6-2] |
| Digital Output signals                         | VO D   | -0.3 | 5.3 | V    | [terminal 6-3] |
| LVDS Input signals                             | LIS    | -0.3 | 5.3 | V    | [terminal 6-4] |
| Brightness adjusting voltage                   | VBRT   | 0    | 5.0 | V    |                |
| Storage temperature                            | Tstg   | -40  | 85  | ℃    | 【Note 6-1,2】   |
| Operating temperature<br>(panel surface)       | Topr1  | -30  | 85  | ℃    | 【Note 6-2,3,4】 |
| Operating temperature<br>(Ambient temperature) | Topr2  | -30  | 65  | ℃    | 【Note 6-4,5】   |

[terminal 6-1] VBS, VR1, VG1, VB1, VR2, VG2, VB2 terminals(Video signal)

[terminal 6-2] HSY, NTP, VS Y, HRV, VRV, CLKC, VMSW, MODS, CLK, MODW, MODN, terminals

[terminal 6-3] HSY, VS Y, PWMS terminals

[terminal 6-4] CLK－,CLK+ terminals

【Note 6-1】 This rating is applied to all parts of the module and should not be exceeded.

【Note 6-2】 Maximum wet-bulb temperature is less than 58℃. Condensation of dew must be avoided as electrical current leaks will occur, causing a degradation of performance specifications.

【Note 6-3】 Please measure in the effective display area only.

【Note 6-4】 The operating temperature only guarantees operation of the circuit. For contrast, speed response, and other factors related to display quality, determine operating temperature using the formula Ta=+25℃

【Note 6-5】 Ambient temperature when the backlight is lit (reference value).

## (7) Electrical characteristics

## 7-1) Recommended operating conditions

## A) TFT-LCD panel driving section

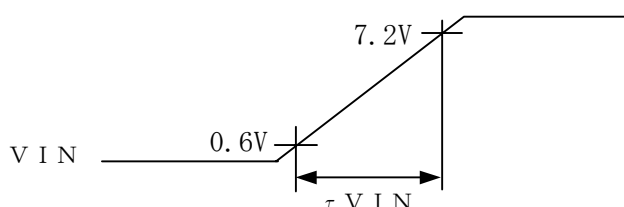
Table 6

GND = 0 V,  $T_{opr1} = -30 \sim 85^{\circ}\text{C}$ 

| Parameter                        |                                   | Symbol              | MIN      | TYP      | MAX      | Unit          | Remarks                  |
|----------------------------------|-----------------------------------|---------------------|----------|----------|----------|---------------|--------------------------|
| Power supply voltage             |                                   | VBL                 | +7.2     | +8.0     | +8.5     | V             |                          |
| Power supply voltage             |                                   | VIN                 | +7.2     | +8.0     | +8.8     | V             |                          |
| Power supply voltage rising time |                                   | $\tau_{VIN}$        |          |          | 60       | ms            | 【Note 7-1】               |
| Analog Input voltage             | Amplitude                         | VBS                 | 0.7      | 1.0      | 2.0      | Vp-p          |                          |
|                                  |                                   | VI                  | -        | 0.7      | -        | Vp-p          | 【Note 7-2】               |
|                                  | D C component                     | VIDC                | -1.0     | 0        | +1.0     | V             | 【Note 7-3】               |
| Digital Input voltage            | Hi                                | VIH                 | +3.5     | -        | +5.0     | V             | 【Note 7-4】               |
|                                  | Lo                                | VIL                 | 0        | -        | +0.5     | V             |                          |
|                                  | Histeresis                        | VH                  | +0.2     | -        | -        | V             |                          |
| Digital output voltage           | Hi                                | VOH                 | +4.0     | -        | +5.0     | V             | 【Note 7-5】               |
|                                  | Lo                                | VOL                 | 0        | -        | +1.0     | V             |                          |
| LVDS Input signal                | Differential Input High Threshold | VTH                 |          |          | +100     | mV            | CLKC="Lo"<br>【Note 7-6】  |
|                                  | Differential Input Low Threshold  | VTL                 | -100     |          |          | mV            |                          |
|                                  | frequency                         | fCLI                | 7.2      | 8.0      | 8.8      | MHz           |                          |
| Input horizontal sync. signal    | frequency                         | NTSC fH(N)          | 15.13    | 15.73    | 16.33    | kHz           | CLKC='Hi'<br>【Note 7-7】  |
|                                  |                                   | PAL fH(P)           | 15.03    | 15.63    | 16.23    | kHz           |                          |
|                                  | pulse width                       | NTSC $\tau_{HI(N)}$ | 4.2      | 4.7      | 5.2      | $\mu\text{s}$ |                          |
|                                  |                                   | PAL $\tau_{HI(P)}$  | 4.2      | 4.7      | 5.2      | $\mu\text{s}$ |                          |
|                                  | rising time                       | $\tau_{rHI1}$       | -        | -        | 0.5      | $\mu\text{s}$ |                          |
|                                  | falling time                      | $\tau_{fHI1}$       | -        | -        | 0.5      | $\mu\text{s}$ |                          |
| Input vertical sync. signal      | frequency                         | NTSC fV(N)          | fH/284   | fH/262.5 | fH/258   | Hz            | CLKC='Hi'<br>【Note 7-8】  |
|                                  |                                   | PAL fV(P)           | fH/344   | fH/312.5 | fH/304   | Hz            |                          |
|                                  | pulse width                       | NTSC $\tau_{VI(N)}$ | -        | 3H       | -        | $\mu\text{s}$ |                          |
|                                  |                                   | PAL $\tau_{VI(P)}$  | -        | 2.5H     | -        | $\mu\text{s}$ |                          |
|                                  | rising time                       | $\tau_{rVI}$        | -        | -        | 0.5      | $\mu\text{s}$ | CLKC='Hi' or 'Lo'        |
|                                  | falling time                      | $\tau_{fVI}$        | -        | -        | 0.5      | $\mu\text{s}$ |                          |
| Input horizontal sync. signal    | frequency                         | fHI                 | fCLI/550 | fCLI/508 | fCLI/490 | kHz           | CLKC='Lo'<br>【Note 7-9】  |
|                                  | pulse width                       | $\tau_{HI}$         | 1        | 5        | 9        | $\mu\text{s}$ |                          |
|                                  | rising time                       | $\tau_{rHI2}$       | -        | -        | 0.05     | $\mu\text{s}$ |                          |
|                                  | falling time                      | $\tau_{fHI2}$       | -        | -        | 0.05     | $\mu\text{s}$ |                          |
| Input vertical sync. signal      | frequency                         | fVI                 | 50       | fHI/262  | fHI/258  | Hz            | CLKC='Lo'<br>【Note 7-10】 |
|                                  | pulse width                       | $\tau_{VI}$         | 1H       | 3H       | 5H       | $\mu\text{s}$ |                          |
| Data setup time                  |                                   | tSU1                | 24       | -        | -        | ns            | CLKC='Lo'                |
| Data hold time                   |                                   | tHO1                | 44       | -        | -        | ns            | 【Note 7-6,9,11】          |
| Data setup time                  |                                   | tSU2                | 1.0      | -        | -        | $\mu\text{s}$ | CLKC='Lo'                |
| Data hold time                   |                                   | tHO2                | 1.0      | -        | -        | $\mu\text{s}$ | 【Note 7-6,10,12】         |

Caution: Signals must input after power has been turned on.

【Note 7-1】



- 【Note 7-2】 VR 1, VG 1, VB 1, VR 2, VG 2, VB 2 terminals (Video signal)
- 【Note 7-3】 VBS, VR 1, VG 1, VB 1, VR 2, VG 2, VB 2 terminals
- 【Note 7-4】 HSY, NTP, VSY, HRV, VRV, CLKC, VSW, MODS, MODW, MODN, PWMI terminals
- 【Note 7-5】 HSY, VSY, PWMS terminals
- 【Note 7-6】 CLK-,CLK+ (DS90C402 : LVDS Receiver made by National Semiconductor)  
(Adaptation LVDS Transmitter : DS90C401)
- 【Note 7-7】 VBS(horizontal sync. component) terminal
- 【Note 7-8】 VBS(vertical sync. component) terminal
- 【Note 7-9】 HSY terminal
- 【Note 7-10】 VSY terminal
- 【Note 7-11】 During the clock input mode, CLK-,CLK+ and the HSY input signal are out of phase. In this mode, the HSY input signal is effected by the rise time of the CLK+ input signal.
- 【Note 7-12】 During the clock input mode, HSY and the VSY input signal are out of phase. In this mode, the VSY input signal is effected by the rise time of the HSY input signal.

## 7-2)Power consumption

Table 7

T a =-30~+85°C

| Parameter               | Symbol | Conditions | MIN | TYP  | MAX  | Unit | Remarks |
|-------------------------|--------|------------|-----|------|------|------|---------|
| Positive supply current | IIN    | VIN=8.0V   | -   | 160  | 210  | mA   |         |
| Positive supply current | IBL    | VBL=8.0V   | -   | 750  | 950  | mA   |         |
| Total                   |        |            | -   | 7.28 | 9.20 | W    |         |

## 7-3)Input/Output signal timing chart

Table 8

VIN=+8.0,GND=0V

CLKC=Hi

NTSC:fH=15.73kHz,fv=60Hz,  $\tau_{HI}=4.7\mu s$

PAL:fH=15.63kHz,fv=50Hz,  $\tau_{HI}=4.7\mu s$

| Parameter  |                         | Symbol       | MIN | TYP  | MAX | Unit    | Remarks     |
|--|-------------------------|--------------|-----|------|-----|---------|-------------|
| Horizontal sync. Output                            | frequency               | fHO          | -   | fH   | -   | kHz     |             |
|  | pulse width             | $\tau_{HO}$  | 2.0 | 4.6  | 8.0 | $\mu s$ | 【Note 7-13】 |
|  | rising time             | $\tau_{rHO}$ | -   | -    | 0.5 | $\mu s$ | CL=10pF     |
|  | falling time            | $\tau_{fHO}$ | -   | -    | 0.5 | $\mu s$ | CL=10pF     |
| Horizontal sync. phase difference                  | HSY falling time        | $\tau_{pd1}$ | 0.5 | 1.6  | 3.0 | $\mu s$ | 【Note 7-14】 |
|  | HSY rising time         | $\tau_{pd2}$ |     | 1.6  | 3.4 | $\mu s$ |             |
| Vertical sync. Output                              | frequency               | fVO          | -   | Fv   | -   | Hz      |             |
|  | pulse width             | $\tau_{VO}$  | -   | 4H   | -   | $\mu s$ | 1H=1/fH     |
|  | sync. output difference | $\tau_{VHO}$ | -   | 11   | 29  | $\mu s$ |             |
|  | rising time             | $\tau_{rVO}$ | -   | -    | 2.0 | $\mu s$ | CL=10pF     |
|  | falling time            | $\tau_{fVO}$ | -   | -    | 2.0 | $\mu s$ | CL=10pF     |
| Vertical sync. Phase Difference                    | odd field               | $\tau_{DV1}$ | -   | 1H   | -   | $\mu s$ |             |
|  | even field              | $\tau_{DV2}$ | -   | 0.5H | -   |         |             |
| Clock and Video signal timing<br>【Reference value】 |                         | td           | 40  | 65   | 90  | ns      | 【Note7-15】  |

【Note7-13】 This is changed by the value of  $\tau_{pd1}$

【Note7-14】 Center position :  $\tau_{pd1}=1.6\pm0.4\mu s$  (NTSC mode)

【Note7-15】 Clock and Video signal timing : Fig.6

## 7-4) Display time range

## (1) NTSC(M) mode (NTP='Hi',CLKC='Hi')

- (a1) Horizontal Direction (full,wide1,2,cinema)  
13.1 ~ 63.2  $\mu$ s from the falling edge of HSY.
- (a2) Horizontal Direction (normal)  
8.0 ~ 68.3  $\mu$ s from the falling edge of HSY
- (b1) Vertical Direction (full,wide1,normal)  
20 ~ 253 H from the falling edge of VSY
- (b2) Vertical Direction (Cinema)  
49 ~ 224 H from the falling edge of VSY
- (b3) Vertical Direction (Wide2)  
42 ~ 228 H from the falling edge of VSY

## (2) PAL(B·G) mode (NTP='Lo',CLKC='Hi')

- (a1) Horizontal Direction (full,wide1,2,cinema)  
13.3 ~ 63.2  $\mu$ s from the falling edge of HSY
- (a2) Horizontal Direction (normal)  
8.1 ~ 68.4  $\mu$ s from the falling edge of HSY. (Normal)
- (b1) Vertical Direction (full,wide1,normal)  
26 ~ 298 H from the falling edge of VSY  
However, the video signals of (14n+12)H,(14n+20)H/Even field.  
(14n+17)H,(14n+23)H/Odd field (n=1,2···, 20)  
are not displayed on the module.
- (b2) Vertical Direction (cinema)  
49 ~ 282 H from the falling edge of VSY
- (b3) Vertical Direction (wide2)  
35 ~ 291 H from the falling edge of VSY  
However, the video signals of (22n+14)H,(22n+21)H/Even field.  
(22n+25)H,(22n+32)H/Odd field (n=1,2···, 12)  
are not displayed on the module.

## (3) External clock mode (NTP='Hi',CLKC='Lo')

Displaying the following range within video signals.

- (a) Horizontal Direction : 86 ~ 485 clk from the falling edge of HSY.  
(clk means input external clock.)
- (b) Vertical Direction : 20 ~ 253H from the falling edge of VSY.

## 7-5) Backlight driving section

Usable area for Backlight lighting

PWM Dimming Duty=100%~5%

(Please use this PWMS signal just in case of inputting standard NTSC or PAL signal)

DC/AC inverter driving frequency = 65kHz (reference value)

## (8)Optical characteristics

Table 9

VIN=+8.0V, VBL=+8.0V Ta=25℃

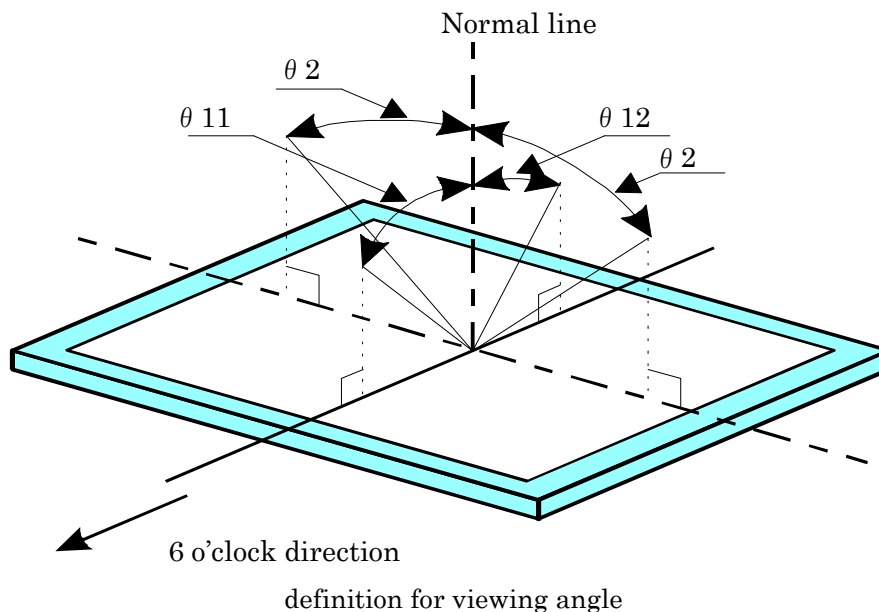
| Parameter           |      | Symbol             | Condition             | Min    | Typ   | Max   | Unit              | Remarks       |
|---------------------|------|--------------------|-----------------------|--------|-------|-------|-------------------|---------------|
| Viewing angle range |      | $\Delta \theta 11$ | $CR \geq 5$           | 60     | 65    | -     | ° (degree)        | 【Note8-1,2,3】 |
|                     |      | $\Delta \theta 12$ |                       | 35     | 40    | -     | ° (degree)        |               |
|                     |      | $\Delta \theta 2$  |                       | 60     | 65    | -     | ° (degree)        |               |
| Contrast ratio      |      | CRmax              | Optimal viewing angle | 60     | -     | -     |                   | 【Note8-1,3】   |
| Response time       | Rise | $\tau r$           | $\theta = 0^\circ$    | -      | 30    | 60    | ms                | 【Note8-1,4】   |
|                     | Fall | $\tau d$           |                       | -      | 50    | 100   | ms                |               |
| Luminance           |      | Y                  | $\theta = 0^\circ$    | 315    | 420   | -     | cd/m <sup>2</sup> | 【Note8-1,5】   |
| White chromaticity  |      | x                  | $\theta = 0^\circ$    | 0.263  | 0.313 | 0.363 |                   | 【Note8-1,5】   |
|                     |      | y                  |                       | 0.279  | 0.329 | 0.379 |                   |               |
| Lamp life time      | +25℃ | -                  | Continuation          | 10,000 | -     | -     | hour              | 【Note8-1,6】   |
|                     | -30℃ | -                  | Intermission          | 2,000  | -     | -     | time              | 【Note8-1,7】   |

Applied voltage condition for the measurement :

- i ) Bright adjustment voltage (BRT) to be opened
- ii ) Video signal of standard black level and 100% white level

【Note 8-1】 Measuring method : Fig.5

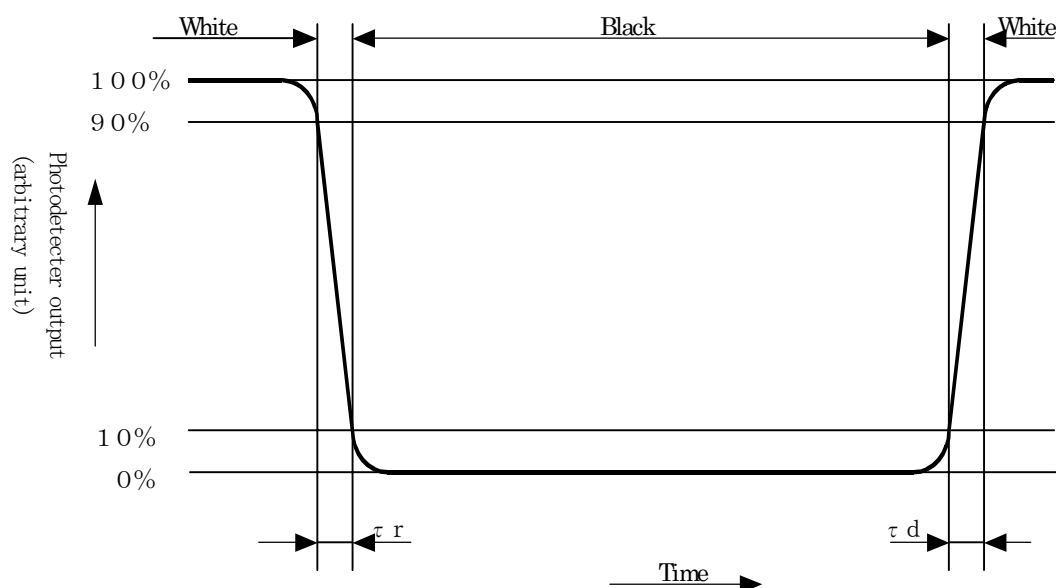
【Note 8-2】 Viewing angle range is defined as follows.



【Note 8-3】 Contrast ratio is defined as follows:

$$\text{Contrast ratio} = \frac{\text{Photodetector output with LCD being "white"}}{\text{Photodetector output with LCD being "black"}}$$

【Note 8-4】 Response time is obtained by measuring the transition time of photodetector output, when input signals are applied so as to make the area "black" to and from "white".



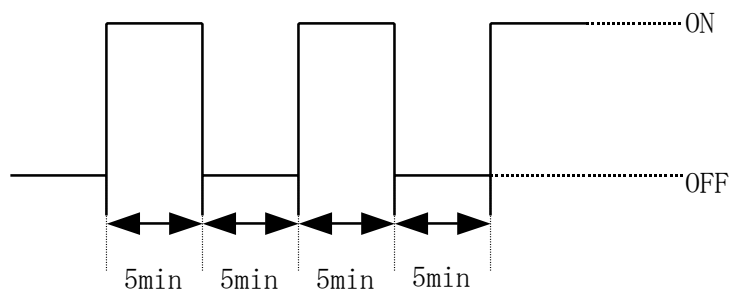
【Note 8-5】 Measured on the center area of the panel at a viewing cone  $1^\circ$

by TOPCON luminance meter BM-7.(After 30 minutes operation)

【Note 8-6】 Lamp life time is defined as the time when brightness not to become under 50% of the original value in the continuous operation under the condition of PWM dimming duty 100%~5% ( $T_a=25^\circ\text{C}$ ).

【Note 8-7】 The intermittent cycles is defined as a time when brightness not to become under 50% of the original value under the condition of following cycle.

Ambient temperature:  $-30^\circ\text{C}$



#### (9) Mechanical characteristics

##### 9-1) External appearance

Extreme defects should not exist. (See Fig. 1)

##### 9-2) Panel toughness

The panel shall not be broken, when 19N is pressed on the center of the panel by a smooth sphere having 15 mm diameter.

Caution: In spite of very soft toughness, if, in the long-term, add pressure on the active area, it is possible to occur the functional damage.

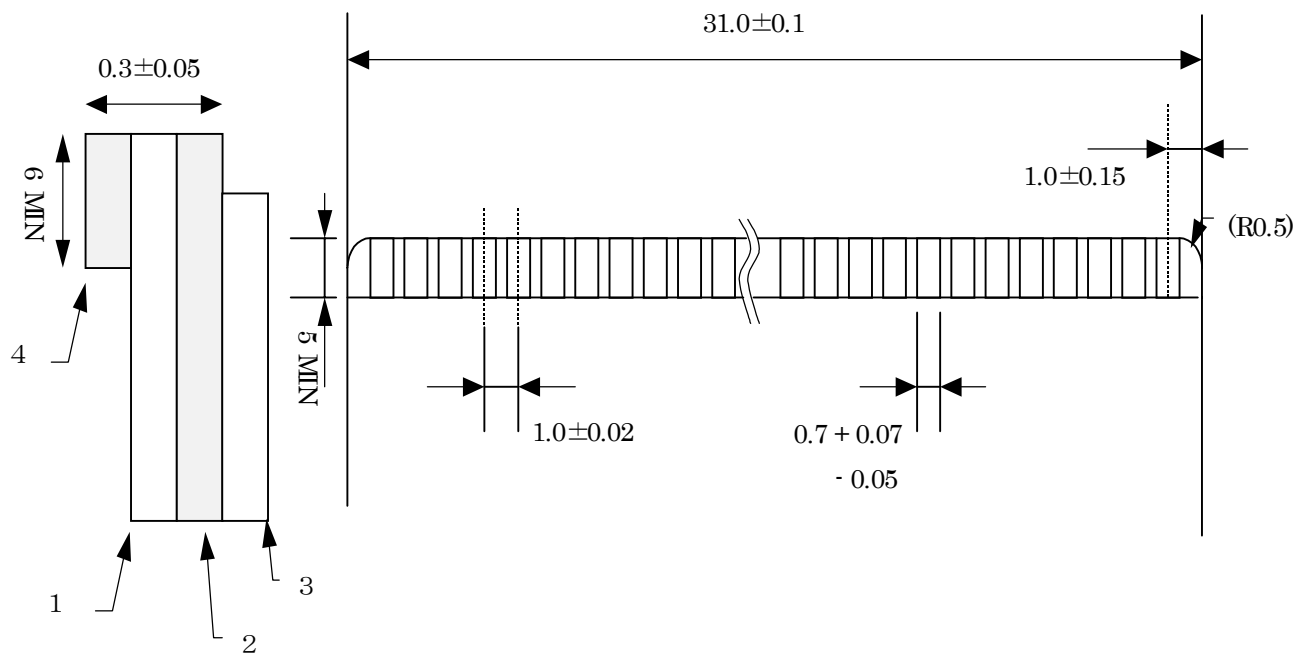


## 9-3) Input/output connector performance

## A) Input/output connectors for the operation of LCD module

(30 pin 【KYOCERA ELCO CORPORATION】 :6200307032800)

- 1) Applicable FPC : Refer the below figure
- 2) Terminal holding force : More than 0.9N/pin.  
(Each terminal is pulled out at a rate of  $25 \pm 3$ mm/min.)
- 3) Insertion/pulling : contact resistance is not twice larger than the durability initial value after applicable FPC is inserted and pulled out 20 times



| No. | Name              | Materials   |
|-----|-------------------|---|
| 1   | Base material     | Polyimide or equivalent material(25 $\mu$ m thick)            |
| 2   | Copper foil       | Copper foil(35 $\mu$ m thick) Solder plated over 2 $\mu$ m    |
| 3   | Cover lay         | Polyimide or equivalent material                              |
| 4   | Reinforcing plate | Polyester polyimide or equivalent material(188 $\mu$ m thick) |

FPC applied to input/output connector (1.0mm pitch)

## (10) Display quality

The display quality of the color TFT-LCD module shall be in compliance with the Incoming Inspection Standard.

## (11) Mechanical Noise

No abnormal mechanical noise which can be easily recognized when the module is shaken by hand.

## (12) Handling instructions

## 12-1) Mounting of module

The TFT-LCD module is designed to be mounted on equipment using the mounting tabs in the four corners of the module at the rear side.

On mounting the module, as the M2.6 tapping screw fastening torque is 0.3 through 0.5N·m is recommended, be sure to fix the module on the same plane, taking care not to wrap or twist the module.

Don't reach the pressure of touch-switches of the set side to a module directly, because images may be disturbed.

Please power off the module when you connect the input/output connector.

## 12-2) Precautions in mounting

Polarizer which is made of soft material and susceptible to flaw must be handled carefully. Protective film (Laminator) is applied on the surface to protect it against scratches and dirt. It is recommended to peel off the laminator immediately before the use, taking care of static electricity.

Precautions in peeling off the laminator

## A) Working environment

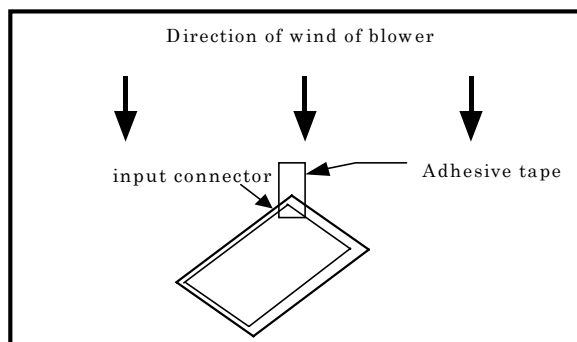
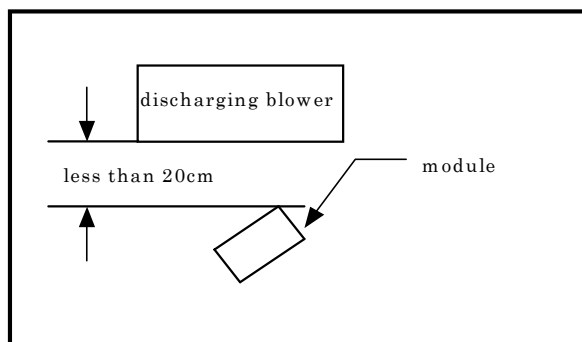
When the laminator is peeled off, static electricity may cause dust to stick to the polarizer surface.

To avoid this, the following working environment is desirable.

- Floor : Conductive treatment of 1MΩ or more on the tile. (conductive mat or conductive paint on the tile)
- Clean room free from dust and with an adhesive mat on the doorway
- Advisable humidity: 50%~70%      Advisable temperature: 15°C~27°C
- Workers shall wear conductive shoes, conductive work clothes, conductive gloves and an earth band.

## B) Working procedures

- Direct the wind of discharging blower somewhat downward to ensure that module is blown sufficiently. Keep the distance between module and discharging blower within 20 cm.
- Attach adhesive tape to the laminator part near discharging blower so as to protect polarizer against flaw.
- Peel off laminator, pulling adhesive tape slowly to your side.
- On peeling off the laminator, pass the module to the next work process to prevent the module from getting dust.



## e) Method of removing dust from polarizer

- Blow off dust with N2 blower for which static electricity preventive measure has been taken. Ionized air gun (Hugle Electronics Co.) is recommended.
- Since polarizer is vulnerable, wiping should be avoided.

But when the panel has stain or grease, we recommend to use adhesive tape to softly remove them from the panel.

When metal part of the TFT-LCD module (shielding lid and rear case) is soiled, wipe it with soft dry cloth. For stubborn dirt, wipe the part, breathing on it.

Wipe off water drop or finger grease immediately. Long contact with water may cause discoloration or spots.

Since TFT-LCD module uses glass which breaks or cracks easily if dropped or bumped on hard surface, handle with care.

Since CMOS LSI is used in this module, take care of static electricity and earth your body when handling.

#### 12-3) Precautions in adjusting module

Adjusting volumes on the rear face of the module have been set optimally before shipment. Therefore, do not change any adjusted values. If adjusted values are changed, the specifications described here may not be satisfied.

#### 12-4) Caution of product design

The LCD module shall be protected against water salt-water by the waterproof cover.

Please take measures to interferential radiation from module, to do not interfere surrounding appliances.

#### 12-5) Mounting direction

Mounting direction of the TFT-LCD module to the application needs to be carefully fixed by evaluating display performance.

#### 12-6) Others

Do not expose the module to direct sunlight or intensive ultraviolet rays for many hours; liquid crystal is deteriorated by ultraviolet rays.

Store the module at a temperature near the room temperature. At lower than the rated storage temperature, liquid crystal solidifies, causing the panel to be damaged. At higher than the rated storage temperature, liquid crystal turns into isotropic liquid and may not recover.

The voltage of beginning electric discharge may over the normal voltage because of leakage current from approach conductor by to draw lump read lead line around. If LCD panel breaks, there may be a possibility that the liquid crystal escapes from the panel. Since the liquid crystal is injurious, do not put it into the eyes or mouth. When liquid crystal sticks to hands, feet or clothes, wash it out immediately with soap. Observe all other precautionary requirements in handling general electronic components.

### (13) Shipping requirements

13-1) Packing form is shown in Fig.8.

#### 13-2) Carton storage condition

① Number of layers of cartons in pile : 10 layers max.

② Environmental condition

• Temperature 0°C to 40°C

• Humidity 60 %PH or less (at 40°C)

No dew condition even at a low temperature and high humidity

• Atmosphere Harmful gases such as acid and alkali which corrode electronic components and wires must not be detected.

• Storage period About 3 months

• Opening of package To prevent TFT-LCD module from being damaged by static electricity, adjust the room humidity to 50%PH or higher and provide an appropriate measure for electrostatic earthing before opening the package.

(14)Reliability test conditions

Reliability test conditions for the TFT-LCD module are shown in Table 10.

(15)Others

15-1)Indication of lot number

The lot number is shown on a label. Attached location is shown in Fig.1(Outline Dimensions).

Indicated contents of the label

|             |            |
|-------------|------------|
| LQ065T5AR01 | ○○○○○○○○○○ |
| model No.   | lot No.    |

|                     |                                      |        |    |                         |                     |
|---------------------|--------------------------------------|--------|----|-------------------------|---------------------|
| Contents of lot No. | the 1 <sup>st</sup>                  | figure | ·· | production year         | (ex.1999 : 9)       |
|                     | the 2 <sup>nd</sup>                  | figure | ·· | production month        | 1,2,3,·····,9,X,Y,Z |
|                     | the 3 <sup>rd</sup> ~8 <sup>th</sup> | figure | ·· | serial No.              | 00001~              |
|                     | the 9 <sup>th</sup>                  | figure | ·· | revision marks          | blank or A,B,C ···  |
|                     | the 10 <sup>th</sup>                 | figure | ·· | production factory code | blank or A,B,C ···  |

Reliability test conditions for TFT-LCD module

Table 10

Remark)

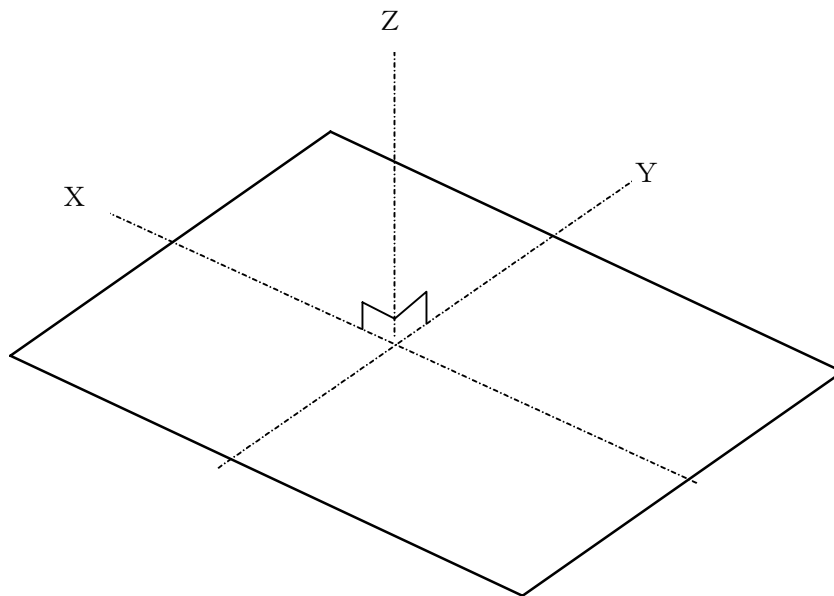
Temperature condition is based on operating temperature conditions on (6)-Table 5

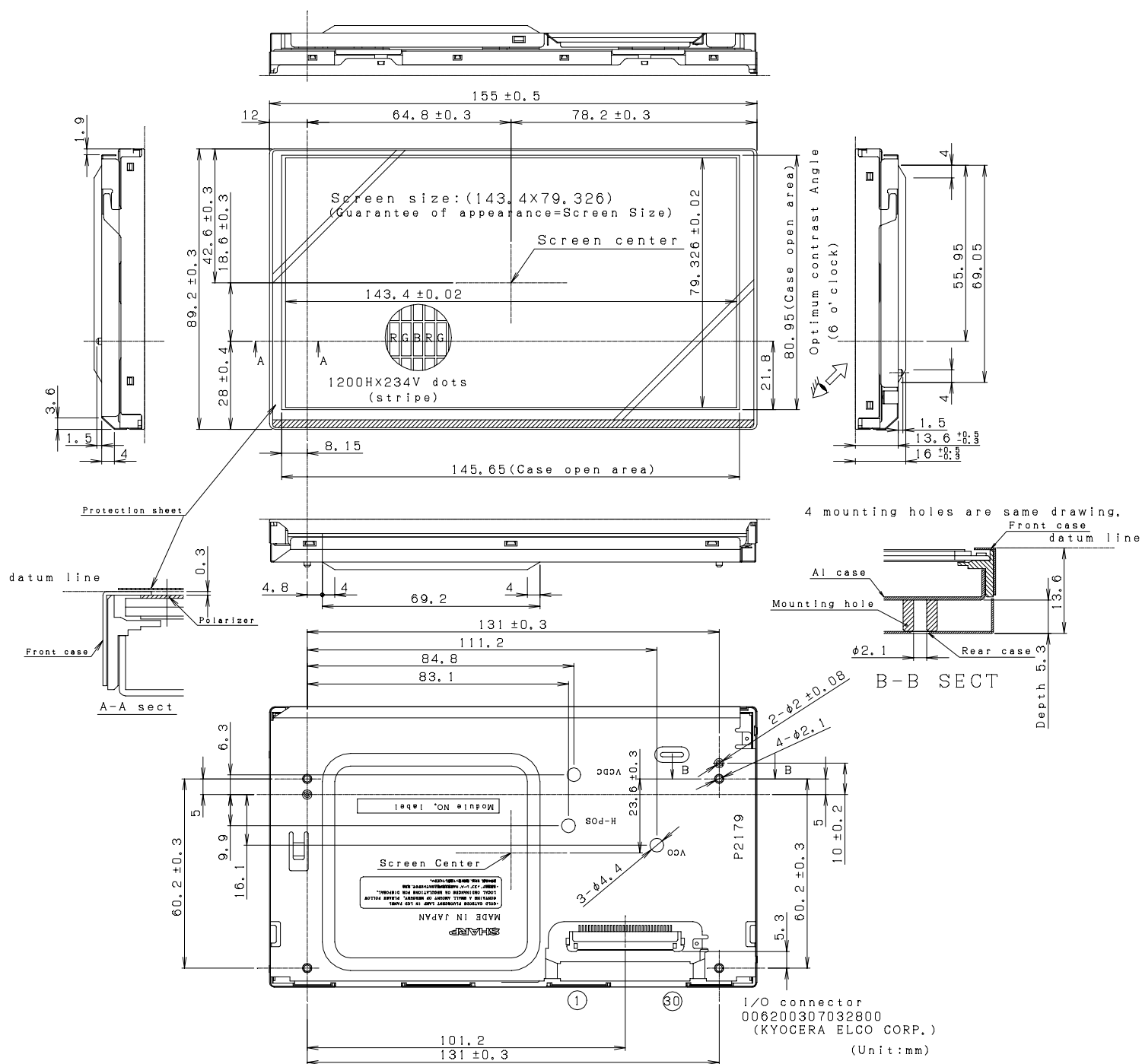
| No. | Test items  | Test conditions   |
|-----|---|---|
| 1   | High temperature storage test                     | Ta=+85°C 240h   |
| 2   | Low temperature storage test                      | Ta=-40°C 240h   |
| 3   | High temperature And high humidity operating test | Ta=+60°C, 90%RH 240h  |
| 4   | High temperature operating test                   | Tp=+85°C (Ta=+65°C) 240h  |
| 5   | Low temperature operating test                    | Ta=-30°C 240h   |
| 6   | Electro static discharge test                     | ±200V, 200pF(0Ω) 1 times for each terminals   |
| 7   | Shock test  | 980m/s <sup>2</sup> ·6ms, ±X, ±Y, ±Z 3times for each direction (JIS C0041,A-7 condition C)  |
| 8   | Vibration test                                    | Frequency range : 8~33.3Hz<br>Stroke : 1.3mm<br>Sweep : 33.3Hz~400Hz<br>Acceleration : 28.4 m/s <sup>2</sup><br>Cycle : 15 minutes<br>X,Z 2 hours for each directions, 4 hours for Y direction (total 8 hours) 【caution】<br>(JIS D1601) |
| 9   | Heat shock test storage test                      | Ta=-30~+85°C / 200cycles<br>(0.5h) (0.5h)   |

【Note】 Ta=Ambient temperature, Tp=Panel temperature

【Check items】 In the standard condition, there shall be no practical problems that may affect the display function.

【Caution】 X,Y,Z directions are shown as follows





note1) General tolerance is  $\pm 0.5$

note2) Unit is mm

note3) Take care in set design to hide the scratches and bubbles appeared on the polarizer or other frame area which is located outside of active area.

Since this module is under development, all the specified value is tentative. The technical literature is subject to change without notice.

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DEVELOPMENT ENGINEERING DEPT. ?  
TFT DIVISION 1  
TFT LIQUID CRYSTAL DISPLAY GROUP  
SHARP CO., LTD.

DRAWING No LCM-01021D DATE 2001.12.11

Fig.1 Outline dimensions of TFT-LCD module

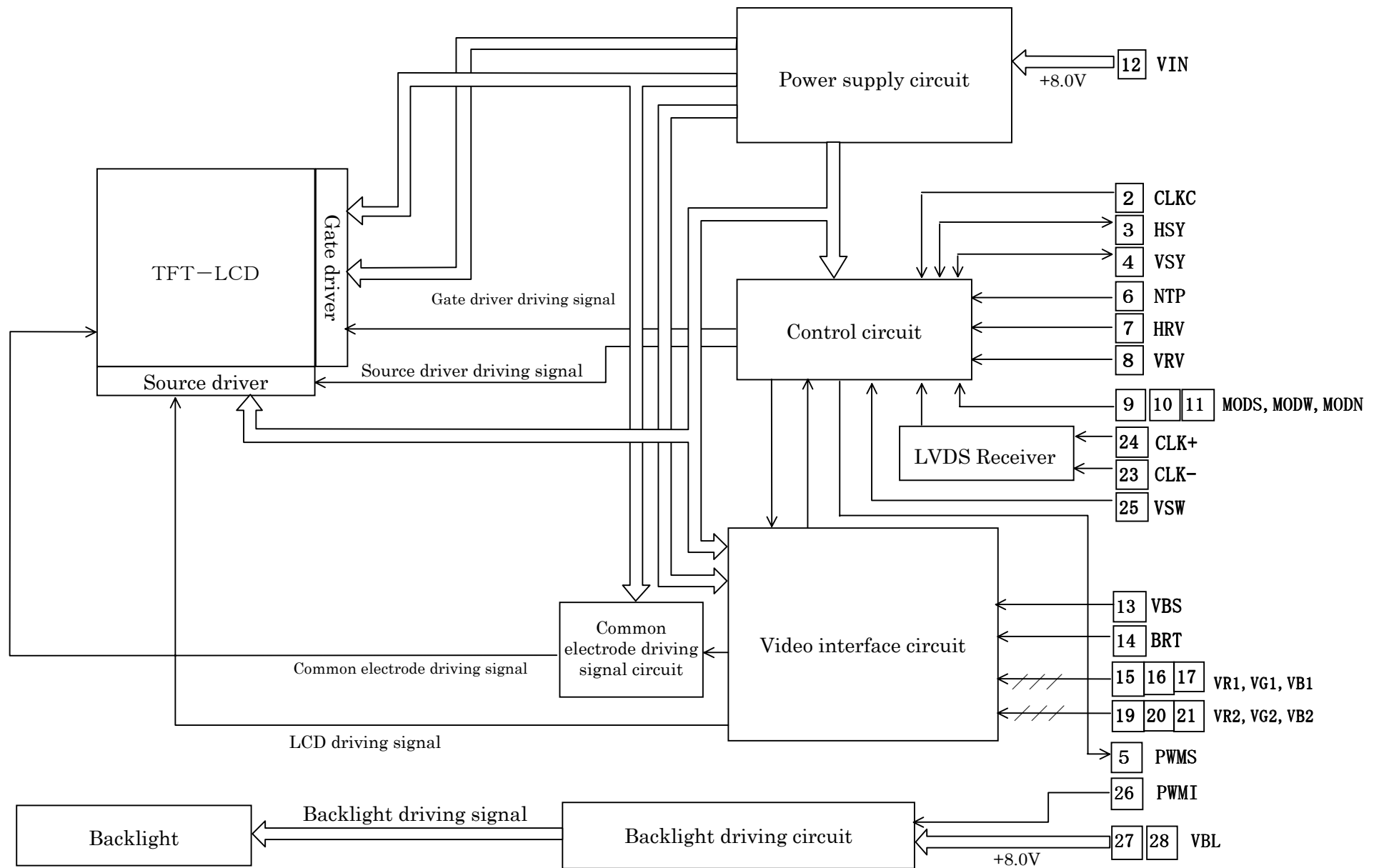
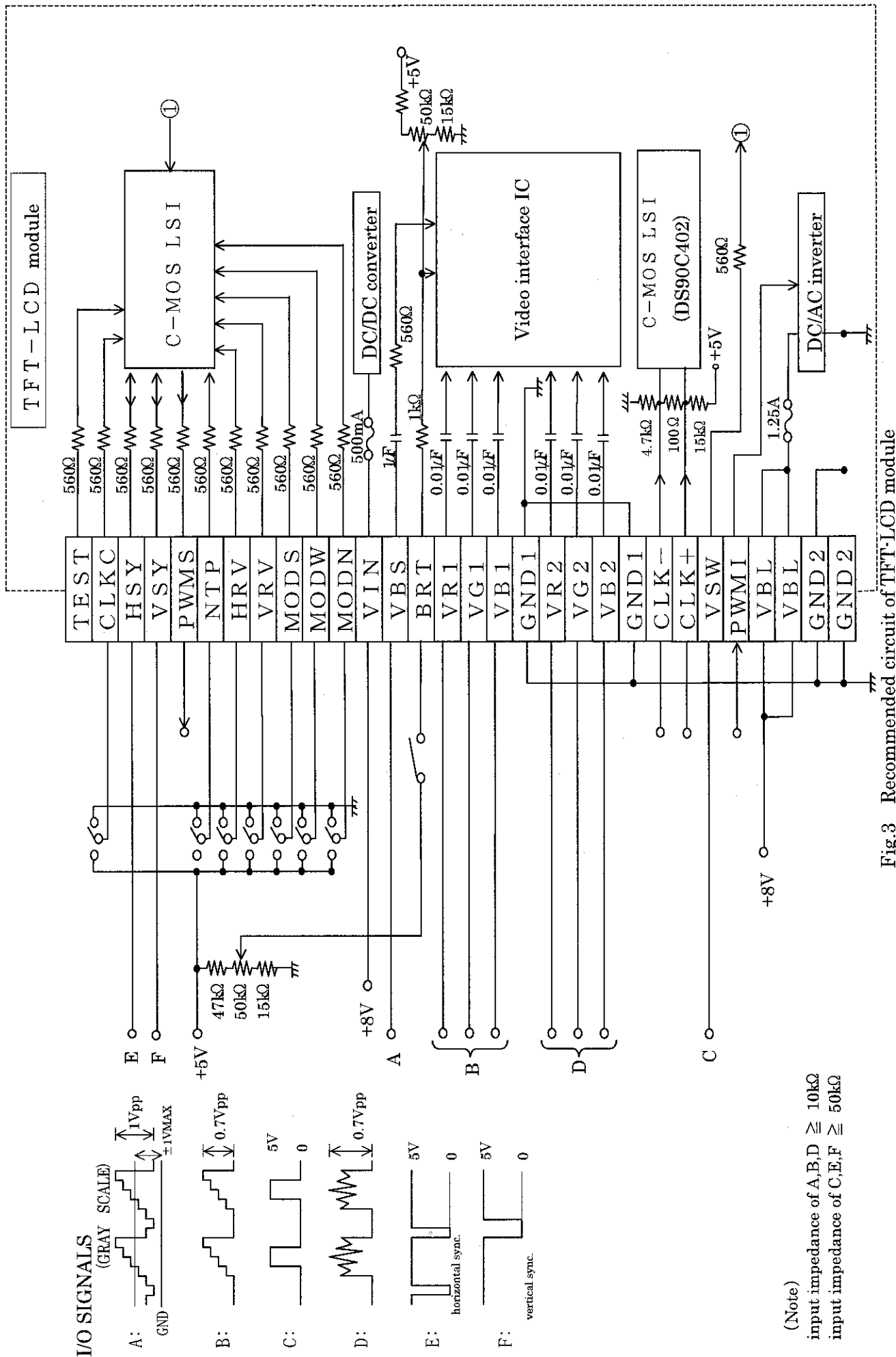


Fig.2 Circuit block diagram of the module





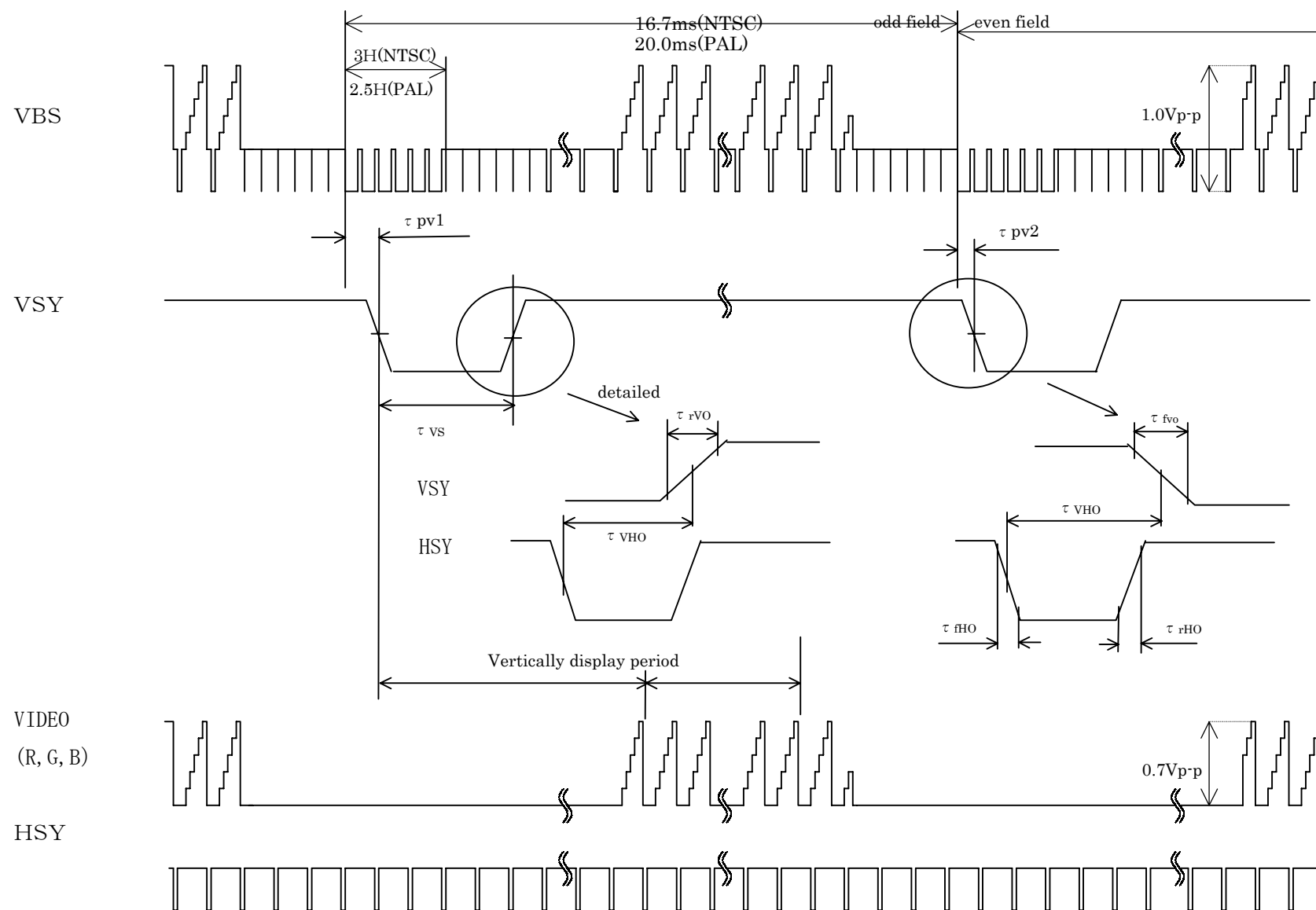


Fig.4-A Input / Output signal waveforms (CLKC=" Hi" )

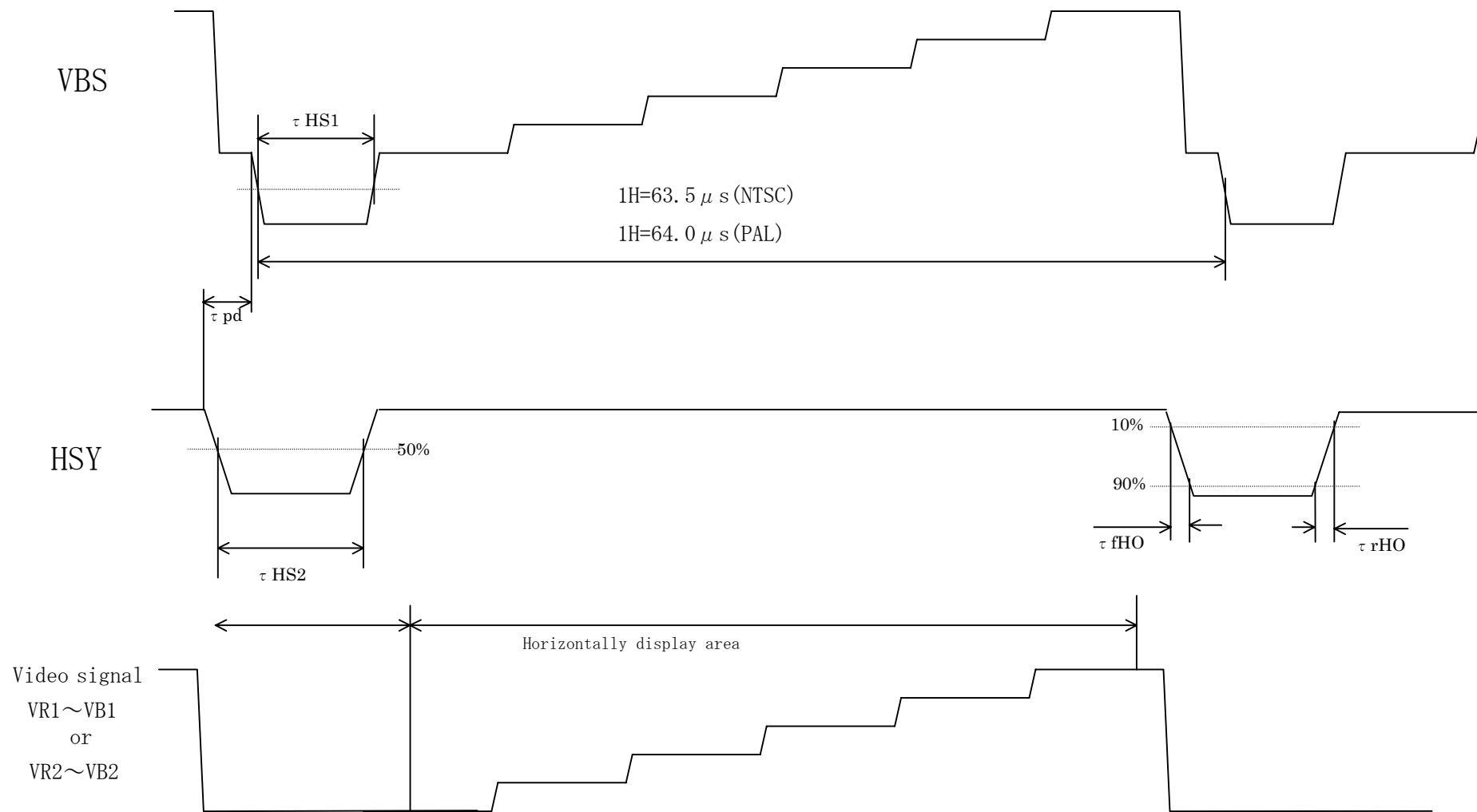


Fig.4-B Input/Output signal waveforms (CLKC=" Hi" )

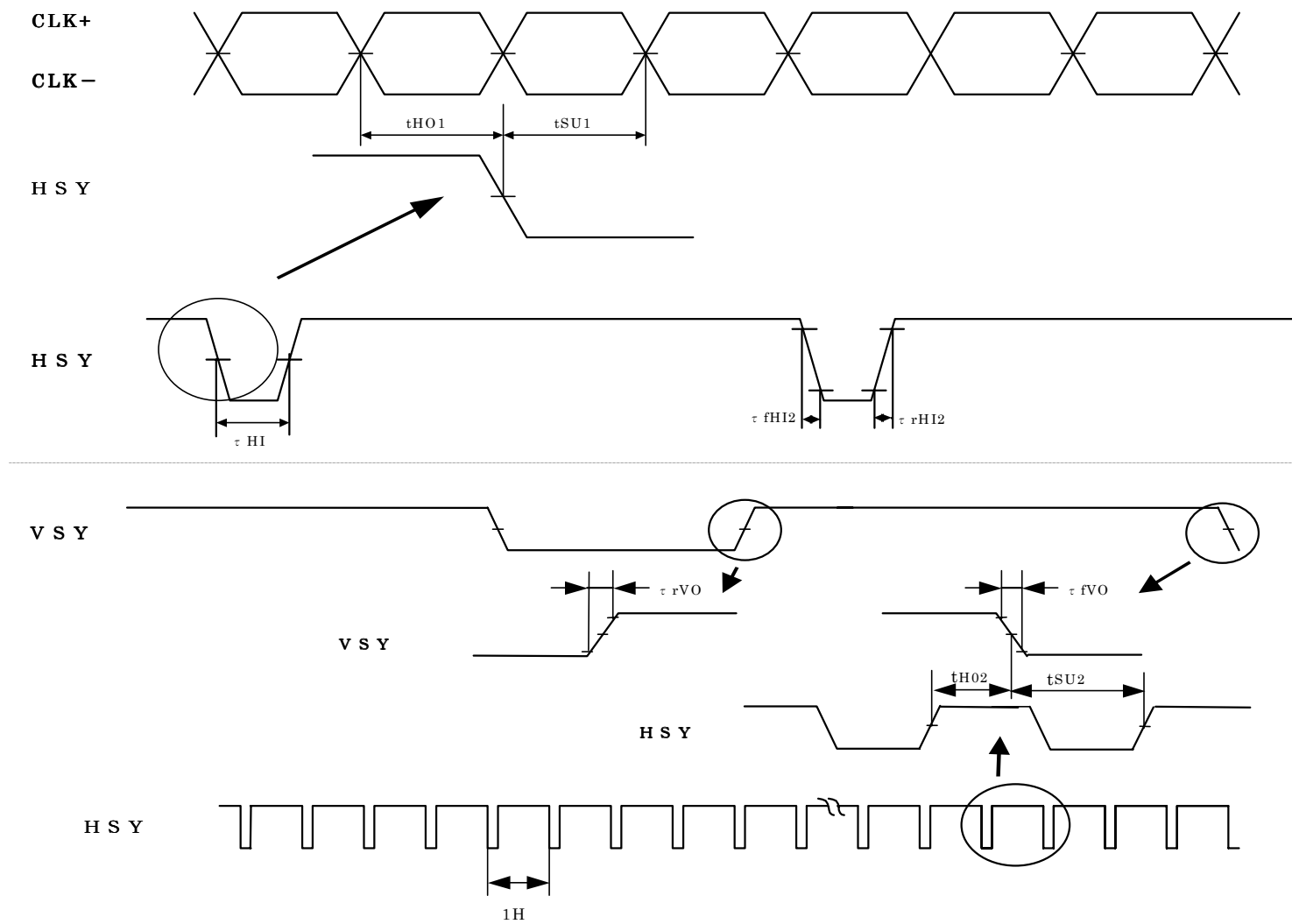


Fig. 4-C Input/Output signal waveforms (external clock mode NTP="Hi", CLKC="Lo")

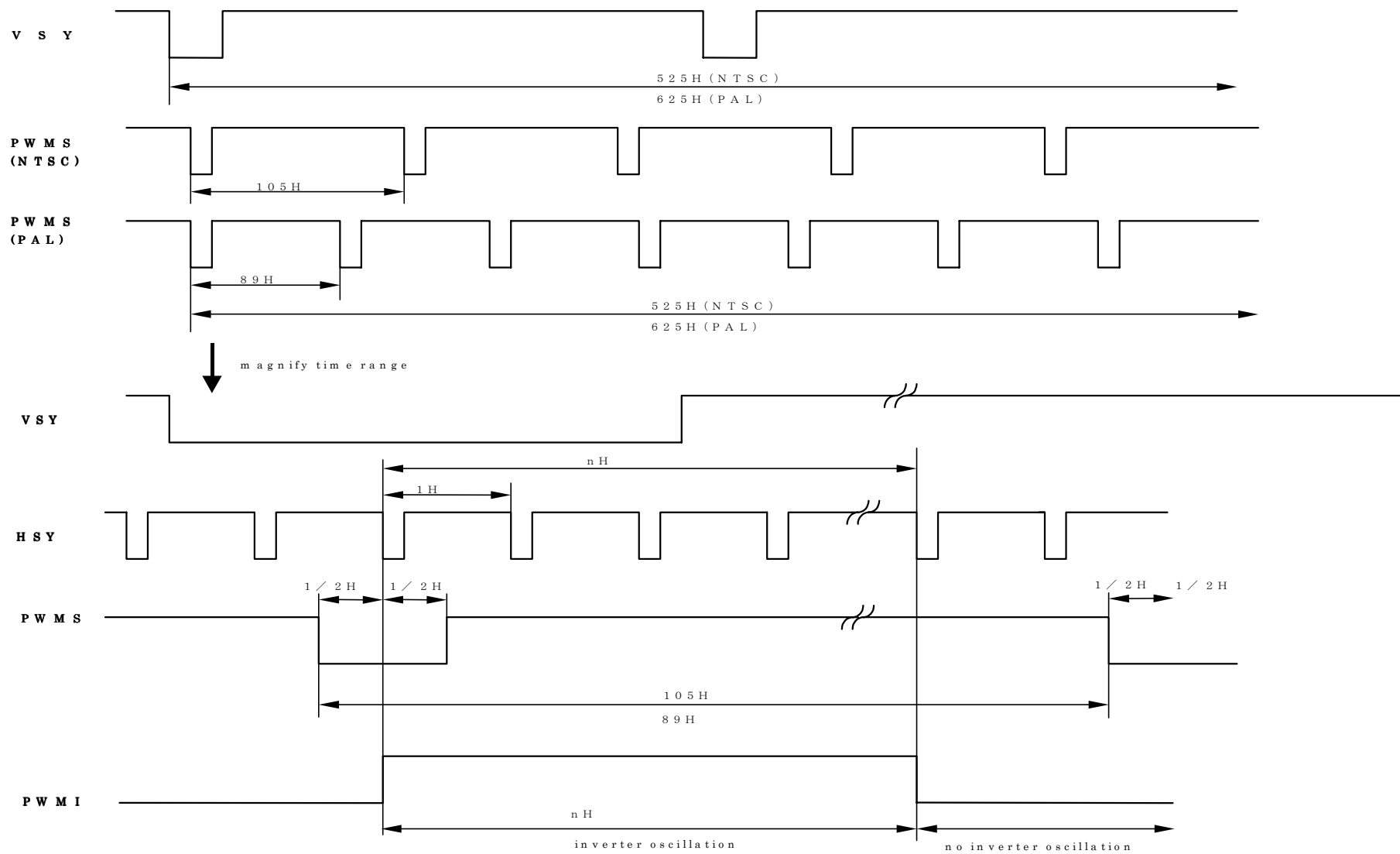


Fig. 4-D PWM dimming timing

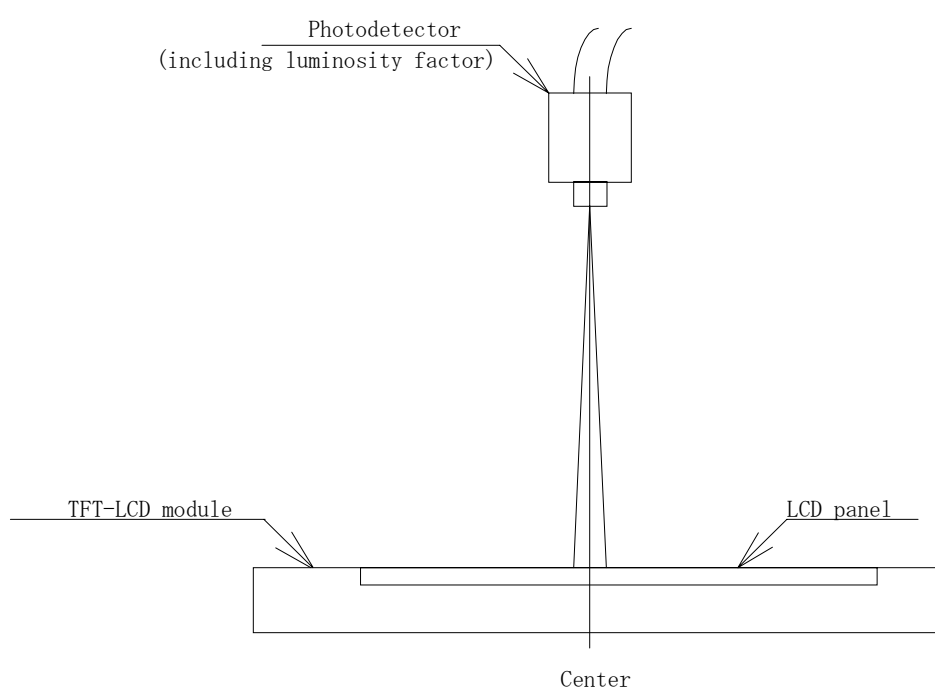


Fig. 5 Measuring method of optical characteristics

## 【Reference】

## Clock and Video signal timing

## [Input Condition]

|                    |   |
|--------------------|---|
| DotClock frequency | f CLK = 8.0MHz  |
| Hsyn. frequency    | fH=15.748kHz  |
| Vsyn. Frequency    | fV=60.107Hz   |
| Video Signal       | Cross-Hatching<br>(To show white lines every 24 dots with the background display of Balck)<br>Amplitude = 0.7Vpp<br>TVr=TVf=17ns<br>TVH=125ns |

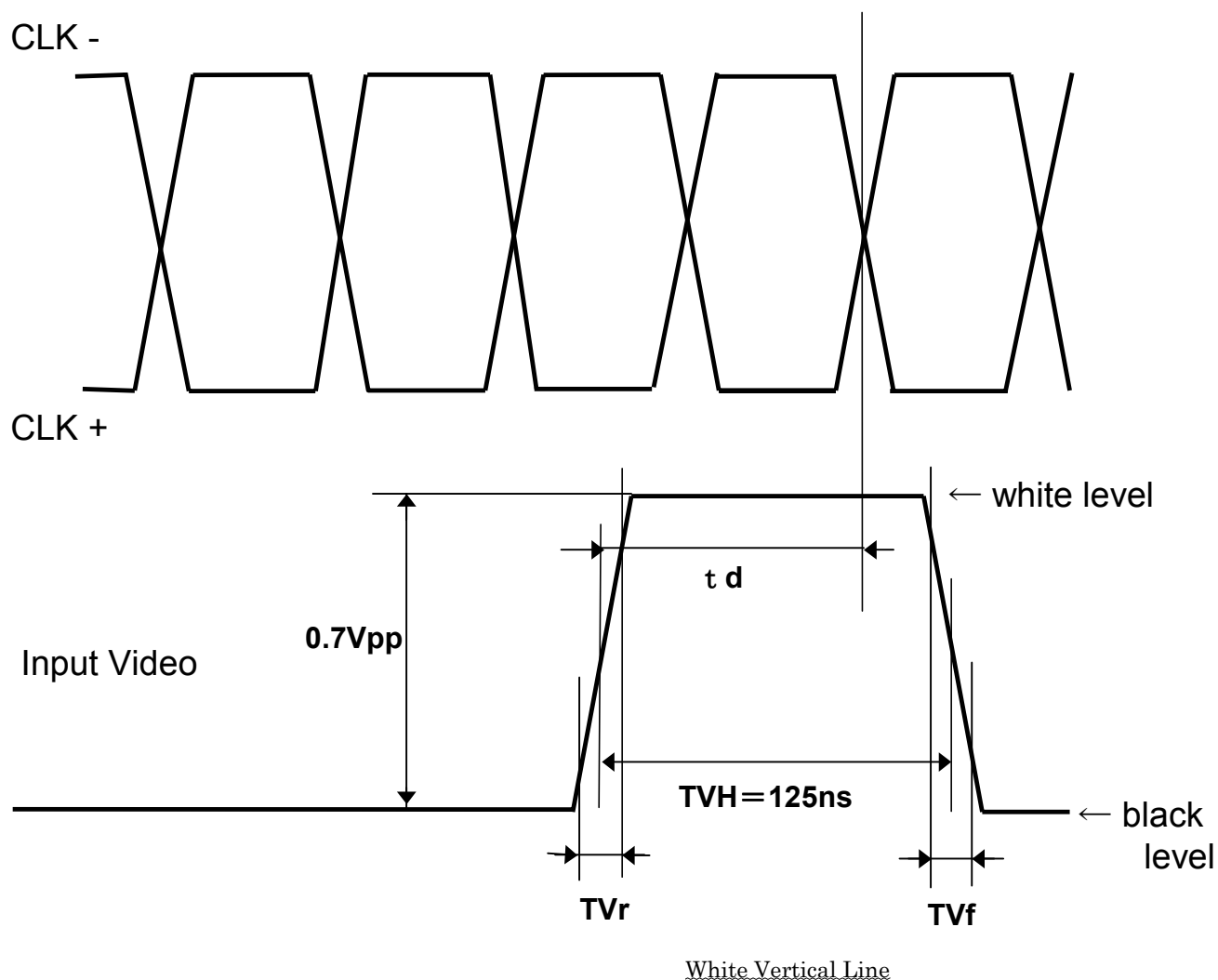


Fig.6 Clock and Video signal timing

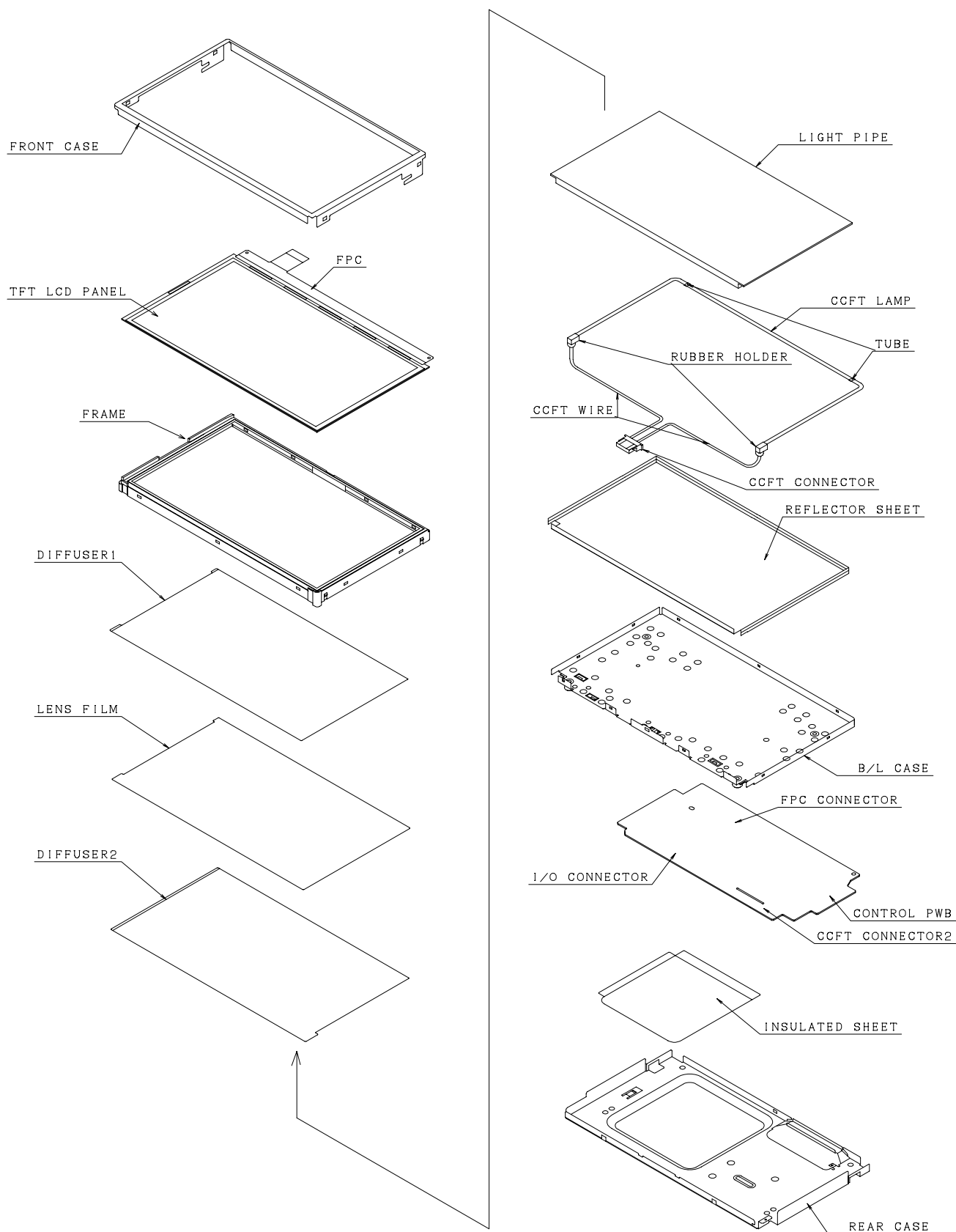


Fig.7 Construction of TFT-LCD module

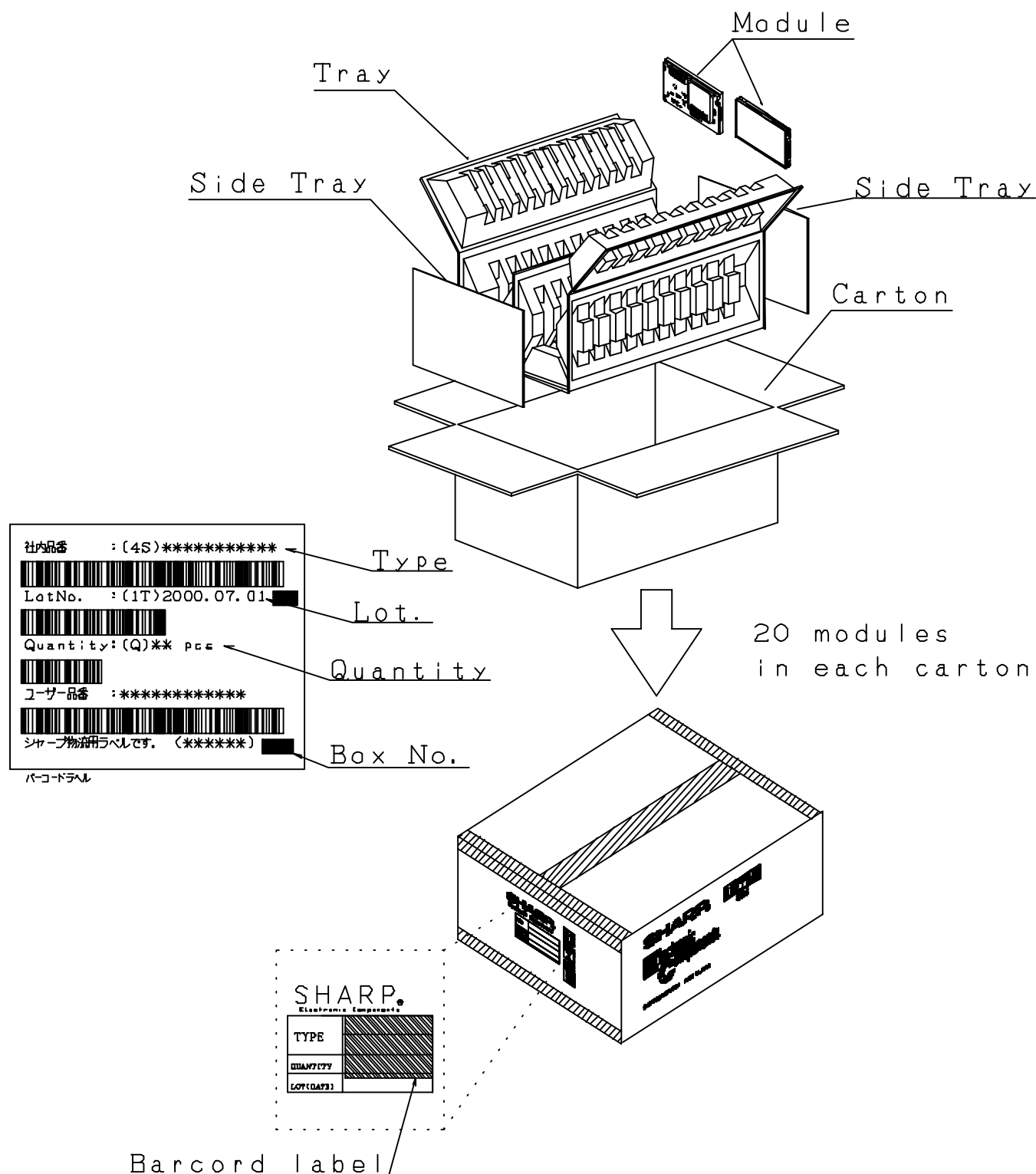


Fig.8 Packing form



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