Preliminary

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Product Technical Brief
S3C2416
May 2008

Overview

SAMSUNG's S3C2416 is a 32/16-bit RISC cost-effective, low power, high performance micro-processor solution for general applications including the GPS Navigation and Mobile Phone markets. Additionally, in order to allow for lower system costs, higher performance and low power, the S3C2416 is fabricated using the 65nm low power CMOS process.

The S3C2416 carries revolutionary upgrades with respect to the S3C2412. Most notably, an upgrade to the ARM926EJ core, the integration of a 2D Graphics Accelerator, an added low power mode, as well as embedded internal ROM/RAM for secure boot, moviNAND booting and low power audio decoding. Furthermore, peripheral and feature upgrades have also been made to increase performance, as well as flexibility. Examples include a USB 1.1 host, in addition to a USB 2.0 high speed device, dual MMC ports, HS-SPI ports as well as other upgraded memory interfaces.

All in all, the S3C2416 presents a low-cost, highly embedded solution with upgraded features.

Features Summary

- ARM926EJ CPU 266/400MHz with 16KB I-cache and 16KB D-cache
- Dual port external memory controller: DRAM/ROM control and chip select logic
- 64KB internal general purpose SRAM
- 32KB internal ROM for moviNAND booting
- LCD controller with DMA-dedicated: 24bpp, 2-PIP
- 2D graphics accelerator
- 6-ch DMAs with external request pins
- 4-ch UART (3Mbps) with IrDA 1.0 (64B FIFO)
- 1-ch HS-SPI (50Mbps)
- 1-ch IIC: multi-master
- 1-ch IIS: PCM and AC97 I/F
- 2-ch SD/SDIO/MMC
- 1 port USB Host v1.1 full speed
- 1 port USB Device v2.0 high speed
- 4-ch PWM timers & 1-ch internal timers
- Real time clock & Watch dog timer
- 2 PLLs with on-chip clock generator
- Power modes: Normal, Idle, Stop & Deep Stop, Sleep and Power-off
- 10-ch 12-bit ADC (Touch screen interface)
- 65nm low-power technology and MtCMOS technology incorporated
- Package
  - 330-pins FBGA (0.65mm Pitch), 14 x 14 x 1.7mm

Functional Block Diagram

System peripheral

- RTC
- PLL x2
- Timer w/ PWM
- Watch dog timer
- DMA 6ch

ARM core

ARM926EJ

I/D-cache 16KB / 16KB
266MHz @ 1.1V
400MHz @ 1.2V

Multimedia accelerator

- CSC & Scaler
- 2D Graphics

Connectivity

- 24bit I2S 1x
  PCM & AC97
- I2C x1
- GPIO
- UART x4
- IrDA v1.0
- 1x HS-SPI
- 2x SDIO/SD/MMC
- USB Device 2.0
- USB Host 1.1
- 12-bit ADC x10

Secure ROM

64KB SRAM

32-bit Multi-layer AHB Bus

Power management

Normal, Idle
Stop, Deep Stop,
Sleep

TFT LCD Controller

24/18bit or
8bit for Dual i80
1024x1024 output
2-layer PIP
16bit a-blending

Memory sub-system

- SRAM/ ROM/
  NOR/ OneNAND
- SDRAM x32
  Mobile SDRAM x32
- mDDR/DDR2 x16
- NAND flash
  1/4/8bit HW ECC
  4KB page read

Product Details

CPU and core

■ Architecture

- Integrated system for hand-held devices and general embedded applications
- 32/16-Bit RISC architecture and powerful instruction set with ARM926EJ-S CPU core
- Enhanced ARM architecture MMU to support Windows CE, Windows mobile, Symbian, Linux, and other High Level OS
- Instruction cache, data cache, write buffer and Physical address TAG RAM to reduce the effect of main memory bandwidth and latency on performance
- Internal Advanced Microcontroller Bus Architecture (AMBA2.0, AHB/APB)

■ Cache Memory

- 64-way set-associative cache with I-cache (16KB) and D-cache (16KB)
- 8 words length per line with one valid bit and two dirty bits per line
- Write-through or write-back cache operation to update the main memory
- The write buffer can hold 16 words of data and four addresses.

Memory sub-system

■ ROM / SRAM / NAND / NOR interface

- NAND flash memory for boot loader and data storage
  - x8, x16 data bus and No density/size limit
  - 1/4/8-bit ECC HW for MLC NAND flash
  - 4KB page read mode
  - 1.8V, 2.5V or 3.3V Interface Voltages
  - 64KB internal buffer (stepping stone)
- OneNAND/SRAM/ROM/NOR flash interface
  - x8, x16 data bus
  - Address support up to 64MB NOR flash
  - 1.8V, 2.5V or 3.3V interface voltages

■ DRAM interface

- Standard SDRAM interface
  - Bus speed up to 133MHz with x32 data bus
  - 1.8V, 2.5V or 3.3V interface voltages
  - Density support: Up to 1Gbit
- Mobile SDRAM interface
  - Bus speed up to 133MHz with x32 Data Bus
  - 1.8V Voltage
  - Mobile SDRAM feature support
    - * DS: Driver strength control
    - * TCSR: Temp. compensated self-refresh control
    - * PASR: Partial array self-refresh control
- Mobile DDR, DDR & DDR2 interface
  - 266Mbps/pin double data rate with x16 data bus
  - 1.8V interface voltage
  - Density support: Up to 1Gbit

Multimedia accelerator

■ TFT-LCD interface

- Support up to 24 bit RGB Interface LCD
  - 1/2/4/8bpp Palletized or 8/16/24-bpp Non-Palletized color TFT-LCD support
- Support 8/6 bit RGB or dual i80 Interface LCD
- 320X240, 640x480 or other display resolutions up to 1024x1024
- Maximum 2K x 2K virtual screen size (4MByte)
- Support 2-window layer for PIP or OSD
- Real time overlay plane multiplexing
- Programmable OSD window positioning
- 16-level alpha blending
- ITU-R 601 format output

■ STN-LCD interface

- Supports 3 types of LCD panels: 4-bit dual scan, 4-bit single scan, and 8-bit single scan display
- Supports monochrome, 4/16 gray levels
- Supports 256 to 4096 colors
- Supports multiple screen size
- Maximum virtual screen size is 4Mbytes
- Supports 4bit/8bit LCD driver I/F

■ 2D Graphic Accelerator

- Primitive drawing engine
  - Line/Point drawing
  - Bit Block Trasfer (BitBLT)
  - Color expansion: Text drawing
- Per-pixel operation (max 2048x2048 resolution)
  - 90°/180°/270°/X-flip/Y-flip rotation
  - Window clipping
  - Rasterization
  - 256-level per-pixel alpha blending

■ A/D Converter (Touch Screen Interface)

- 10-ch multiplexed ADC
- Max 500K samples/sec and 12bit resolution
- Internal FET for direct Touch Screen interface

System & Peripherals

■ Clock & power manager

- On-chip MPLL and EPLL:
  - MPLL: the clock to operate CPU
  - EPLL: the clock to operate USB Host/Device
- Clock can be fed selectively to each function block by software
- Power mode

  - Normal mode: Normal operating mode
  - Slow mode: Low frequency clock without PLL
  - Idle mode: CPU Clock is stopped
  - Stop mode: All PLL's disabled, thus stopping the peripheral clocks, as well as the CPU clock
  - Deep Stop mode: All Clocks disabled and power to the CPU is disabled as well.
  - Sleep mode: Power to the internal logic, as well as the CPU, is disabled
- Wake up by EINT[15:0] or RTC alarm interrupt from Power-Off mode
- *Low Power MtCMOS technology*

■ Interrupt controller

- Interrupt sources
- Level/Edge mode on external interrupt source
- Programmable polarity of edge and level
- Supports Fast Interrupt request (FIQ) for very urgent interrupt request

■ DMA controller

- 6 channel programmable DMA controller with DMA burst operation (plus dedicated DMAs)
- Supports memory to memory, IO to memory, memory to IO, and IO to IO transfers
- Burst transfer mode to enhance the transfer rate

■ Internal SRAM and ROM

- 32KB internal ROM for secure boot and NAND/OneNAND/moviNAND booting purpose
- 64KB internal SRAM for low power audio and secure RAM purpose

■ RTC (Real Time Clock)

- Full clock feature: second, minute, hour, date, day, month, and year
- 32.768 KHz operation with fine-tuned clock source
- Alarm and time tick interrupt

■ Timers with PWM

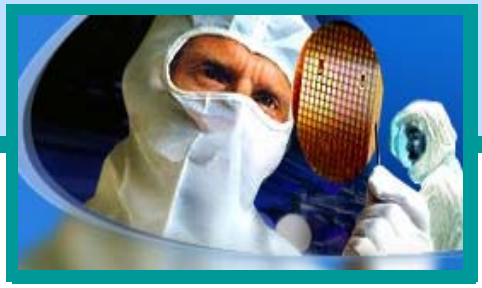
- 4 channel 16-bit PWM timers & 1 channel 16-bit general purpose internal timers: DMA or INT mode
- Programmable duty cycle, frequency, and polarity
- Dead-zone generation
- Supports external clock sources

■ Watchdog Timer

- 16-bit Watchdog Timer
- Interrupt request or system reset at time-out

■ eFuse

- Chip ID purpose



Connectivity

■ UART

- 4 channel UART with DMA-based or interrupt-based operation
- Supports 5-bit, 6-bit, 7-bit, or 8-bit serial data transmit/receive (Tx/Rx)
- Supports external clocks for the UART operation (UCLK)
- Programmable baud rate up to 3Mbps
- Supports IrDA 1.0 (115.2Kbps)

■ USB Device

- 1 channel USB Device including PHY transceiver
- Compatible with USB Specification version 2.0 High Speed (480Mbps) with 9 end-points

■ USB Host

- 1 channel USB host, compatible with USB Specification version 1.1 full speed (big endian)

■ SD/MMC Host Interface

- 2 channel SD/SDIO/MMC
- Compatible with SDIO Card Protocol version 1.0
- Compatible with Multimedia Card Protocol version 2.11 (MMC)
- 512Byte FIFO for Tx/Rx
- DMA based or Interrupt based operation

■ HS-SPI Interface

- 1 channel HS-SPI (50Mbps)
- 64Byte FIFO for Tx/Rx
- DMA-based or interrupt-based operation

■ General Purpose Input/Output Ports

- 16 external interrupt ports
- Multiplexed input/output ports

■ IIS-Bus Interface

- 1 channel of Dolby 5.1 supporting IIS-bus for audio interface with DMA-based operation
- Serial, 8-/16-bit per channel data transfers
- 128 Bytes (64-Byte + 64-Byte) FIFO : 4 FIFO
- Supports IIS format and MSB-justified data format
- Support full duplex mode

■ PCM Audio I/F

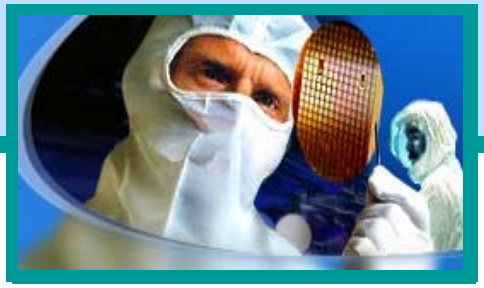
- 16-bit mono audio I/F and master mode only
- 1 channel muxed with IIS

■ AC97 Audio I/F

- Independent channels for stereo PCM In, stereo PCM Out, mono MIC In.
- 16-bit stereo(2-channel) audio
- Variable sampling rate AC97 Codec interface (48KHz and below)
- 1 channel muxed with IIS

■ IIC-Bus Interface

- 1 channel multi-master IIC-Bus
- Serial, 8-bit oriented and bi-directional data transfers can be made at up to 100 Kbit/s in Standard mode or up to 400 Kbit/s in Fast mode



Electrical Characteristics

■ Operation conditions

- Supply voltage for core and logic
  - 266MHz @ 1.1V
  - 400MHz @ 1.2V
- External memory interface: 1.8V / 2.5V / 3.3V
- External IO interface: 3.3V

❒ Package information

- Package type: 330-pins FBGA (0.65mm Pitch)
- Dimension: 14 x 14 x 1.7mm