

50MHz CLOCK OUT
Generate by IP101A

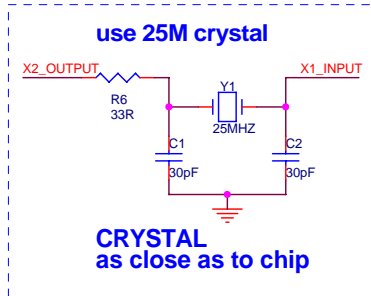
P3 50MHz_CLKOUT >> 50MHz_CLKOUT

Set IP101A
to RGMII Mode

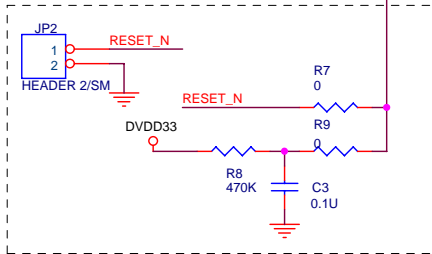
IP101A

BANDGAP
RESISTOR

RGMII Signals

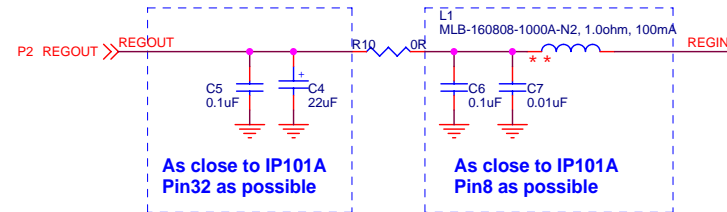
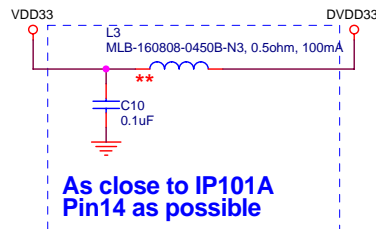
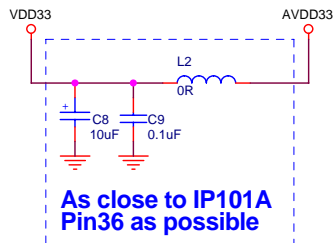


Pin48 could be short VDD33 if
interrupt funtion is not
used.




Hardwire Configuration network:

1. This configuration shows
Enable: Auto negotiation, Full duplex, 100Mbps,
Link Down Power Saving, RGMII interface
Disable: Isolate, Repeater mode
2. These seven configuration pins could be connected
to VDD or GND directly.



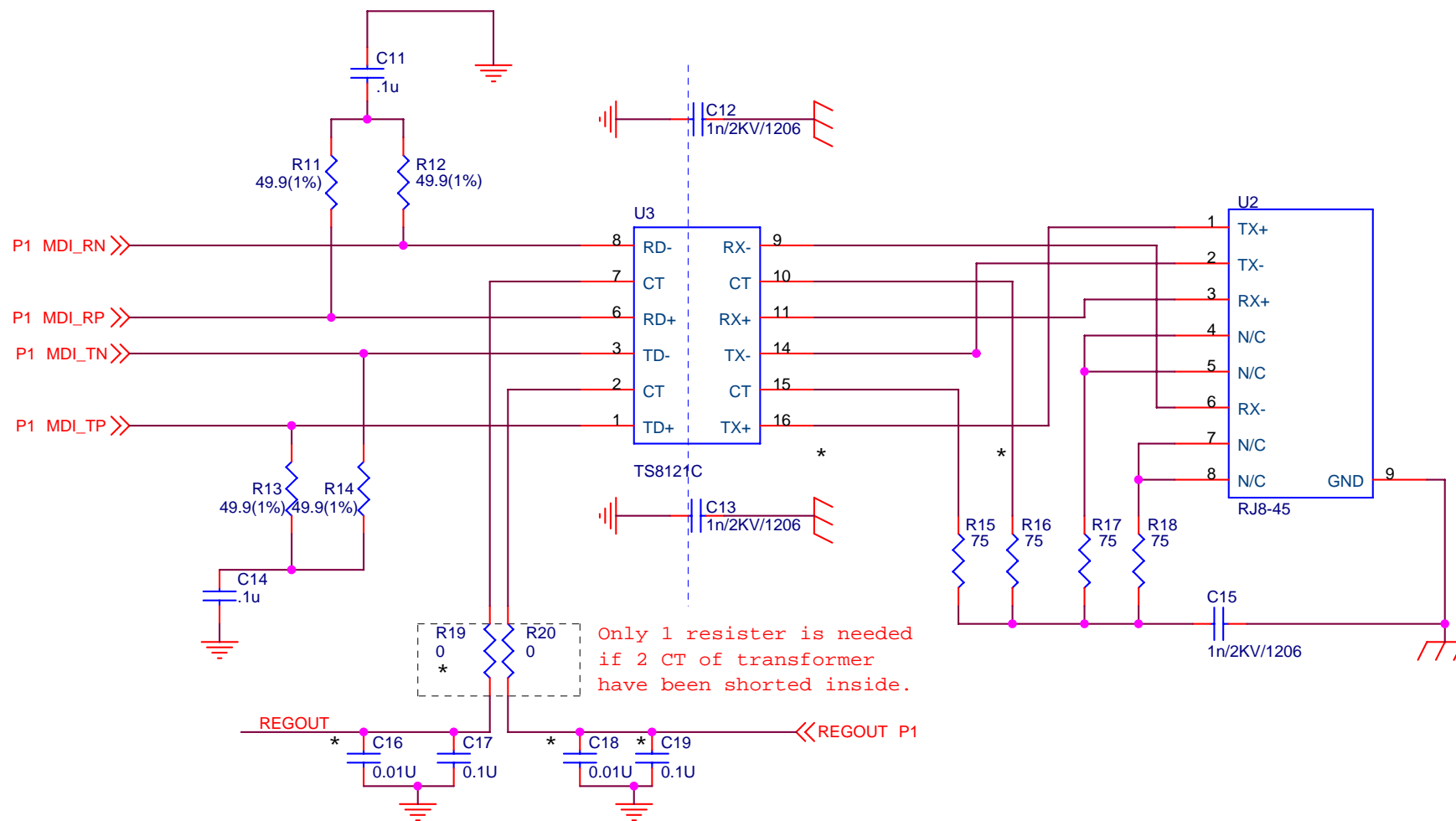
** Bead should be placed as close to IP101A
as possible and in the same side as IP101A.



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Title IP101A Chip Circuit Diagram		
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* : Optional ,but recommended



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Title

IP101A Chip Circuit Diagram

Size
A

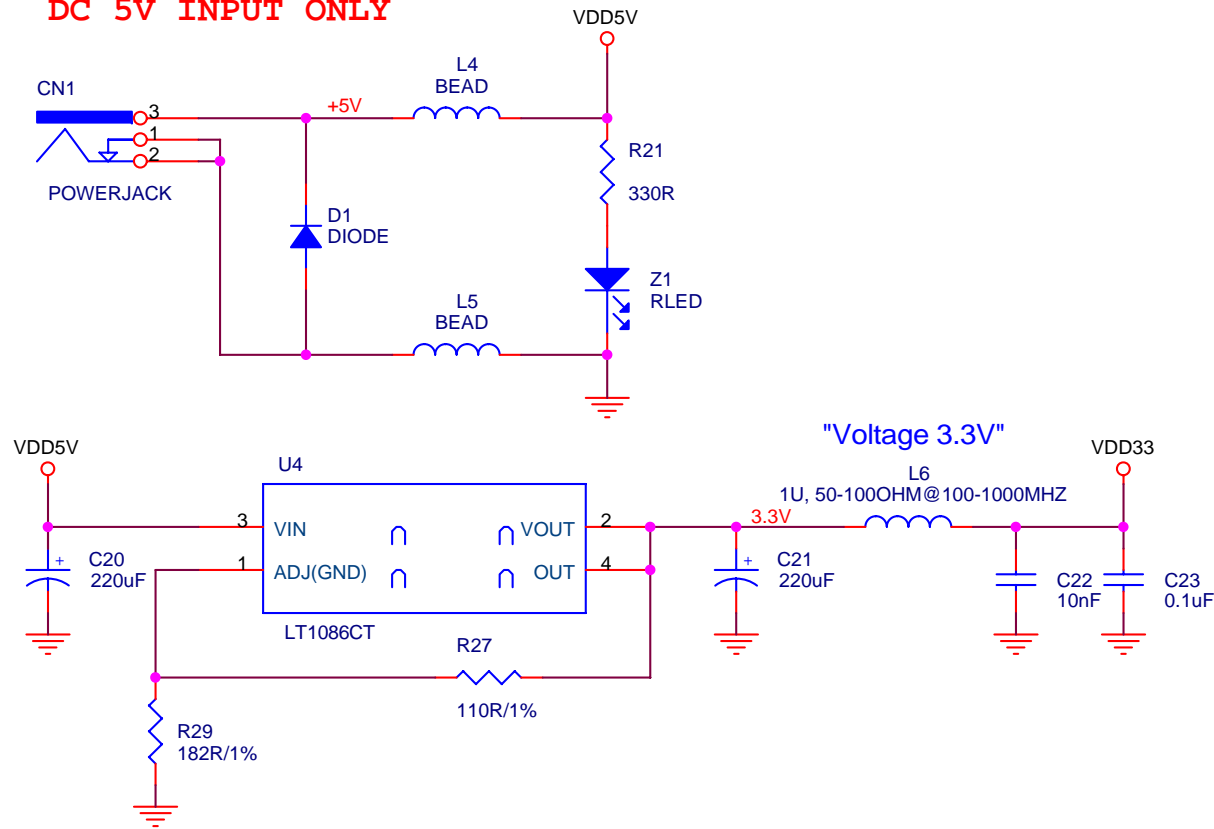
Document Number
RMII UTP

Rev

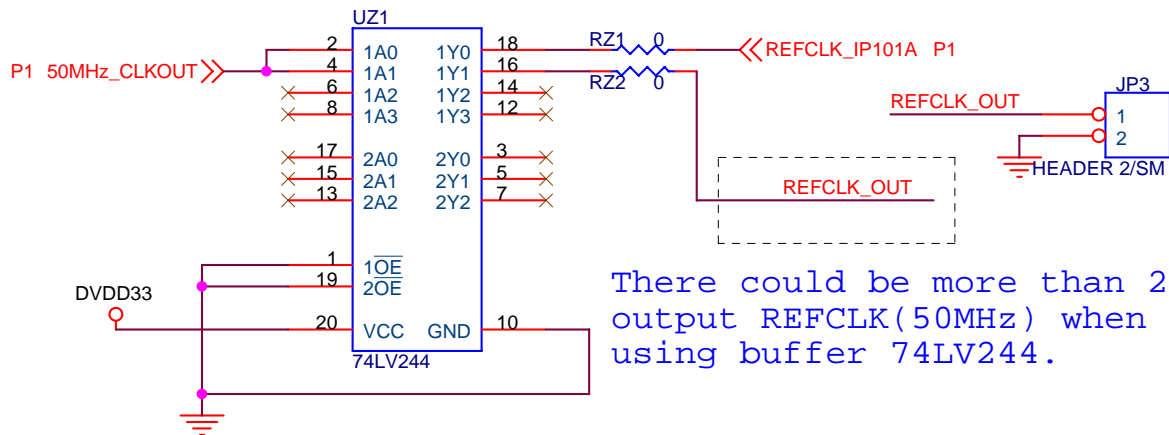
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DC 5V INPUT ONLY



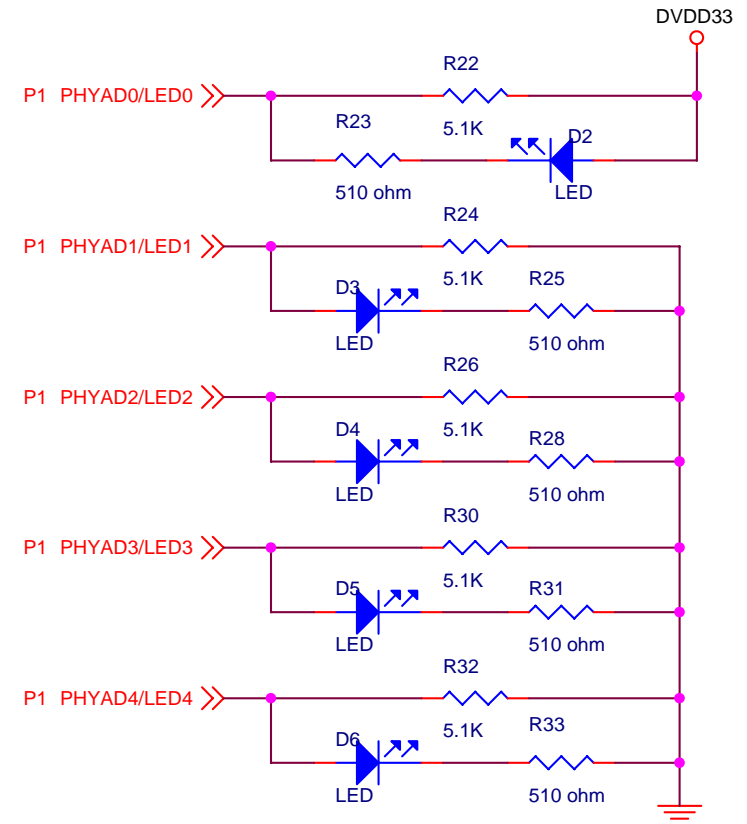
CLOCK generate by IP101A



There could be more than 2 output REFCLK(50MHz) when using buffer 74LV244.

LED and PHY address Configuration

This schematic sets PHY address to 00001b.



LED0	LED1	LED2	LED3	LED4
Link	Dupx	10Act	100Act	COL

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Title

IP101A Chip Circuit Diagram

Size
A

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