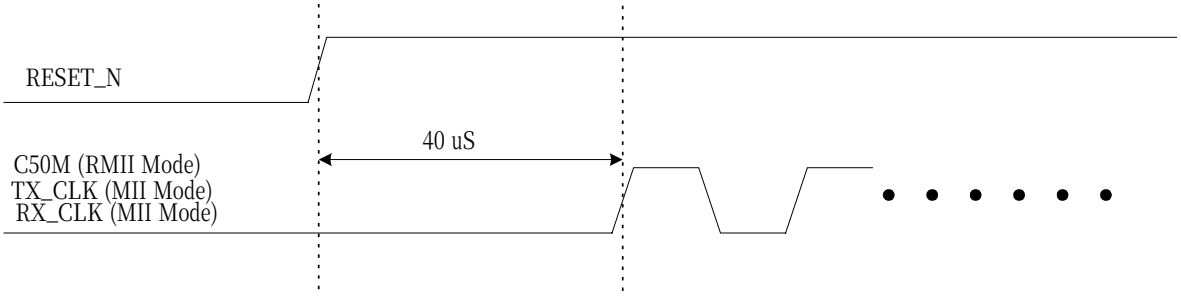
IP101/IP101A Application Note

Relationship between the reset & the clock output

The output delay time of the clock output is around 40us. This time period is measured from the rising edge of reset to the first rising edge of output clock.

The designer should pay attention to this limitation to avoid the improper operation. If the system requires a clock less than 40us delay, the designer can drive the reset of IP101A/IP101 earlier than other devices or use a separate clock source.



Relationship between the reset & the PHY register

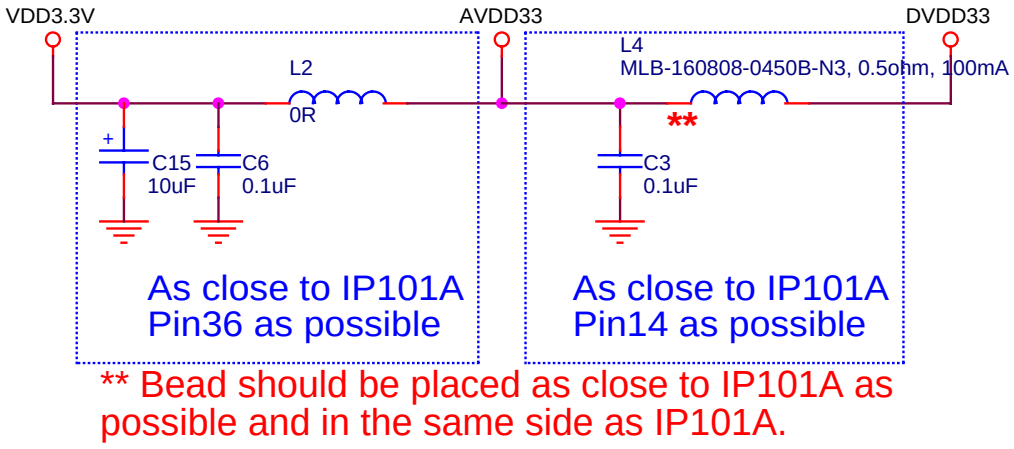
There is a delay time, around 2.5 ms, between the rising edge of the reset and the active state of the internal register. IP101A/IP101 registers keep inactive until the delay time expires.

Transformer

To support MDI/MDIX, the designer should use the transformer with center tap pin.

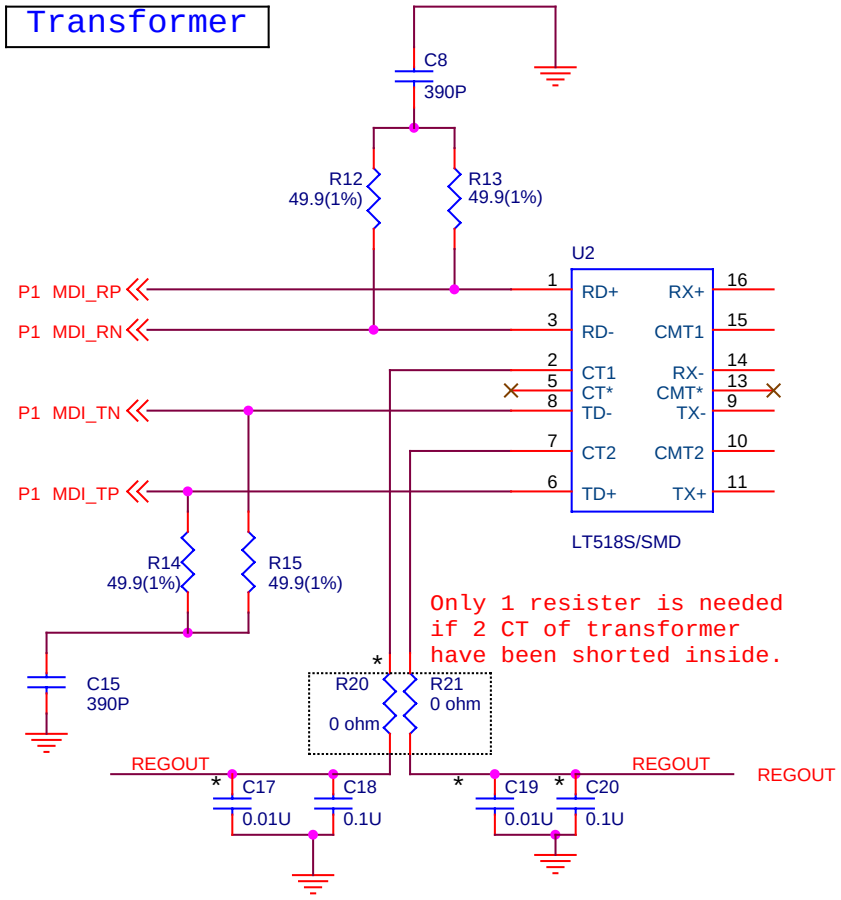
EMI Suppression

(1) There should be a ferrite bead between DVDD and AVDD to reduce the high frequency noise between these two power sources. Since the ferrite bead is used in the power path, the spec, as shown in the figure, should be different from that used in signal path.

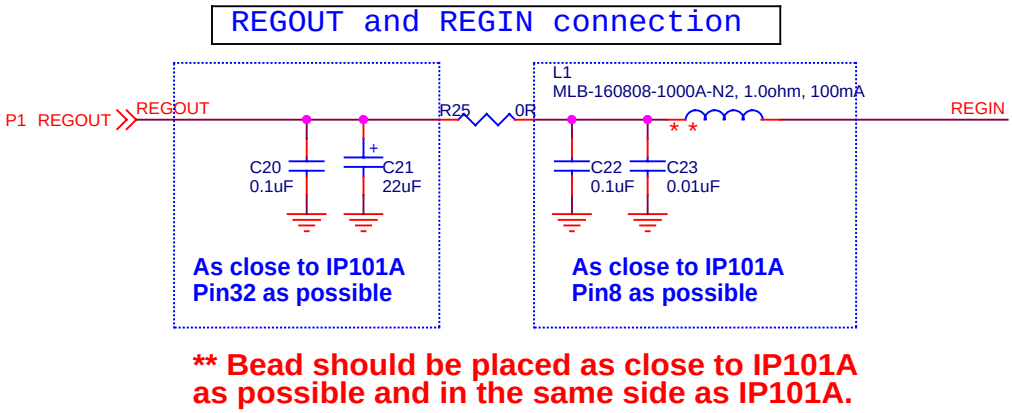


** Bead should be placed as close to IP101A as possible and in the same side as IP101A.

(2) The capacitors C8, C15, C17, C18, C19, C20 help suppress the EMI. In normal case, designers do not need to change these capacitors to pass EMI test. Even so, it's possible the designer have to change the value of capacitors according to the EMI condition.



(3) The ferrite bead and capacitors placed between RegOut and RegIn form a filter array. With these components, the system EMI effect will be greatly suppressed. The decoupling capacitors CB1, CB2, C16 also help reduce the EMI caused by DVDD and should be close to IP101A/IP101.



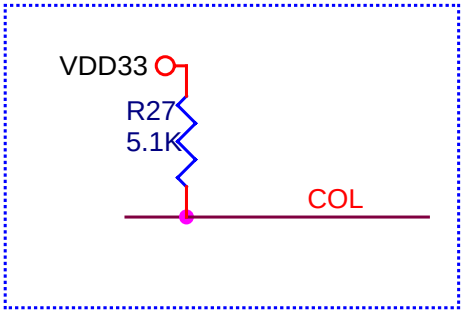
- **LED function**

	IP101/101A (LED mode1, default)	RTL8201BL	RTL8201CL/CP (Pin 1 pulled high)	RTL8201CL/CP (Pin 1 Not pulled high)
Pin 9 (Link)	Light on when link			Light on when link
Pin 10 (Duplex)	Light on when full duplex operation			Light on when full duplex operation
Pin 12 (10M)	Light on when link in 10M mode; Blinking when 10M Tx/Rx occur			Blinking when 10M Tx/Rx occur
Pin 13 (100M)	Light on when link in 100M mode; Blinking when 100M Tx/Rx occur			Blinking when 100M Tx/Rx occur
Pin 15 (Col)	Blinking when collision occur			Blinking when collision occur

- **The MII/RMII mode selection**

IP101 : In MII mode ,R27(NC)
In Test mode ,R27(5.1K ohm)

IP101A : In MII mode, R27(NC)
In RMII mode, R27(5.1K ohm)



R27 is reserved for 8201CL/CP LED Mode Change to compatible with 8201BL

RTL8201BL : R27(NC)
RTL8201CL/CP : R27(5.1K ohm)

Change MDI signals by manual operation

Following steps to change MDI signals by manual operation:
(1) Set high to bit 11 of Register 16 to disable the automatic switch of MDI and MDI-X modes.
(2) Disable APS mode: Set low to bit 1 of Register 16, and pull Pin41 “APS” down.
(3) When auto-crossover is disabled, the bit 3 of Register 30 is used to select MDI or MDIX channel.

Bit	Name	Description/Usage	Default value (h): 0002
Register 30: PHY Spec. Control Registers			
3	FORCE_MDIX	Set high to force the MDIX channel to be selected. 1: Force the MDIX channel to be selected. 0: MDI channel is selected when auto-MDIX is turned off. When IP101A LF operates in Force 10Mb mode or APS mode, this bit is not able to write.	0, RW

Connecting to INT5500CS

There may be a design issue between IP101A & INT5500CS. When this symptom occurs, INT5500CS cannot communicate with IP101A. The cause of this symptom is listed as following.

Cause:
(1) Upon reset, INT5500Cs starts scanning the PHY device by polling the PHY register. The sequence of scanned PHY ID is 0, 1, ….., 31, and then 0, 0, 0, ……
(2) As mentioned above, the PHY register will not be ready until the delay time 2.5ms expires. Its most likely INT5500Cs cannot find IP101A at the first run of scan (PHY ID ranging from 0 to 31), and then confirm the existence of IP101A during the 0,0….. scanning sequence.

Solution:
(1) Set the PHY ID of IP101A to address “0”, so that IP101A can be recognized by INT5500CS during 0,0,0,….scanning process.
(2) Drive the reset of IP101A 2.5ms earlier than that of INT5500CS. This approach allows the designer to set IP101A to any PHY ID other than “0”.