AN 18.20

Migrating from the LAN8700 to the LAN8710/LAN8720

1 Objective

SMSC is pleased to announce its latest industry leading solution for the 10/100 Ethernet transceiver market. This application note is intended for customers who are currently using our LAN8700 solution and who are creating new designs using the LAN8710/LAN8720 transceiver. This next generation transceiver provides improved power savings, PCB area savings, and enhanced performance features.

1.1 References

- LAN8700 Datasheet
- LAN8710 Datasheet
- LAN8720 Datasheet
- Reference Design for the LAN8700
- Reference Design for the LAN8710
- Reference Design for the LAN8720

1.2 Overview of Changes Required

Table 1.1 summarizes the changes needed to migrate from the LAN8700 to the LAN8710/LAN8720.

Table 1.1 Summary of Changes Required

CHANGE REQUIRED	COMMENTS	REFERENCES
RMII select strap option moved to RXD2 (RXD2/RMIISEL)	Applicable only on LAN8710. LAN8720 RMII only device.	LAN8710 datasheet LAN8720 datasheet Section 2.1, "Selecting RMII Mode Operation"
MODE2 strap option moved to COL/CRS_DV (COL/CRS_DV/MODE2)	LAN8720 signal name CRS_DV/MODE2	LAN8710 datasheet LAN8720 datasheet Section 2.2, "MODE Configuration Pins"
PHYAD2 strap option on RXD3 (RXD3/PHYAD2)	Signal available on LAN8710 only.	LAN8710 datasheet LAN8720 datasheet Section 2.3, "PHY Address Strapping"
nINTSEL strap option moved to LED2 (LED2/nINTSEL)	Also selects REFCLK out operation on LAN8720	LAN8710 datasheet LAN8720 datasheet Section 2.6, "LED Functionality and Polarity Configuration" Section 2.4, "50MHz REFCLK Out to MAC"
PHYAD0 strap option moved to RXER (RXER/RXD4/PHYAD0)	LAN8720 signal name RXER/PHYAD0	LAN8710 datasheet LAN8A20 datasheet Section 2.3, "PHY Address Strapping"

Table 1.1 Summary of Changes Required (continued)

CHANGE REQUIRED	COMMENTS	REFERENCES
PHYAD1 strap option moved to RXCLK (RXCLK/PHYAD1)	Signal available on LAN8710 only.	LAN8710 datasheet LAN8720 datasheet Section 2.3, "PHY Address Strapping"
REGOFF strap option moved to LED1 (LED1/REGOFF)		LAN8710 datasheet LAN8720 datasheet Section 2.6, "LED Functionality and Polarity Configuration" Section 2.5, "1.2V Regulator"
PHY address pins now strap to logic ‘0’ when floated.		LAN8710 datasheet LAN8720 dataSheet Section 2.3, "PHY Address Strapping"
VDDCR now 1.2V	1.2V must be supplied via external regulator when internal regulator is disabled (LED1/REGOFF pulled high)	LAN8710 datasheet LAN8720 datasheet Section 2.5, "1.2V Regulator"
RBIAS (signal called EXRES1 on LAN8700) now requires 12.1K 1% resistor to ground.		LAN8710 datasheet LAN8720 datasheet Section 2.7, "RBIAS Resistor"
1uF external capacitor required on VDDCR.	LAN8700 required 01.uF and 4.7uF external capacitors.	LAN8710 datasheet LAN8720 datasheet Section 2.8, "External VDDCR Capacitors"

2 Hardware Changes

2.1 Selecting RMII Mode Operation

Although the LAN8710 can be configured for either MII or RMII operation, the LAN8720 (RMII only) is recommended for RMII applications. The LAN8720 is available in a low cost 24QFN package, and provides a 50MHz clock out option to drive the MAC. This reduces BOM cost by requiring a low cost 25MHz crystal rather than a higher priced clock oscillator.

2.1.1 RMII Mode Configuration for the LAN8710

To select RMII mode operation on the LAN8710, the RXD2/RMIISEL pin must be pulled high externally by a 10K resistor as shown in Figure 2.1. This signal must be sampled as a logic ‘1’ on a power up or on the rising edge of nRESET.

RMIISEL was previously on the COL/RMII/CRS_DV signal of the LAN8700.

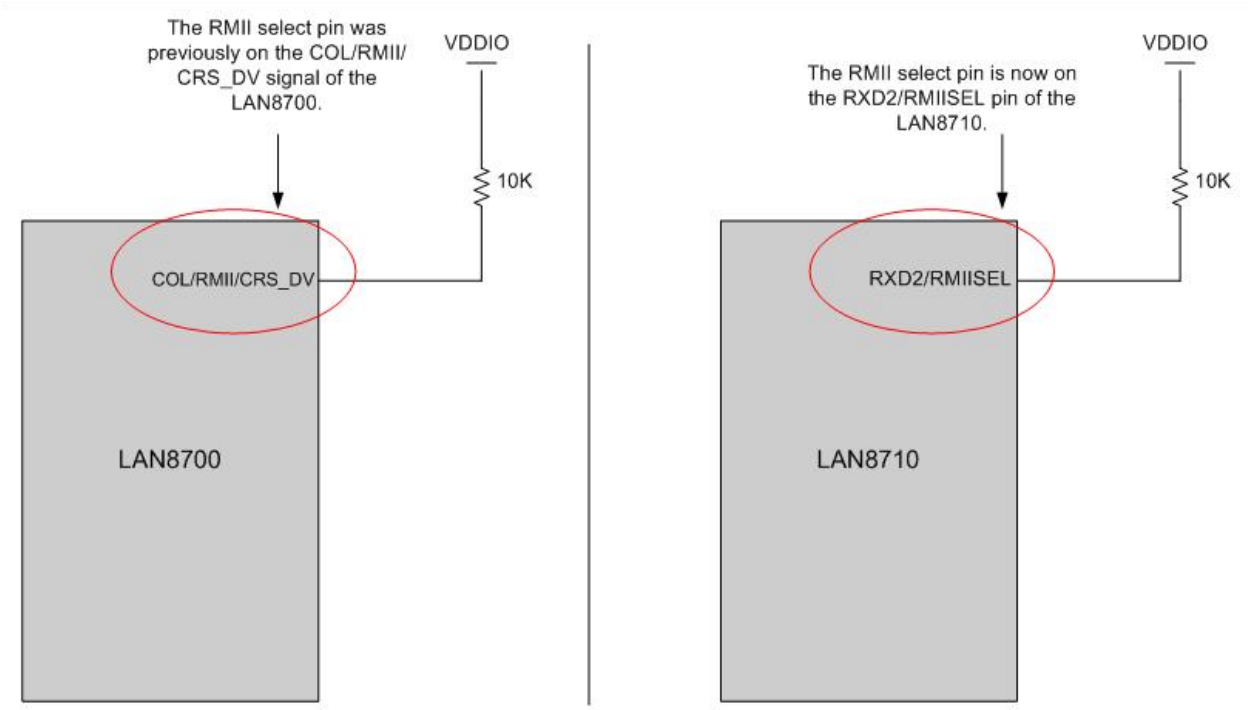

Figure 2.1 LAN8710 Configured for RMII Operation

2.1.2 RMII Mode Configuration for the LAN8720

The LAN8720 is by default configured for RMII operation, and requires no external strap resistors.

2.2 MODE Configuration Pins

The MODE[2] strap configuration pin on the LAN8710/LAN8720 has been moved to the COL/CRS_DV/MODE2 pin (signal name is CRS_DV/MODE2 on the LAN8720). The new MODE bit signals are shown below in Table 2.1.

MODE[2] was previously on the RXD2/MODE2 signal of the LAN8700.

Table 2.1 LAN8710/LAN8720 MODE Bits

MODE BIT	LAN8700 PIN NAME	LAN8710/8720 PIN NAME
MODE[0]	RXD0/MODE0	RXD0/MODE0
MODE[1]	RXD1/MODE1	RXD1/MODE1
MODE[2]	RXD2/MODE2	COL/CRS_DV/MODE2

2.3 PHY Address Strapping

2.3.1 LAN8710 PHY Address Strapping

PHYAD[2:0] is now multiplexed on RXER/PHYAD0, RXCLK/PHYAD1, and RXD3/PHYAD2 respectively. The LAN8710 does not have a 4th PHY address bit.

The PHYAD[2:0] pins have internal pull-down resistors, and can be floated for address bit values of logic ‘0’. The PHYAD[2:0] pins can be pulled high externally for address values of logic ‘1’.

Table 2.2 LAN8710 PHY Address Bits

PHY ADDRESS BIT	LAN8700 PIN NAME	LAN8710 PIN NAME
PHYAD[0]	SPEED100/PHYAD0	RXER/PHYAD0
PHYAD[1]	LINK/PHYAD1	RXCLK/PHYAD1
PHYAD[2]	ACTIVITY/PHYAD3	RXD3/PHYAD2
PHYAD[3]	CRS/PHYAD4	-

2.3.2 LAN8720 PHY Address Strapping

The LAN8720 PHY address may be configured via PHYAD[0], which is now multiplexed on RXER/PHYAD0.

The PHYAD[0] pin has an internal pull-down resistor, and can be floated for an address bit value of logic ‘0’, or pulled high externally for an address value of logic ‘1’.

The user can configure the PHY address using a software configuration if an address greater than 1 is required. The PHY address can be written (after SMI communication at some address is established) using the 10/100 Special Modes register (Reg 18[4:0]).

Table 2.3 LAN8720 PHY Address Bits

PHY ADDRESS BIT	LAN8700 PIN NAME	LAN8710 PIN NAME
PHYAD[0]	SPEED100/PHYAD0	RXER/PHYAD0
PHYAD[1]	LINK/PHYAD1	-
PHYAD[2]	ACTIVITY/PHYAD3	-
PHYAD[3]	CRS/PHYAD4	-

2.4 50MHz REFCLK Out to MAC

The LAN8720 introduces an enhanced feature that allows the 50MHz RMII reference clock (REFCLKO) to be generated by the LAN8720, while only requiring a low cost 25MHz crystal connected to the LAN8720. REFCLKO is multiplexed with the nINT pin (nINT/REFCLKO), and is selected by pulling the LED2/nINTSEL pin low. This allows a logic '0' to be sampled either on a power up or on the rising edge of nRESET, and enables the 50MHz REFCLKO signal on the nINT/REFCLKO pin.

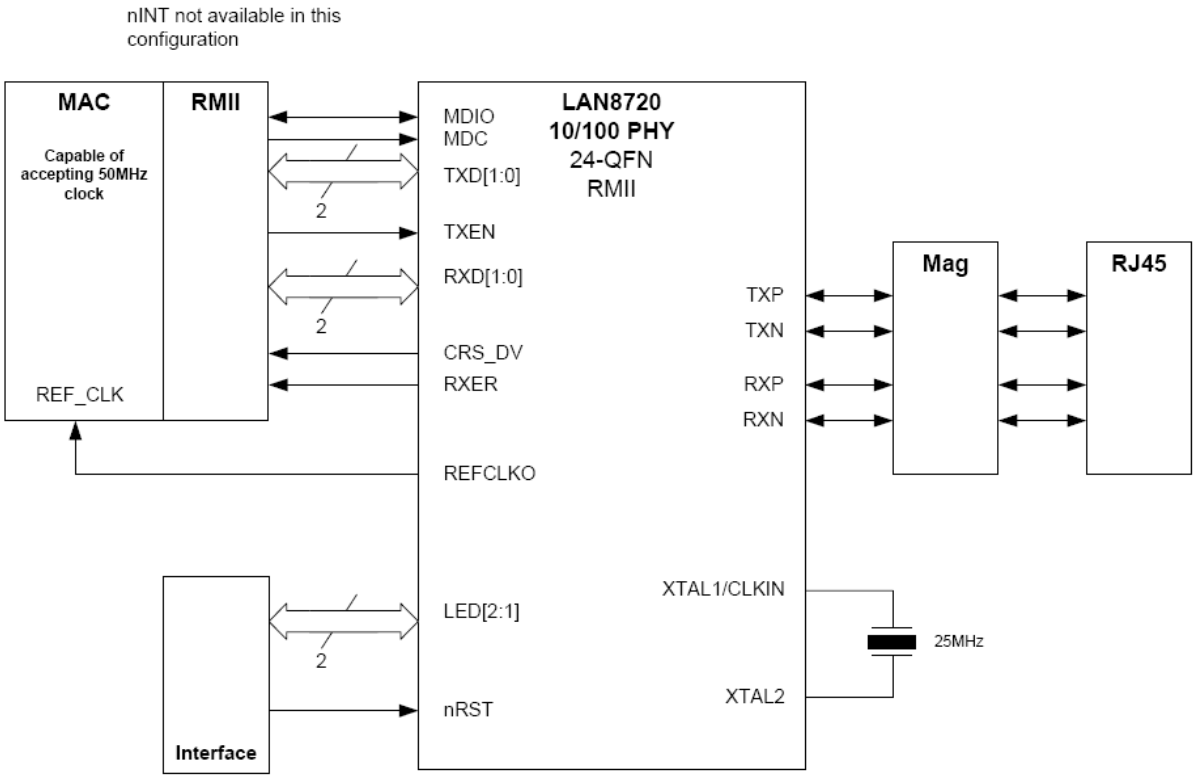

Figure 2.2 50MHz REFCLKO Configuration

When using the LAN8720 to generate the 50MHz RECLKO to drive the MAC, only a 25MHz crystal or clock input to the LAN8720 can be used (cannot be 50MHz).

The LAN8720 can still be driven by a 50MHz clock (for example, when the MAC drives the 50MHz clock to the LAN8720), however the nINT/REFCLKO pin must be configured for nINT operation by either floating or pulling up (with external pull-up resistor) the LED2/nINTSEL signal.

The 50MHz REFCLKO option is only available on the LAN8720.

2.5 1.2V Regulator

In order to improve power consumption the LAN8710/LAN8720 uses a 1.2V VDDCR voltage. The VDDCR voltage on the LAN8700 was 1.8V, so designs that utilize an external voltage regulator for VDDCR now require that the external supply be 1.2V. The external stability and decoupling capacitors that were previously required on the LAN8700 has been reduced on the LAN8710/LAN8720. The LAN8710/LAN8720 now requires only a 1uF decoupling capacitor on the VDDCR pin, reducing the total system BOM cost.

2.5.1 Disabling the Internal 1.2V Regulator

The internal 1.2V regulator of the LAN8710/LAN8720 can be disabled to allow for the use of an external 1.2V regulator. To disable the internal 1.2V regulator, an external pull-up resistor must be added to LED1/REGOFF to select a logic '1' when this pin is sampled during power up. for additional information on LED polarity, see Section 2.6, "LED Functionality and Polarity Configuration". When the internal 1.2V regulator is disabled, an external 1.2V regulator must be input on the VDDCR pin of the LAN8710/LAN8720. When an external 1.2V regulator is used with the LAN8710/LAN8720, decoupling and/or stability capacitors may be required on the VDDCR pin of the LAN8710/LAN8720.

2.6 LED Functionality and Polarity Configuration

2.6.1 LED Functionality

The LAN8710/LAN8720 has combined 3 LED functions from the LAN8700 into 2 LEDs on the LAN8710/LAN8720, as shown below in Figure 2.3.

LED1 will be active when the LAN8710/LAN8720 has a valid LINK (in either 10BT or 100BT), and will blink when there is activity present.

LED2 will be active when the LAN8710/LAN8720 has a valid LINK in 100BT. LED2 will be inactive when no link is present, or when a 10BT link exists.

LED1 and LED2 of the LAN8710/LAN8720 are now in the VDD2A domain. When either LED1 or LED2 are configured as active low, the LED should be connected to VDD2A. For more information, see Section 2.6.2, "LED Polarity Configuration".

Previously on the LAN8700, the LED signals were part of the VDDIO domain as shown below in Figure 2.3.

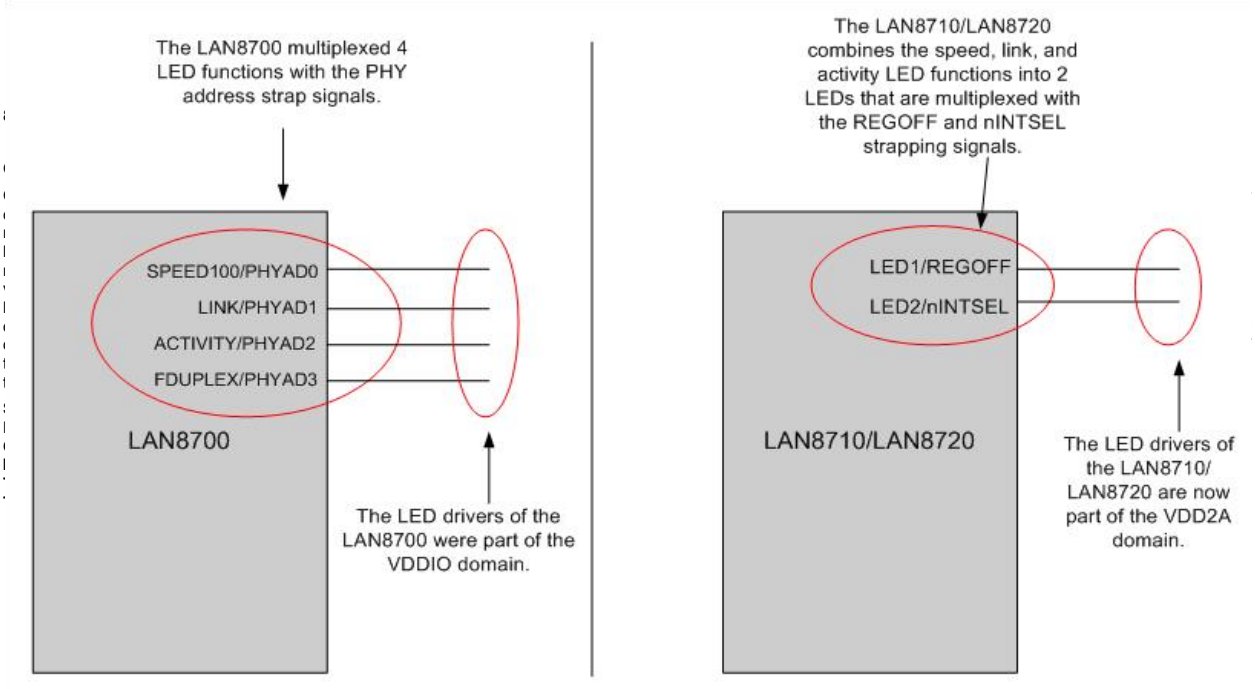

Figure 2.3 LED Functionality

2.6.2 LED Polarity Configuration

The polarity of the two LED output signals of the LAN8720 will be set based on the presence of a pull-up or pull-down resistor. Since LED1 has an internal pull-down resistor, the polarity will be active high by default (when the LED1 pin is floated or pulled down externally). Since LED2 has an internal pull-up resistor, the polarity will be active high by default (when the LED2 pin is floated, or pulled up externally). This must be considered when configuring LED1 and LED2.

2.6.2.1 LED1/REGOFF Polarity Configuration

The REGOFF configuration pin is shared with the LED1 pin. If LED1/REGOFF is pulled low (by the internal pull-down resistor, or by an external pull down resistor) to select a logic '0' for LED1/REGOFF, then the output of LED1 will be active high. If LED1/REGOFF is pulled high to VDD2A through an external pull-up resistor to select a logic '1' for LED1/REGOFF, then the output of LED1 will be active low. Figure 2.4 below shows the hardware configuration for the two LED1/REGOFF configuration options.

If LED1/REGOFF is pulled high, an external 1.2V regulator must be supplied to the VDDCR pin of the LAN8710/LAN8720. See Section 2.5.1, "Disabling the Internal 1.2V Regulator" for more information on disabling the internal 1.2V regulator.

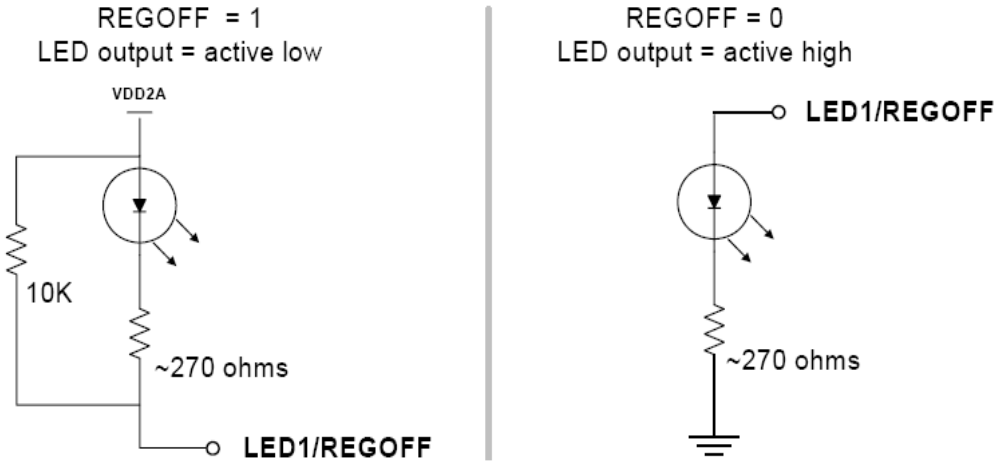

Figure 2.4 LED1 Polarity Configuration

2.6.2.2 LED2/nINTSEL Polarity Configuration

The nINTSEL configuration pin is shared with the LED2 pin. If LED2/nINTSEL is pulled high to VDD2A (through the internal pull-up resistor) to select a logic '1' for LED2/nINTSEL, then the output of LED2/nINTSEL will be active low. If LED2/nINTSEL is pulled low through an external pull-down resistor to select a logic '0' for LED2/nINTSEL, then the output of LED2 will be active high. Figure 2.5 below shows the hardware configuration for the two LED2/nINTSEL configuration options.

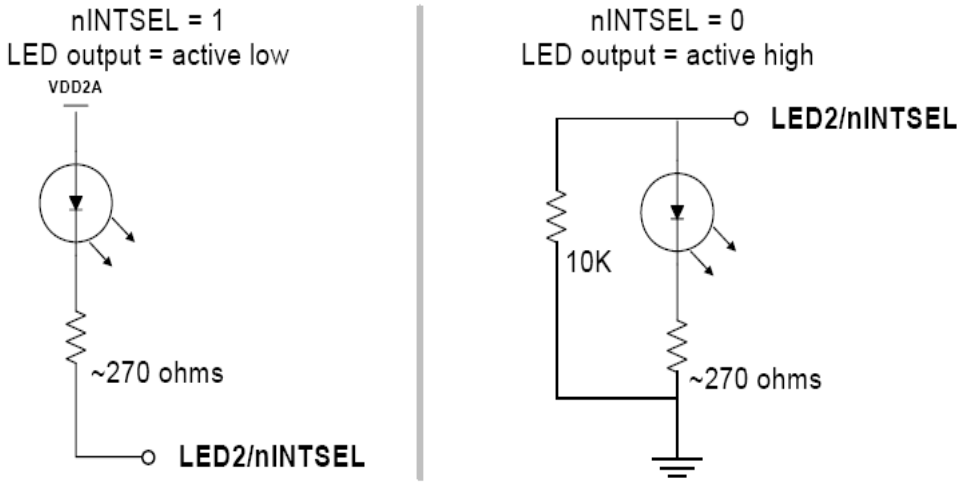

Figure 2.5 LED2 Polarity Configuration

2.7 RBIAS Resistor

A 12.1K 1% resistor is required from the RBIAS pin to ground on the LAN8710/LAN8720 as shown below in Figure 2.6. This signal was called EXRES1 previously on the LAN8700, and had a value of 12.4K 1%.

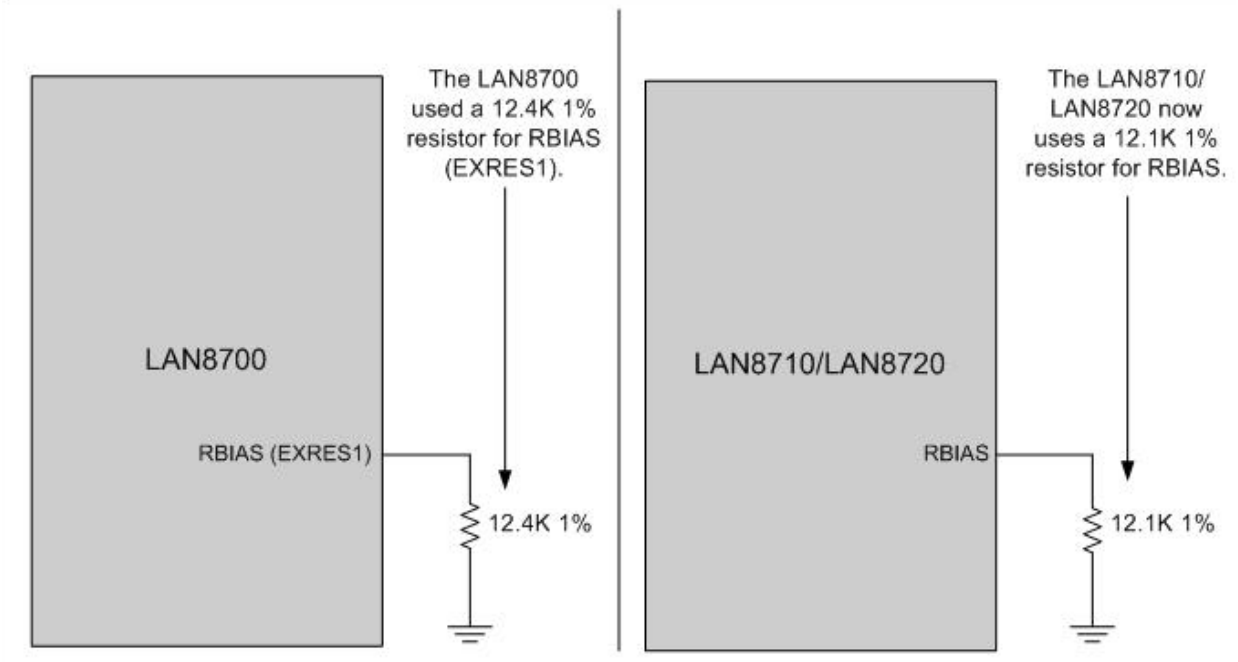

Figure 2.6 RBIAS

2.8 External VDDCR Capacitors

When using the on-chip 1.8V regulator of the LAN8700, external 4.7uF and 0.1uF capacitors were required on the VDD_CORE pin. The LAN8710/LAN8720 requires only a 1uF external capacitor when using the on-chip 1.2V regulator, reducing the total system BOM cost.

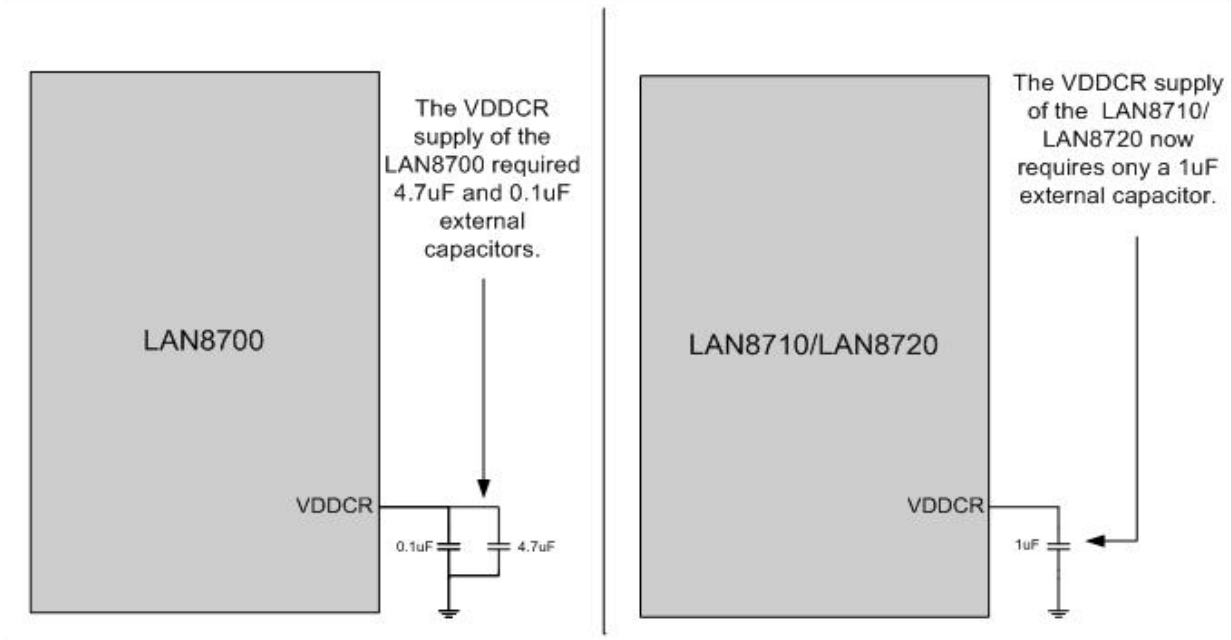

Figure 2.7 External VDDCR Capacitors

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