NV2A GPU

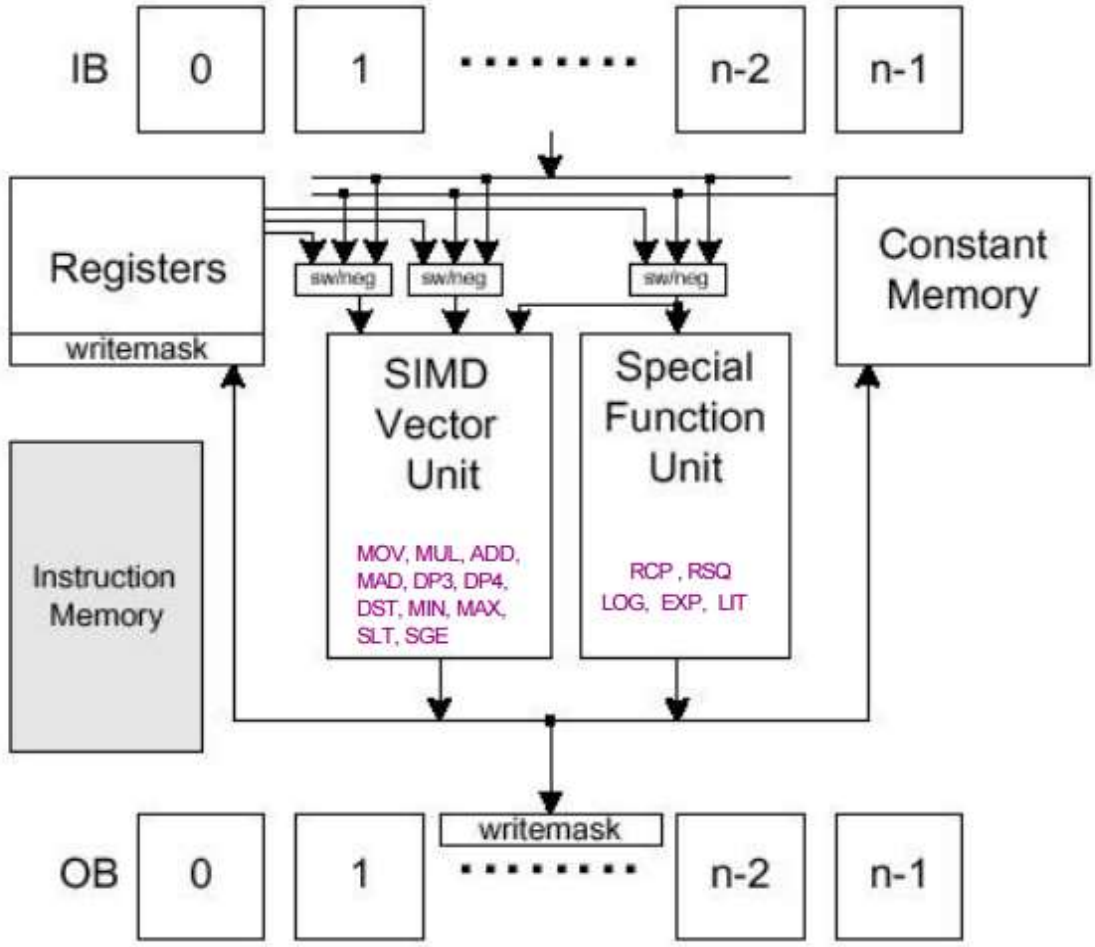

Figure 1 Vertex Program Flow

PCI Id	GPU	Vertex Programs	Pixel Pipelines and ROPs	Texture Units	Date	Notes
02a0*	NV2A	2	4	8	15.11.2001	the XBOX IGP [XGPU]

NV2A BYTECODE

The GPU in the original Xbox was GeForce 3 NV2A DirectX 8.0 based GPU. NV2A bytecode is used to represent machine instructions for the GPU in a compact format. Each byte code is 128bits long and can contain instructions for either the SIMD Vector unit or the Special Function unit (possibly both).

Dword	Bit Offset (RTL)	Bit Length	Name	Bit Offset (LTR)
0	0	32	Note: This is branching/loop code bits. How they work is unknown[1]	0
1	0	7	ScalarOpCode[2]	25
1	7	4	VectorOpCode[3]	21
1	11	8	ConstantSource[4]	13
1	19	4	AttributeSource[5]	9
1	23	9	Param0 (MS bits)[6]	0
2	0	6	Param0 (LS bits)	26
2	6	15	Param1[7]	11
2	21	11	Param2 (MS bits)[8]	0
3	0	4	Param2 (LS bits)	28
3	4	4	Temporary Destination Write-mask[9]	24
3	8	4	Temporary Destination[10]	20
3	12	4	ScalarOp Write-mask[11]	16
3	16	4	VectorOP Write-mask[12]	12
3	20	1	Temporary Destination Bit[13]	11
3	21	8	Destination[14]	3
3	29	1	[15]	2
3	30	1	IndexConstant[16]	1
3	31	1	Last Instruction Bit[17]	0

[1] More research needed.
[2] Operation to be performed by the scalar (special function) unit
[3] Operation to be performed by the vector (SIMD) unit
[4] Index of constant register used by constant type params
[5] Index of attribute register used by attribute type params
[6] 0th Parameter (Generally used by SIMD instructions)
[7] 1st Parameter (Generally used by SIMD instructions)
[8] 2nd Parameter (Generally used by special function unit)
[9] Write-mask to enable or disable writing to components of the destination register
[10] Controls referencing of destination registers (unknown)
[11] Write-mask to enable or disable writing to components of the special function unit destination register
[12] Write-mask to enable or disable writing to components of the SIMD unit destination register
[13] Enables writing to temporary destination (this might be incorrect)
[14] Destination Register enum value
[15] Unknown bit
[16] Enables the use of the a0 Index constant register (unknown)
[17] Marks this instruction as the last instruction of the stream