Date Released: Thursday, February 15, 2024

Due Date: Monday, February 19, 2024 12:00

Assignment - I

Read the Instructions Carefully

Design:

Consider a CPU with a 32 bit address bus and an 16-bit data bus.

How do you interface 8 memory chips (4K x 8 bit) with it?

The design should eliminate all memory-folding issues.

NB:

1. Use an A4 sheet for the assignment.
2. Submit the assignment to Room 321, Caesar Building on Monday, February 19, 2024, no later than 12 noon.