Report

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We decided to optimize the pipeline with data forwarding because it was an easier option for us. For the data forwarding, we did encounter problems with the fmedian2 in our first approach using the original code from Project 3 which had some duplicate logic for checking the Rs register for instruction that only depends on Rs and instructions dependent on both Rt and Rs registers. We passed the test file but not the fmedian2. We also wrote our own assembly file to check for data forwarding, and all the instructions worked but not for fmedian2. We thought we must be missing an edge case since we were duplicating a lot of the data forwarding logic and checking the Rs and Rt registers for data dependency. We solve this problem by simplifying our code for checking data dependency. Instead of checking Rs registers multiple times for the two types of instruction, we change to check the wr_reg_MEM_w and wr_reg_EX_w wires for whether the stages were writing and check the data dependency of the Rs and Rt registers with the write register numbers of the EX and MEM stages. If the instruction is ALUR, SW, or branch, we check for data dependency on both the Rs and Rt register. If the instruction is ALUI, LW or jump, we check for Rs register dependency. For LW during data dependency, we stall the pipeline one cycle because LW's data is ready during the MEM stage.

We also attempted to do branching optimization with branch not taken. We don't think we were successful.

The percentage of work my partner Chidambaram did for this project is 50% for board checking and helping to debug the data forwarding logic and trying out branch not taken. I did around 50% with the data forwarding logic.

Our optimization of clock frequency was 100MHZ.

With no optimization, the Project 3's old time is 67 seconds. Adding clock optimization at 100MHZ with 50MHZ reference clock cycle, Project 3's time is 33 seconds. With just the data forwarding with no clock optimization, the time is 53.2 seconds. With both the data forwarding and clock optimization at 100MHZ with 50MHZ reference clock, the timing for fmedian2 is 26.7 seconds.