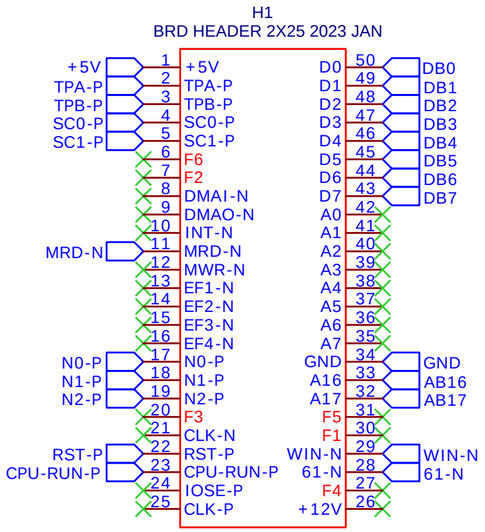
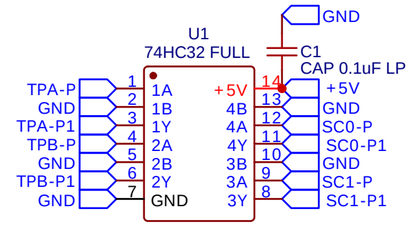
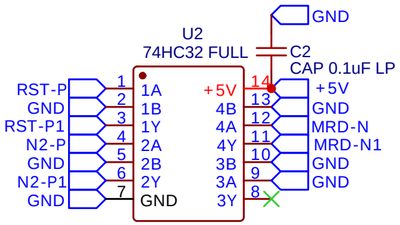
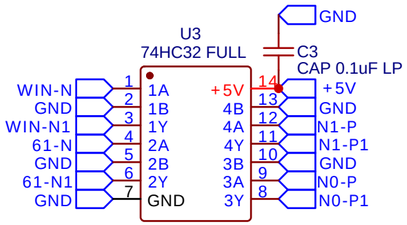
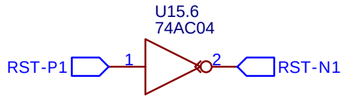


LOGIC BUFFERS

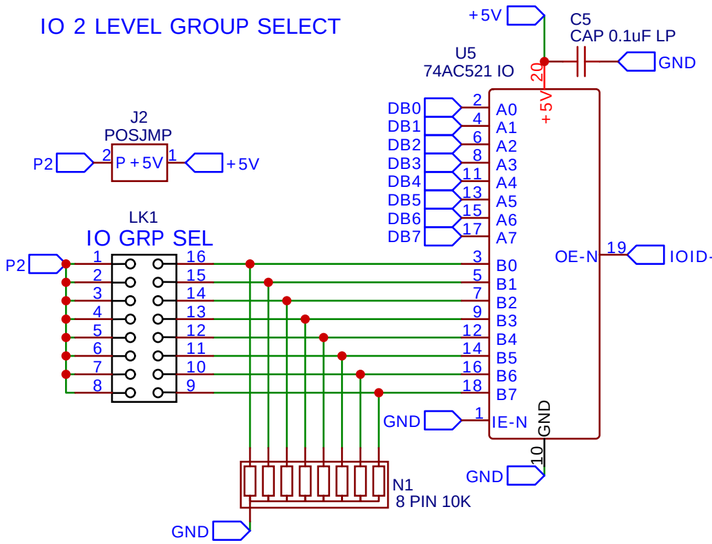




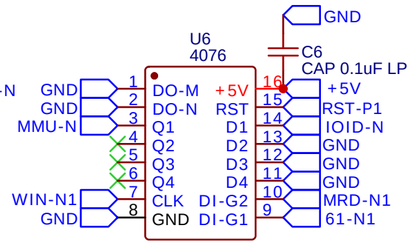




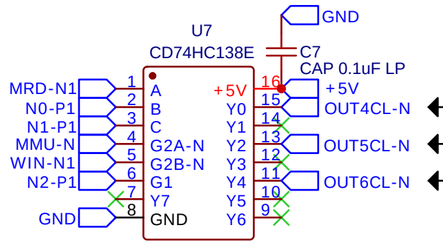
IO 2 LEVEL GROUP SELECT

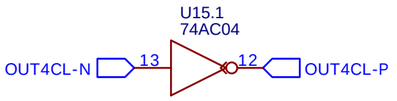


BANK IO ENABLE LATCH



IO COMMAND DECODE





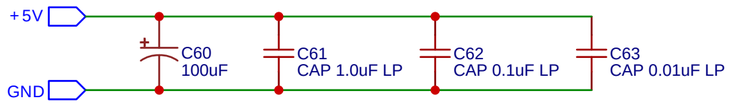
IO INSTRUCTIONS

OUT P4 (64)
SET REGISTER PAGE
OUTPUT BYTE CONSISTS OF
HIGH NIBBLE: REGISTER 0-F
LOW NIBBLE: PAGE 0-3

OUT P5 (65)
ENABLE MMU
OUTPUT BYTE NOT APPLICABLE

OUT P6 (66)
DISABLE MMU
OUTPUT BYTE NOT APPLICABLE

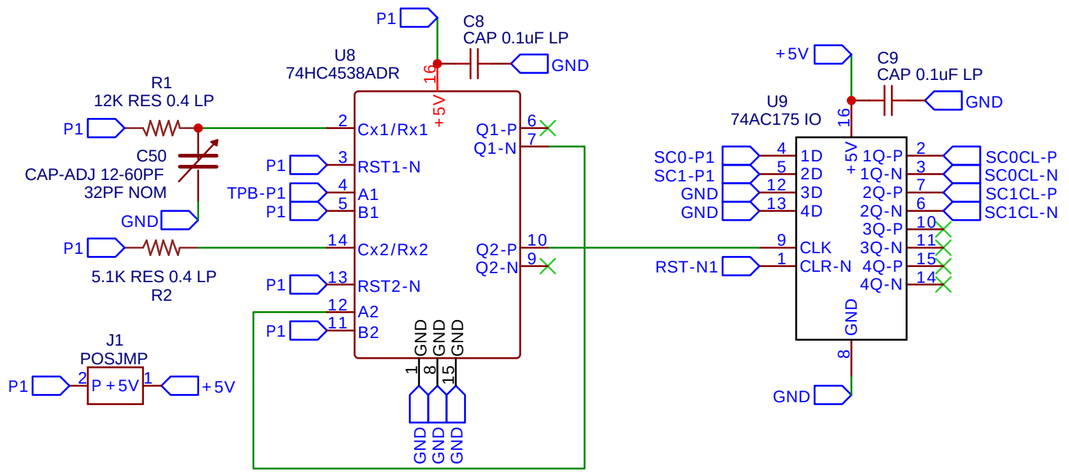
DO NOT LEAVE BOARD IO ENABLED BEYOND NEED TO EFFECT MMU



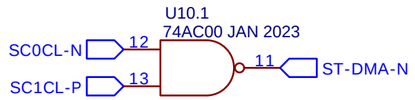
TITLE: INTERFACE		REV: 1.0
嘉立创EDA	Company: Your Company	Sheet: 1/4
	Date: 2023-02-24 Drawn By: jeff.truck	

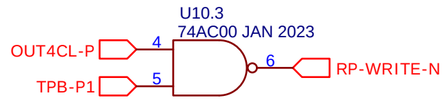
CURRENT STATE LATCH

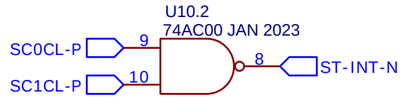
TRIGGER LATCH 535nS
AFTER TPB RISING EDGE
NOTE: R1,R2,C50,C51
CHOSEN FOR 4MHz CPU CLOCK

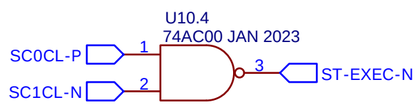


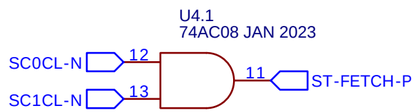
CURRENT STATES / REGISTER PAGE WRITE

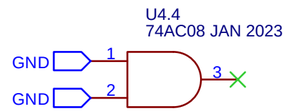


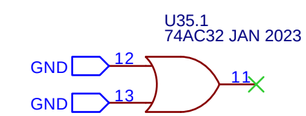


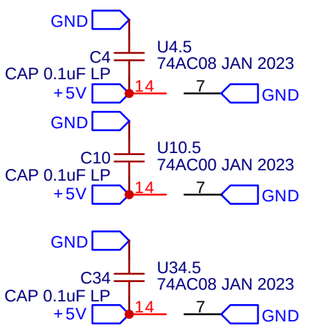




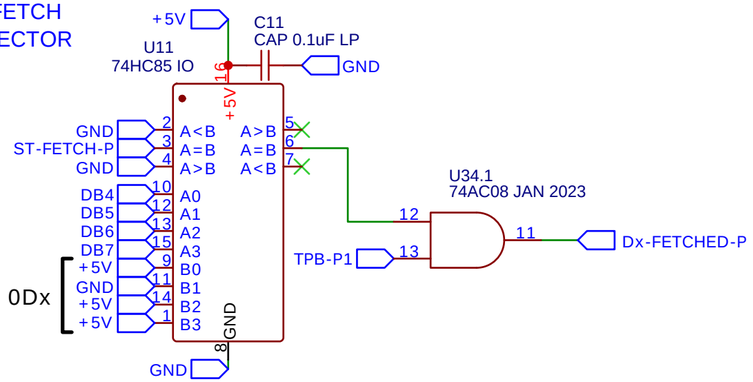




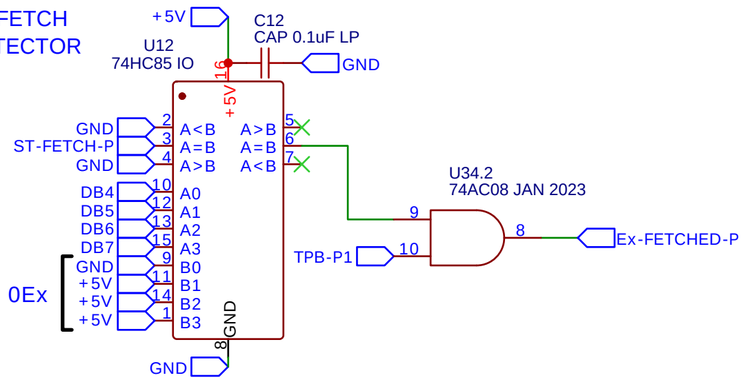




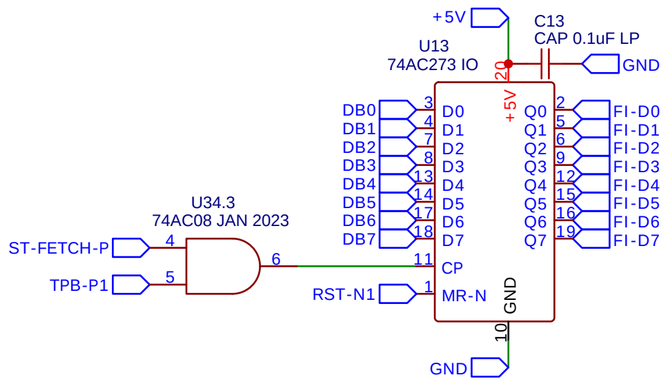
Dx FETCH DETECTOR



Ex FETCH DETECTOR



FETCHED INSTRUCTION



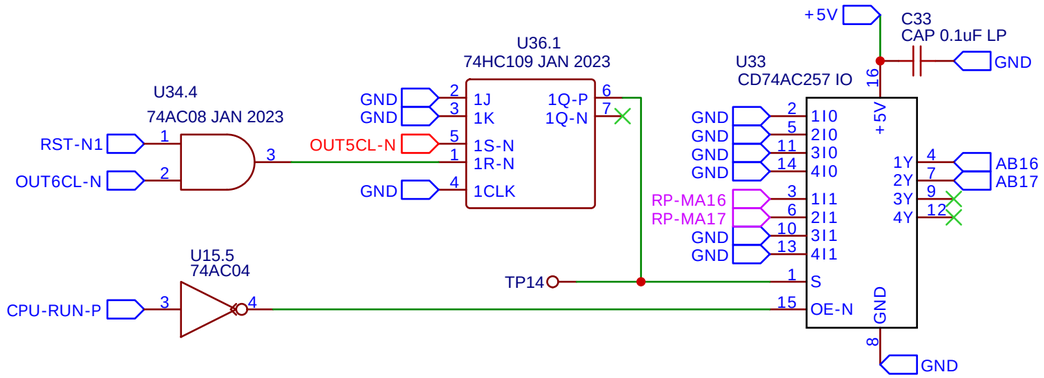
TITLE: CURRENT STATES	REV: 1.0
Company: Your Company	Sheet: 2/4
Date: 2023-02-24 Drawn By: jeff.truck	

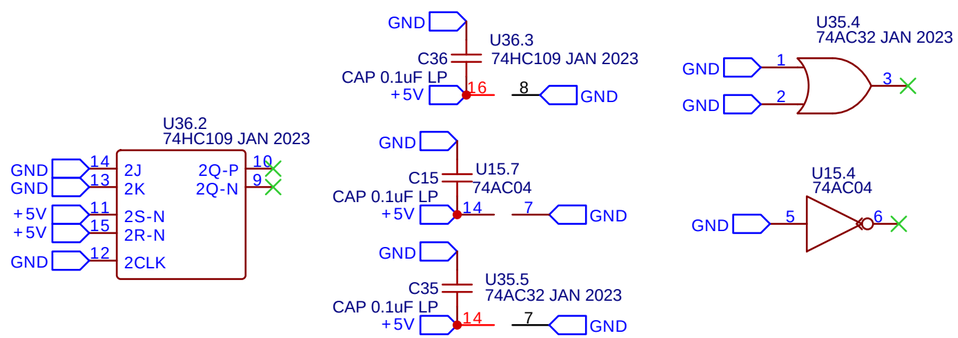
ST-FETCH-P
U15.2 74AC04
U35.3 74AC32 JAN 2023
U15.3 74AC04
6nS
6nS
6nS
'P' REGISTER
U18 74HC173 IO
C18 CAP 0.1uF LP
Dx-FETCHED-P
NEW P
17nS
REGISTER PAGES
U20 CY7C199-35PC
35nS
C20 CAP 0.1uF LP
RP-WRITE-N
OUT4CL-P
D2-D7 NOT USED
R_NET_8_22K RN2
C24 CAP 0.1uF LP
U24 AT28C16 IO
EXECUTE MICROCODE
RN1 R_NET_8_10K
FI-D0
FI-D1
FI-D2
FI-D3
FI-D4
FI-D5
FI-D6
FI-D7
ST-EXEC-N
OUT4CL-P
IO7 NOT USED
'X' REGISTER
U19 74HC173 IO
C19 CAP 0.1uF LP
Ex-FETCHED-P
NEW X
TP3
TP4
TP5
TP6
TP7
TP8
PAGE LATCH
U21 74AC175 IO
C21 CAP 0.1uF LP
12nS
RST-N1
RP-MA16
RP-MA17
TP1
TP2
REGISTER SETTING IO
U22 74HC245
C22 CAP 0.1uF LP
OUT4CL-N
PAGE NUMBER REGISTER
DMA REGISTER
U17 74AC125 IO
C17 CAP 0.1uF LP
ST-DMA-N
00x
'N' REGISTER
U23 74AC125 IO
C23 CAP 0.1uF LP
INT REGISTER
U16 74AC125 IO
C16 CAP 0.1uF LP
ST-INT-N
01x
R3 12K RES 0.4 LP
C52 CAP-ADJ 12-60PF 32PF NOM
R4 5.1K RES 0.4 LP
U14 74HC4538ADR
C14 CAP 0.1uF LP
TPA-P1
J3 POSJMP
TRIGGER LATCH 535nS AFTER TPA RISING EDGE
NOTE: R4,R5,C52,C53 CHOSEN FOR 4MHz CPU CLOCK
** DISABLED DURING OUT4

TITLE: BANK SELECT	REV: 1.0
Company: Your Company	Sheet: 3/4
Date: 2023-02-24 Drawn By: jeff.truck	

嘉立创EDA

SYSTEM (ENABLE / DISABLE) OR NANO BANKING





TITLE: MEMORY		REV: 1.0
嘉立创EDA	Company: Your Company	Sheet: 4/4
	Date: 2023-02-24 Drawn By: jeff.truck	