IO CONTROL

H1
BRD HEADER 2X25 2023 JAN

+5V	1	50	DB0
TPA-P	2	49	DB1
TPB-P	3	48	DB2
SC0-P	4	47	DB3
SC1-P	5	46	DB4
F6	6	45	DB5
F2	7	44	DB6
DMAI-N	8	43	DB7
DMAO-N	9	42	A0
INT-N	10	41	A1
MRD-N	11	40	A2
MWR-N	12	39	A3
EF1-N	13	38	A4
EF2-N	14	37	A5
EF3-N	15	36	A6
EF4-N	16	35	A7
N0-P	17	34	GND
N1-P	18	33	A16
N2-P	19	32	A17
F3	20	31	F5
CLK-N	21	30	F1
RST-P	22	29	WIN-N
CPU-RUN-P	23	28	61-N
IOSE-P	24	27	F4
CLK-P	25	26	+12V

Pin labels: +5V, TPA-P, TPB-P, SC0-P, SC1-P, DMAI-N, DMAO-N, INT-N, MRD-N, MWR-N, EF1-N, EF2-N, EF3-N, EF4-N, N0-P, N1-P, N2-P, CLK-N, RST-P, CPU-RUN-P, IOSE-P, CLK-P, RESET-P, WIN-N, 61-N

J1 POSJMP — P1 — P +5V — +5V

U1 74HC85 IO — C1 CAP 0.1uF LP
U2 74HC85 IO — C2 CAP 0.1uF LP
U3 4076 IO — C3 CAP 0.1uF LP
U7.1 74HC04 2023 JAN — BRDSEL-N
U6 74HC138 — C6 CAP 0.1uF LP

U6 pins: A, B, C, G1, /G2A, /G2B, /Y0, /Y1, /Y2, /Y3, /Y4, /Y5, /Y6, /Y7, GND
MRD-N1, N0-P1, N1-P1, N2-P1, WIN-N1, GND — OUT6-N, IN6-N, OUT7-N, IN7-N

U1: A<B, A=B, A>B, A>B, A=B, A<B, A0, A1, A2, A3, B0, B1, B2, B3, GND — P1, GND, DB0, DB1, DB2, DB3
U2: A<B, A=B, A>B, A>B, A=B, A<B, A0, A1, A2, A3, B0, B1, B2, B3 — DB4, DB5, DB6, DB7, GND
U3 4076 IO: DI-G1, DI-G2, D1, D2, D3, D4, CLK, DO-M, DO-N, RST, Q1, Q2, Q3, Q4, GND — MRD-N1, 61-N1, GND, WIN-N1, GND, RESET-P

LK1 IO GRP SEL HDR — P1
Pins: 1–16, 2–15, 3–14, 4–13, 5–12, 6–11, 7–10, 8–9

RN1 R_NET_8_10K — GND

Legend box:
IN6 - UART Data Read
OUT6 - UART Data Write
IN7 - UART Control Read
OUT7 - UART Control Write

U4.1 CD74HC32 JAN 2023 — MRD-N, GND → MRD-N1 (12,13,11)
U4.2 CD74HC32 JAN 2023 — WIN-N, GND → WIN-N1 (9,10,8)
U4.3 CD74HC32 JAN 2023 — 61-N, GND → 61-N1 (4,5,6)
U4.4 CD74HC32 JAN 2023 — N0-P, GND → N0-P1 (1,2,3)
U5.1 CD74HC32 JAN 2023 — N1-P, GND → N1-P1 (12,13,11)
U5.2 CD74HC32 JAN 2023 — N2-P, GND → N2-P1 (9,10,8)
U7.6 74HC04 2023 JAN — RESET-P → RESET-N (1,2)
U5.4 CD74HC32 JAN 2023 — TPB-P, GND → TPB-P1 (1,2,3)

UART DATA BUS CONTROL

U8 74HC245 — C8 CAP 0.1uF LP — GND
Pins: DIR, A1, A2, A3, A4, A5, A6, A7, A8, GND, +5V, OE-N, B1, B2, B3, B4, B5, B6, B7, B8
SM-D7, DB0, DB1, DB2, DB3, DB4, DB5, DB6, DB7, GND — +5V, GND, UART-DB0, UART-DB1, UART-DB2, UART-DB3, UART-DB4, UART-DB5, UART-DB6, UART-DB7

EXTERNAL SIGNAL GATES

L2 EFx Select Link — EF1-N, EF2-N, EF3-N, EF4-N / EF1 EFX, EF2 EFX, EF3 EFX, EF4 EFX
L1 EFx Select Link — EF1-N, EF2-N, EF3-N, EF4-N / EF1 EFX, EF2 EFX, EF3 EFX, EF4 EFX
L3 INT Enable Link — INT-N / INT-N INTX-N
L4 UART EXT ES LINK — A, COM, B, H → +5V, EXT-ES-N
L5 UART EXT PSI LINK — A, COM, B, H → +5V, EXT-PSI-N

U9 74HC245 — C9 CAP 0.1uF LP — GND
Pins: DIR, A1, A2, A3, A4, A5, A6, A7, A8, GND, +5V, OE-N, B1, B2, B3, B4, B5, B6, B7, B8
GND — +5V, BRDSEL-N, UART-DA-N, UART-THRE-N, UART-EXT-INT-N, GND...

J4 POSJMP — P4 — P +5V — +5V
J5 POSJMP — P5 — P +5V — +5V

U7.2 74HC04 2023 JAN — P4 (11,10)
U7.3 74HC04 2023 JAN — P4 (9,8)
U7.4 74HC04 2023 JAN — P4 (5,6)
U7.5 74HC04 2023 JAN — P4 (3,4)
U5.3 CD74HC32 JAN 2023 — P5, P5 (4,5,6)

U7.7 74HC04 2023 JAN — C7 CAP 0.1uF LP — +5V, GND (14,7)
U4.5 CD74HC32 JAN 2023 — C4 CAP 0.1uF LP — +5V, GND (14,7)
U5.5 CD74HC32 JAN 2023 — C5 CAP 0.1uF LP — +5V, GND (14,7)

Power decoupling: +5V / GND
C60 100uF, C61 CAP 1.0uF LP, C62 CAP 0.1uF LP, C63 CAP 0.01uF LP

1.8432 MHz = 115K/57K BAUD RATE CLOCK

X1
ECS-2100X 3.6864MHz

U10.1
74HC109 JAN 2023

U10.2
74HC109 JAN 2023

CAP 0.1uF LP
C50

J2
POSJMP
P2 + 5V

H2
3 PIN GENERAL HDR
P1 — BD-115-CLK
P2 — BD-CLK
P3 — BD-57-CLK

STATE MACHINE

U11
AT28C16 IO

C11
CAP 0.1uF LP

J6
POSJMP
P6 + 5V

CDP 1854 UART

U14
CDP 1854

C14
CAP 0.1uF LP

J3
POSJMP
P3 + 5V

FTDI DEVICE

JP1
FTDI_DEVICE

UART STATUS LED INTERFACE

U12.1 74HC04 2023 JAN
U12.2 74HC04 2023 JAN
U12.3 74HC04 2023 JAN
U12.4 74HC04 2023 JAN
U12.5 74HC04 2023 JAN
U12.6 74HC04 2023 JAN

H3
6 PIN 2X3 HDR

C12
CAP 0.1uF LP
U12.7
74HC04 2023 JAN

C10
CAP 0.1uF LP
U10.3
74HC109 JAN 2023

TITLE: UART

REV: 1.0

Company: Your Company

Sheet: 1/1

嘉立创EDA

Date: 2023-02-19   Drawn By: jeff.truck

		Control Address											Address	Address	EEPROM Data Bits								EEPROM BYTE	EEPROM BYTE
		A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0			SM-D7	SM-D6	SM-D5	SM-D4	SM-D3	SM-D2	SM-D1	SM-D0		
UART Pin Mappings to EEPROM Data Bits															BUS DIR	N/C	CS2-N	N/C	N/C	RD-P/WR-N	RSEL-P	N/C		
Write UART Data Byte	OUT6	1	1	1	1	1	1	1	1	1	1	0	07FE	2046	1	1	0	1	1	0	0	1	D9	217
Read UART Data Byte	IN6	1	1	1	1	1	1	1	1	1	0	1	07FD	2045	0	1	0	1	1	1	0	1	5D	93
Write UART Control Register	OUT7	1	1	1	1	1	1	1	1	0	1	1	07FB	2043	1	1	0	1	1	0	1	1	DB	219
Read UART Status Register	IN7	1	1	1	1	1	1	1	0	1	1	1	07F7	2039	0	1	0	1	1	1	1	1	5F	95
ALL OTHER BYTES															1	1	1	1	1	1	1	1	FF	255

TITLE: STATE MACHINE LOGIC

REV: 1.0

Company: Your Company

Sheet: 1/1

Date: 2023-03-17   Drawn By: jeff.truck