## SDK MEC80 Connecter Pin Assignment

AD9866	RXCLK(J3)	- T7 T9 R9 R3 P8 P1 M8 P2 N6	VCC3P3  RESET_EXPn  EG_P1  EG_P2  EG_P3  EG_P4  EG_P5  EG_P6  EG_P7  EG_P8  GND	1 3 5 7 9 11 13 15 17	2 4 6 8 10 12 14 16	VCC3P3  - EG_P35 EG_P36 GND EG_P37 EG_P38 EG_P38	- - T8 R8 - P6 N8	3V3 PWREN# CLK(1) - GND ADCMOSI	J5 TP6	3V3		3	3V3
AD9866  TP1  Paddle Dash CN3-10  AD9866	RXCLK(J3)	T9 R9 R3 P8 P1 M8 P2 N6 - R1	EG_P1 EG_P2 EG_P3 EG_P4 EG_P5 EG_P6 EG_P7 EG_P8	5 7 9 11 13 15	6 8 10 12 14 16	EG_P36 GND EG_P37 EG_P38	T8 R8 - P6	CLK(1) - GND ADCMOSI	TP6				
TP1 Paddle Dash CN3-10 AD9866	- PGA[0] PGA[1] PGA[2] PGA[3] PGA[4] GND GAIN/PGA[5] SEN~ SCLK SDO	R9 R3 P8 P1 M8 P2 N6	EG_P2 EG_P3 EG_P4 EG_P5 EG_P6 EG_P7 EG_P8	7 9 11 13 15	8 10 12 14 16	EG_P36 GND EG_P37 EG_P38	R8 - P6	- GND ADCMOSI					
Paddle Dash CN3-10 AD9866	PGA[0] PGA[1] PGA[2] PGA[3] PGA[4] GND GAIN/PGA[5] SEN~ SCLK SDO	R3 P8 P1 M8 P2 N6 - R1	EG_P3 EG_P4 EG_P5 EG_P6 EG_P7 EG_P8	9 11 13 15 17	10 12 14 16	GND EG_P37 EG_P38	- P6	ADCMOSI					
AD9866	PGA[0] PGA[1] PGA[2] PGA[3] PGA[4] GND GAIN/PGA[5] SEN~ SCLK SDO	P8 P1 M8 P2 N6 - R1	EG_P4 EG_P5 EG_P6 EG_P7 EG_P8	11 13 15 17	12 14 16	EG_P37 EG_P38	P6	ADCMOSI	CN3-2				
AD9866	PGA[1] PGA[2] PGA[3] PGA[4] PGA[4] GND GAIN/PGA[5] SEN~ SCLK SDO	P1 M8 P2 N6 - R1	EG_P5 EG_P6 EG_P7 EG_P8	13 15 17	14 16	EG_P38			CN3-2	1	,	4	i
AD9866	PGA[2] PGA[3] PGA[4] GND GAIN/PGA[5] SEN~ SCLK SDO	M8 P2 N6 - R1	EG_P6 EG_P7 EG_P8	15 17	16	_	N8		0.10 =	ı			
AD9866 AD9866 AD9866 AD9866 AD9866 AD9866 AD9866 AD9866	PGA[3] PGA[4] GND GAIN/PGA[5] SEN~ SCLK SDO	P2 N6 - R1	EG_P7 EG_P8	17		FG P39	110	ADCCLK	CN3-4				
AD9866 AD9866 AD9866 AD9866 AD9866 AD9866 AD9866	PGA[4] GND GAIN/PGA[5] SEN~ SCLK SDO	N6 - R1	EG_P8		12		M7	cwkey_i	CN3-3	Paddle Dot	ı		
AD9866 AD9866 AD9866 AD9866 AD9866	GND GAIN/PGA[5] SEN~ SCLK SDO	- R1	_	19	10	EG_P40	L8	ADCMISO	CN3-6				
AD9866 AD9866 AD9866 AD9866 AD9866	GAIN/PGA[5] SEN~ SCLK SDO		GND	13	20	EG_P41	L7	cwkey_o	CN3-5		ı		
AD9866 AD9866 AD9866 AD9866 AD9866	SEN~ SCLK SDO			21	22	GND	-	GND			ı		
AD9866 AD9866 AD9866 AD9866	SCLK SDO	NIT	EG_P9	23	24	EG_P42	M6	MSCK	U2-1	SSCK	-	10	SCLK
AD9866 AD9866 AD9866	SDO	N5	EG_P10	25	26	EG_P43	T2	MSI	U2-3	MOSI		9	SDIN
AD9866 AD9866		K1	EG_P11	27	28	EG_P44	G5	nADCCS	CN3-8				
AD9866		K2	EG_P12	29	30	EG_P45	F3	ptt_i	CN3-7		ı		
	SDIO	P11	EG_P13	31	32	GND	-	GND		GND		2	GND
	GND	-	GND	33	34	EG_P46	N16	MSO	U2-4	CDIN -	<b></b>	6	DIN
AD9866	TXCLK	L2	EG_P14	35	36	EG_P47	L1	MCSn	U2-5	nCS -	, <b>&gt;</b>	8	nCS
AD3000	TXEN	P16	EG_P15	37	38	EG_P48	R16	-	TP5	CLRCIO	<b></b>	1	LRCIN/OUT
AD9866	RXEN	P3	EG_P16	39	40	EG_P49	N3	RXCLK(J6)	AD9866				
AD9866	ADIO0	N1	EG_P17	41	42	EG_P50	N2	-	TP4	CMCLK -	<b></b>	11	MCLK
AD9866	ADIO1	L4	EG_P18	43	44	GND	-	GND					
AD9866	ADIO2	L3	EG_P19	45	46	EG_P51	J2	-	J4	SideTone(SQW)			
AD9866	ADIO3	J1	EG_P20	47	48	EG_P52	T11	-	TP3	CBCLK	-	5	BCLK
AD9866	ADIO4	T10	EG_P21	49	50	EG_P53	N11	PTT#	PCIE		- 		
AD9866	ADIO5	G2	EG_P22	51	52	EG_P54	P14	USEROUT0	PCIE		I	cf. for che	ck
	GND	-	GND	53	54	GND	-	GND				CLRCIO	48kHz
AD9866	ADIO6	G1	EG_P23	55	56	EG_P55	N12	USEROUT1	PCIE			CMCLK	12.288MHz
AD9866	ADIO7	N14	EG_P24	57	58	EG_P56	L14	USEROUT2	PCIE			CBCLK	3.072MHz
AD9866	ADIO8	F1	EG_P25	59	60	EG_P57	L15	USEROUT3	PCIE		• 		
AD9866	ADIO9	L16	EG_P26	61	62	EG_P58	K15	USEROUT4	PCIE		Ì		
AD9866	ADIO10	F2	EG_P27	63	64	EG_P59	J14	USEROUT5	PCIE		]		
AD9866	ADIO11	J13	EG_P28	65	66	EG_P60	T7	USEROUT6	PCIE		]		
AD9866	MODE	M10	EG_P29	67	68	-	-	-			Ì		
	-	-	-	69	70	-	-	-			]		
	-	-	-	71	72	-	-	-			]		
PCIE	PTT#	-	-	73	74	-	-	-			]		
PCIE	USEROUT0	-	-	75	76	GND	-	GND			]		
	_	-	-	77	78	EXP_PRESENT	EXP_PRESENT	DVDD			I		
		· · · · · · · · · · · · · · · · · · ·	VCC5P0	_	80						,		

Keyer (Squarewave only) Min. case + Audio Codec (Sinewave) (Pull-Up by FPGA)

Not assigned: CDOUT (Mic In)