SDK MEC80 Connecter Pin Assignment

Keyer	Fr/To	Signal	SDK FPGA	MEC80				SDK FPGA	Signal	Fr/To	Keyer
		3V3	-	VCC3P3	1	2	VCC3P3	-	3V3		3V3
	AD9866	RESET~	T7	RESET_EXPn	3	4	-	-	PWREN#	J5	
	AD9866	RXCLK(J3)	T9	EG_P1	5	6	EG_P35	T8	CLK(1)		
	TP1	-	R9	EG_P2	7	8	EG_P36	R8	-	TP6	
Paddle Dash	CN3-10	-	R3	EG_P3	9	10	GND	-	GND		
	AD9866	PGA[0]	P8	EG_P4	11	12	EG_P37	P6	ADCMOSI	CN3-2	
	AD9866	PGA[1]	P1	EG_P5	13	14	EG_P38	N8	ADCCLK	CN3-4	
	AD9866	PGA[2]	M8	EG_P6	15	16	EG_P39	M7	cwkey_i	CN3-3	Paddle Dot
	AD9866	PGA[3]	P2	EG_P7	17	18	EG_P40	L8	ADCMISO	CN3-6	
	AD9866	PGA[4]	N6	EG_P8	19	20	EG_P41	L7	cwkey_o	CN3-5	
		GND	-	GND	21	22	GND	-	GND		
	AD9866	GAIN/PGA[5]	R1	EG_P9	23	24	EG_P42	M6	MSCK	U2-1	SSCK
	AD9866	SEN~	N5	EG_P10	25	26	EG_P43	T2	MSI	U2-3	MOSI
	AD9866	SCLK	K1	EG_P11	27	28	EG_P44	G5	nADCCS	CN3-8	
	AD9866	SDO	K2	EG_P12	29	30	EG_P45	F3	ptt_i	CN3-7	
	AD9866	SDIO	P11	EG_P13	31	32	GND	-	GND		GND
		GND	-	GND	33	34	EG_P46	N16	MSO	U2-4	CDIN
	AD9866	TXCLK	L2	EG_P14	35	36	EG_P47	L1	MCSn	U2-5	nCS
	AD9866	TXEN	P16	EG_P15	37	38	EG_P48	R16	-	TP5	CLRCIO
	AD9866	RXEN	P3	EG_P16	39	40	EG_P49	N3	RXCLK(J6)	AD9866	
	AD9866	ADIO0	N1	EG_P17	41	42	EG_P50	N2	-	TP4	CMCLK
	AD9866	ADIO1	L4	EG_P18	43	44	GND	-	GND		
	AD9866	ADIO2	L3	EG_P19	45	46	EG_P51	J2	-	J4	SideTone(SQW)
	AD9866	ADIO3	J1	EG_P20	47	48	EG_P52	T11	-	TP3	CBCLK
	AD9866	ADIO4	T10	EG_P21	49	50	EG_P53	N11	PTT#	PCIE	
	AD9866	ADIO5	G2	EG_P22	51	52	EG_P54	P14	USEROUT0	PCIE	
		GND	-	GND	53	54	GND	-	GND		
	AD9866	ADIO6	G1	EG_P23	55	56	EG_P55	N12	USEROUT1	PCIE	
	AD9866	ADIO7	N14	EG_P24	57	58	EG_P56	L14	USEROUT2	PCIE	
	AD9866	ADIO8	F1	EG_P25	59	60	EG_P57	L15	USEROUT3	PCIE	
	AD9866	ADIO9	L16	EG_P26	61	62	EG_P58	K15	USEROUT4	PCIE	
	AD9866	ADIO10	F2	EG_P27	63	64	EG_P59	J14	USEROUT5	PCIE	
	AD9866	ADIO11	J13	EG_P28	65	66	EG_P60	T7	USEROUT6	PCIE	
	AD9866	MODE	M10	EG_P29	67	68	-	-	-		
		-	-	-	69	70	-	-	-		
		-	-	-	71	72	-	-	-		
	PCIE	PTT#	-	-	73	74	-	-	-		
	PCIE	USEROUT0	-	-	75	76	GND	-	GND		
		-	-	-	77	78	EXP_PRESENT	EXP_PRESENT	DVDD		
		FPGA5V	-	VCC5P0	79	80	VCC5P0	-	FPGA5V		

Audio Codec Board	
3	3V3
10	SCLK
9	SDIN
2	GND
6	DIN
8	nCS
1	LRCIN/OUT
11	MCLK
5	BCLK

cf. for check

CLRCIO	48kHz
CMCLK	12.288MHz
CBCLK	3.072MHz

Min. case

Keyer (Squarewave only)
+ Audio Codec (Sinewave)

Not assigned :
(Pull-Up by FPGA)

CDOUT (Mic In)