# A Log-Domain Implementation of the Diffusion Network in Very Large Scale Integration

**Authored by:**

Hsin Chen
Yi-da Wu
Shi-jie Lin

**Abstract**

The Diffusion Network(DN) is a stochastic recurrent network which has been shown capable of modeling the distributions of continuous-valued, continuous-time paths. However, the dynamics of the DN are governed by stochastic differential equations, making the DN unfavourable for simulation in a digital computer. This paper presents the implementation of the DN in analogue Very Large Scale Integration, enabling the DN to be simulated in real time. Moreover, the log-domain representation is applied to the DN, allowing the supply voltage and thus the power consumption to be reduced without limiting the dynamic ranges for diffusion processes. A VLSI chip containing a DN with two stochastic units has been designed and fabricated. The design of component circuits will be described, so will the simulation of the full system be presented. The simulation results demonstrate that the DN in VLSI is able to regenerate various types of continuous paths in real-time.

## 1 Paper Body

In many implantable biomedical microsystems [1, 2], an embedded system capable of recognising high-dimensional, time-varying signals have been demanded. For example, recognising multichannel neural activity on-line is important for implantable brain-machine interfaces to avoid transmitting all data wirelessly, or to control prosthetic devices and to deliver bio-feedbacks in realtime [3]. The Diffusion Network (DN) proposed by Movellan is a stochastic recurrent network whose stochastic dynamics can be trained to model the probability distributions of continuous-time paths by the Monte-Carlo Expectation-Maximisation (EM) algorithm [4, 5]. As stochasticity is useful for generalising the natural variability in data [6, 7], the DN is further shown suitable for recognising noisy, continuous-time biomedical data [8]. However, the stochastic dynamics of the DN is defined by a set of continuous-time, stochastic differential equations (SDEs). The speed

of simulating stochastic differential equations in a digital computer is inherently limited by the serial processing and numerical iterations of the computer. Translating the DN into analogue circuits is thus of great interests for simulating the DN in real time by exploiting the natural, differential current-voltage (I-V) relationship of capacitors [9]. This paper presents the implementation of the DN in analogue Very Large Scale Integration (VLSI). To minimise the power consumption, the power supply voltage is only 1.5V, and most transistors are operated in subthreshold regions. As the reduced supply voltage limits directly the dynamic range available for voltages across capacitors, the log-domain representation proposed in [10] is applied to the DN, allowing diffusion processes to be simulated in a limited voltage ranges. After a brief 1

introduction to the DN, the following sections will derive the log-domain representation of the DN and describe its corresponding implementation in analogue VLSI. ?jj

?(xi ) EXP

xj ?ij

?ij ? ?j

?ji

xi

xk

?

dB dt

?j xof f

Figure 1: The architecture of a Diffusion Network with one visible and two hidden units

?jj

xj

EXP

?kk

?j

?j + ??ij ?i

VXj

?ii

2

EXP

EXP

CXj

?j Is

?(xj ) Is

xof f

Figure 2: The block diagram of a DN unit in VLSI

The Diffusion Network

As shown in Fig. 1, the DN comprises n continuous-time, continuous-valued stochastic units with fully recurrent connections. The state of the j th unit at time t, xj (t), is governed by

dB(t) dxj (t) = ?j xj (t) + ? ? dt dt

(1)

where ?j (t) is a deterministic drift term given in (2), ? a constant, and dB(t) the Brownian motion. The Brownian motion introduces the stochasticity, enriching greatly the representational capability of the DN [5].

n X

?ij ? ? xi (t) (2) ?j xj (t) = ?j ? ??j xj (t) + ?j + i=1

??1 j

?ij defines the connection weight from unit i to unit j. and ??1 j represent the input capacitance th and transmembrane resistance, respectively, of the j unit. ?j is the input bias, and ? is the sigmoid function given as a 2 ?(xj ; a) = ?1 + = tanh xj (3) 1 + e?axj 2 where a adapts the slope of the sigmoid function. As shown in Fig. 1, the DN contains both visible(white) and hidden(grey) stochastic units. The learning of the DN aims to regenerate at visible units the probability distribution of a specific set of continuous paths. The number of visible units thus equals the dimension of the data to be modeled, while the minimum number of hidden units required for modeling data satisfactorily is identified by experimental trials. During training, visible units are ?clamped? to the dynamics of the training dataset, and the dynamics of hidden units are Monte-Carlo sampled for estimating optimal parameters (?ij , ?j , ?j , ?j ) that maximise the expectation of training data [5]. After training, all units are given initial values at t = 0 only to sample the dynamics modeled by the DN. The similarity between the dynamics of visible units and those of training data indicate how well the DN models the data. 2.1

Log-domain translation

To maximise the dynamic ranges for diffusion processes in VLSI, the stochastic state xj (t) is represented as a current and then logarithmically-compressed into a voltage VXj in VLSI [11]. The logarithmic compression allows xj (t) to change over three decades within a limited voltage range for VXj . The voltage representation VXj further facilitates the exploitation of the nature, differential (I-V) relationship of a capacitor to simulate SDEs in real-time and in parallel. 2

The logarithmic relationship between xj (t) and VXj can be realised by the exponential I-V characteristics of a MOS transistor in subthreshold operation [12]. To keep xj (t) a non-negative value (current) in VLSI, an offset xof f is added to xj (t), resulting in the following relationship between xj (t) and VXj . xj + xof f ? IS ? e?VXj , dxj = ?IS ? e?VXj ? dVXj

(4)

where Is and ? are process-dependent constants extractable from simulated I-V curves of transistors. Substituting Eq. (4) into Eq. (1) then translates the diffusion process in Eq. (1) into the following equation.

n X dVXj ? dBj (t) ??VXj CXj ? = ?j + ?ij ?(xi ) ? e??VXj + ?e + ?j xof f ? e??VXj ? ?j IS dt ? dt j i=1 (5) where CXj equals ?/?j . Fig. 2 illustrates the block diagram for implementing Eq. (5) in VLSI. CXj is a capacitor and VXj the voltage across the capacitor. Each term on the right hand side of Eq. (5) then corresponds to a current flowing into CXj . Let (VP ? VN ) and IV AR represent the differential input voltage and the input current of an EXP-element,

respectively. Each EXP-element in Fig. 2 produces an output current of Iout = IV AR ? e?(VP ?VN ) . Therefore, the EXP-elements implement the first three terms multiplied with e??VXj in accordance with Eq. (5). The last term, ?j IS , is a constant and is thus implemented by a constant current source. Finally, the Pnsigmoid circuit transforms xj into ?(xj ) and the multipliers output a total current proportional to i=1 ?ij ? ?(xi ). 7 6 5 4 3

7 6 5 4 3 0

100

200 300 Time samples

400

500

0 100 200 300 400 500 600 700 800 900 1000 Time samples

Figure 3: The stochastic dynamics (gray lines) regenerated by the DN trained on the bifurcating curves (black lines).

Figure 4: The stochastic dynamics (gray lines) regenerated by the DN trained on the sinusoidal curve (the black line). 10 9 8 Unit 2

7.5 6.5 5.5 4.5 3.5 2.5

6 5 4

0

20

40 Time samples

60

80

Figure 5: The stochastic dynamics (gray lines) regenerated by the DN trained on the QRS segments of electrocardiograms (black lines). 2.2

7

3.5

4.5

5.5 6.5 Unit 1

7.5

8.5

Figure 6: The stochastic dynamics (gray lines) regenerated by the DN trained on the handwritten ? (the black line).

Adapting ?j instead of ?j

The DN has been shown capable of modeling various distributions of continuous paths by adapting wij , ?j , and ?j in [5]. An adaptable ?j corresponds to an adaptable CXj , but a tunable capacitor with a wide linear range is not easy to implement in VLSI. As Eq. (2) indicates that ?j is complementary 3

to ?j in determining the ?time constant? of the dynamics of the unit j, the possibility of adapting ?j instead of ?j is investigated by Matlab simulation. With ?j = 1, the DN was trained to model different data by adapting ?ij , ?j , and ?j for 100 epochs. A DN with one visible and one hidden units was proved capable of regenerating the dynamics of bifurcating curves (Fig. 3), sinusoidal waves (Fig. 4), and electrocardiograms (Fig. 5). Moreover, a DN with only two visible units was able to regenerate the handwritten ? satisfactorily, as illustrated in Fig. 6. The promising results supported the suggestion that

adapting ?j instead of ?j also allowed the DN to model different data. As a variable ?j simply corresponded to a tunable current source ?j IS in Fig. 2, the VLSI implementation was greatly simplified. 2.3

Parameter mappings

Table 1 summarises the parameter mappings between the numerical simulation and the VLSI implementation. All variables except for VXj in Fig. 2 are represented as currents in VLSI. The unit currents (Iunit ) of xj , ?ij , and ?j are defined as 10 nA to match the current scales of transistors in subthreshold operation, as well as to reduce the power consumption. Moreover, extensive simulations indicate that the dynamic ranges required for modeling various data are [?3, 5] for xj and [?30, 30] for ?ij . With xof f = 5 in Eq. (4), i.e. xof f = 50nA in VLSI, VXj ranges from 773 to 827 mV. While the diffusion process in Eq. (1) is iterated with ?t = 0.05 in numerical simulation, ?t = 0.05 is set to be 5 ?s in VLSI, corresponding to a reasonable sampling rate (200kHz) at which most instruments can sample multiple channels(units) simultaneously. Finally, the unit capacitance for 1/?j is calculated as Cunit = Iunit ? ?tunit /VXj,unit , equaling 1 pF and resulting in CXj = ? ? Cunit = 30 pF. Table 1: Parameter mappings between numerical simulation and VLSI implementation parameter xj xof f VXj ?, ? ?(xj ) CXj ?t ?

3

numeric -3?5 5 0.773?0.827 -30?30 -1?1 ?/?j = 30 0.05 0.5?2

circuit -30?50 nA 50 nA 773?827 mV -300?300 nA -400?400 nA 30 pF 5 ?s 0.5?2

comment Iunit = 10 nA offset term in Eq. (4) VXj,unit = 1 V Iunit = 10 nA activation function Cunit = 1 pF tunit = 0.1 ms

Circuit implementation

A DN with two stochastic units have been designed with the CMOS 0.18 ?m technology provided by the Taiwan Semiconductor Manufacturing Company (TSMC). The following subsections introduce the design of each component circuit. 3.1 The EXP element Fig. 7(b) shows the schematics of the EXP element. With M1 and M2 operated in the subthreshold region, the output current is given as

1 (VP ? VN ) (6) Iout = IB ? exp nUT where UT denotes the thermal voltage and n the subthreshold slope factor. Comparing Eq. (6) with Eq. (4) reveals that ? = 1/nUT . As the drain current (Id ) of a transistor in subthreshold operation is exponentially proportional to its gate-to-source voltage (VGS ) as Id ? eVGS /nUT , ? = 1/nUT is extracted to be 30 by plotting log(Id ) versus VGS in SPICE. Transistors M3-M5 form an active biasing circuit that sinks IB + Iout . By adjusting the gate voltage of M3 through the negative feedback, Iout is allowed to change over several decades. In addition, 4

IOU T

VP VN

M7

IOU T

EXP

0 IOU T

IB
VN
VP M1
IB
0 IOU T
IB
IOU T
IB M5
IV AR

n actually depends on the gate voltage and introduces variability to ? [13]. To prevent the variable ? from introducing simulation errors, all EXP elements of the DN unit are biased with a constant IB = 100 nA. As shown by Fig. 7(a), Iout of each element is then re-scaled by the one-quadrant 0 current multiplier basing on translinear loops (Fig. 7(c)) [13] to produce Iout = Iout ? IV AR /IB , where IV AR represents the current input to each element in Fig. 2 (e.g.??? or ?xof f ).

IV AR
M2
M3
M4
M1 VS M2
Vbiasn
Vbiasn Vref
M4
M6
M3
(a)
M5
(b)
(c)

Figure 7: The circuit diagram of the EXP element.

3.2

Current multipliers

Four-quadrant multipliers basing on translinear loops [13] are employed to calculate ??ij ?(xi ) in Eq. (5). Both ?ij and ?(xi ) are represented by differential currents as

?ij = I?+ ? I?? , ?(xi ) = I?+ ? I??

(7)

Let the differential current (IZ+ ? IZ? ) represents the multiplier?s output and IU represent a unit current. Eq. (8) indicates that the four-quadrant multiplication can be composed of four one-quadrant multipliers in Fig. 7(c), as illustrated in Fig. 8.

IZ+ ? IU ? IZ? ? IU = (I?+ ? I?+ + I?? ? I?? ) ? (I?+ ? I?? + I?? ? I?+ )

(8)

I?+ IU

IZ?
Figure 8: The four-quadrant current multiplier 5
I??
IZ+
IU I?+
IU I??
I?+
IU
I??
I?+
I??

Fig. 9 shows the simulation result of the four-quadrant multiplier, exhibiting satisfactory linearity over the dynamic ranges required in Table 1.

(IZ+ ? IZ? ) in nA
500
= ?400nA = ?300nA = ?200nA = ?100nA
300
100 0 ?100
?i ?i ?i ?i
?200 ?400
= = = =
?200
gain=0.8 gain=1.0 gain=3.0 gain=5.0
400 Output current in nA
?i ?i ?i ?i
200
?i = 0 100nA 200nA 300nA 400nA
200 100 0 -100 -200 -300 -400
0
200
-500 -600
400
-400
-200 0 200 Input current in nA
(I?+ ? I?? ) in nA
Figure 9: The simulation results of the fourquadrant current multiplier 3.3
400
600
Figure 10: The simulation result of the sigmoid circuit with different Va
Sigmoid function ?(?)

Fig. 11 shows the block diagram for implementing the sigmoid function in Eq. (3). The current IXi representing xi is firstly converted into a voltage Vi by the the operational amplifier(OPA) with a voltage-controlled active resistor (VCR) proposed in [14]. Vi is then sent to an operational transconductance amplifier(OTA) in subthreshold operation, producing an output current of Is = IB tanh

1 (Vi ? Vref ) 2nUT
(9)

Since Vi ? Vref = Ri ? Ixi , with Ri representing the resistance of the VCR, the voltage Va adapts Ri and thus the slope of the sigmoid function. Finally, the 2nd generation current conveyor (CCII) in Fig. 12 [15] converts the current Is into a pair of differential currents (IOU T N , IOU T P ) ranging between ?400 nA and +400 nA. The differential currents are then duplicated for the inputs of four-quadrant multipliers of all DN units. Va

VCR
IXi
IOU T P OPA Vref
CCII
OTA Vref
IOU T N
Vref

Figure 11: The block diagram of the sigmoid circuit.

3.4 Capacitor amplification As CXi = 30 pF requires considerable chip area, CXi is implemented by the circuit in Fig. 13, utilising the Miller effect to amplify the capacitance. Let A denote the gain of the amplifier. The effective capacitance between X and Y is (1 + A) ? CX . Fig. 13 also shows the schematics of the amplifier whose gain is designed to be 2. As a result, CX = 10 pF is sufficient for providing an effective CXi of 30 pF.

VBIAS
CX VREF
X
4/4x16
M1
X
?A
Y
Y 4/4x1
CEQ = CX (1 + A)
M2

Figure 13: The circuit diagram of the capacitor amplified by the Miller effect.

6

Vbiasp 1.2V
IP
IOU T N
Isig 0.3V
VY
VX
1.2V
IN
OPA
VREF
IOU T P Vbiasn 0.3V

Figure 12: The circuit diagram of the single-to-differential current conveyor
Technology
1P6M 0.18 ?m CMOS
Power Supply
1.5 Volts
Power Consumption
345 ?Watts
Num. of Units
2
1.368?1.368mm2
Chip Area
(including pads)
Capability
1D/2D continuous paths
Max. Bandwidth
1.6 kHz
Figure 14: The chip layout and its specification.
55 50
IX1 in ?A
IX1 in ?A
50 40 30
45 40 35 30
0
0.5
1
1.5
2
0
Time in ms
0.05
0.1
0.15
0.2
0.25
0.3
Time in ms
Figure 16: The electrocardiogram dynamics regenerated by the DN chip in post-layout simulation (10 trials).
Figure 15: The sinusoidal dynamics regenerated by the DN chip in post-layout simulation (10 trials). 7
70 60
IX2 in ?A
50
IX1 in ?A
60 50 40
40 30 20

30
10 10 15 20 25 30 35 40 45 50 55
20 0
0.5
1
1.5
2
2.5
IX1 in ?A
Time in ms

Figure 17: The bifurcating dynamics regenerated by the DN chip in post-layout simulation (8 trials).

4

Figure 18: The handwritten ? regenerated by the DN chip in post-layout simulation (10 trials).

The Diffusion Network in VLSI

Fig. 14 shows the chip layout of the log-domain implementation of the DN with two stochastic units, so is the specification shown. The area of the core circuit and the capacitors are 0.306 mm2 and 0.384 mm2 , respectively. The total power consumption is merely 345 ?W, by the merit of low supply voltage (1.5V) and subthreshold operation. The chip has been taped out for fabrication with the CMOS 0.18 ?m Technology by the TSMC. The post-layout simulations are shown in Fig. 15?18 and described as follows. With one unit functioning as a visible unit and the other as a hidden unit, the parameters of the DN was programmed to regenerate the one-dimensional paths in Sec. 2.2. The noise current ?? ? dB dt was simulated by a piecewise-linear current source with random amplitudes in the SPICE. As shown by Fig. 15-17, the visible unit was capable of regenerating the sinusoidal waves, the electrocardiograms, and the bifurcating curves with negligible differences from Fig. 3-5. Moreover, as both units functioned as visible units, the DN was capable of regenerating the handwritten ? as Fig. 18. These promising results demonstrate the capability of the DN chip to model the distributions of different continuous paths reliably and power-efficiently. After chip is fabricated in August, the chip will be tested and the measurement results will be presented in the conference.

5

Conclusion

The log-domain representation of the Diffusion Network has been derived and translated into analogue VLSI circuits. Based on well-defined parameter mappings, the DN chip is proved capable of regenerating various types of continuous paths, and the log-domain representation allows the diffusion processes to be simulated in real-time and within a limited dynamic range. In other words, analogue VLSI circuits are proved useful for solving (simulating) multiple SDEs in real-time and in a power-efficient manner. After verifying the chip functionality, a DN chip with a scalable number of units will be further developed for recognising multi-channel, time-varying biomedical signals in implantable microsystems. Acknowledgments The authors thank National Chip

Implementation Center (CIC) for fabrication services, and Mr. C.-M. Lai and S.-C. Sun for helpful discussions.

8

# 2 References

[1] G. Iddan, G. Meron, A. Glukhovsky, and P. Swain, ?Wireless capsule endoscopy,? Nature, vol. 405, no. 6785, p. 417, July 2000. [2] T. W. Berger, M. Baudry, J.-S. L. Roberta Diaz Brinton, V. Z. Marmarelis, A. Y. Park, B. J. Sheu, and A. R. Tanguay, JR., ?Brain-implantable biomimetic electronics as the next era in neural prosthetics,? Proc. IEEE, vol. 89, no. 7, pp. 993?1012, July 2001. [3] M. A. Lebedev and M. A. L. Nicolelis, ?Brain-machine interfaces: past, present and future,? Trends in Neuroscience, vol. 29, no. 9, pp. 536?546, 2006. [4] J. R. Movellan, ?A learning theorem for networks at detailed stochastic equilibrium,? Neural Computation, vol. 10, pp. 1157?1178, July 1998. [5] J. R. Movellan, P. Mineiro, and R. J.Williams, ?A Monte Carlo EM approach for partially observable diffusion processes: Theory and applications to neural networks,? Neural Computation, vol. 14, pp. 1507?1544, July 2002. [6] H. Chen and A. F. Murray, ?A continuous restricted Boltzmann machine with an implementable training algorithm,? IEE Proc. of Vision, Image and Signal Processing, vol. 150, no. 3, pp. 153?158, 2003. [7] D. F. Specht, ?Probabilistic neural networks,? Neural Networks, vol. 3, no. 1, pp. 109?118, 1990. [8] Y. S. Hsu, T. J. Chiu, and H. Chen, ?Real-time recognition of continuous-time biomedical signals using the diffusion network,? in Proc. of the Int. Joint Conf. on Neural Networks (IJCNN), 2008, pp. 2628?2633. [9] L. O. Chua, T. Roska, T. Kozek, and A. Zarandy, ?CNN universal chips crank up the computing power,? IEEE Circuits and Devices Mag., vol. 12, no. 4, pp. 18?28, July 1996. [10] T. Serrano-Gotarredona and B. Linares-Barranco, ?Log-domain implementation of complex dynamics reaction-diffusion neural networks,? IEEE Trans. Neural Networks, vol. 14, pp. 1337?1355, Sept. 2003. [11] D. R. Frey, ?Exponential state space filters: A generic current mode design strategy,? IEEE Trans. Circuits Syst. I, vol. 43, pp. 34?42, Jan. 1996. [12] E. Vittoz and J. Fellrath, ?CMOS analog integrated circuits based on weak inversion operation,? IEEE J. Solid-State Circuits, vol. 12, pp. 224?231, June 1977. [13] S.-C. Liu, J. Kramer, G. Indiveri, T. Delbr?uck, and R. Douglas, Analog VLSI: Circuits and Principles. The MIT Press, 2002. [14] M. Banu and Y. Tsividis, ?Floating voltage-controlled resistors in CMOS technology,? Electronics Letters, vol. 18, no. 15, pp. 678?679, July 1982. [15] C. Toumazou, F. J. Lidgey, and D. G. Haigh, Analogue IC Design: The Current-Mode Approach. Peter Peregrinus Ltd, 1990.

9