

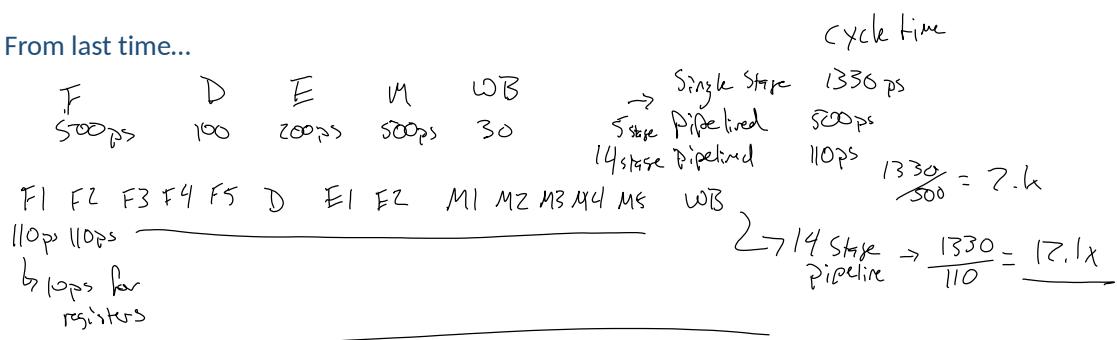
Lecture 11: More pipelining

Friday, February 1, 2019 7:51 AM

Outline

- Finish pipeline performance implications
- More multicycle/pipeline details
- Hazards

From last time...



Power? More

$$P = I C V^2 f$$

about the UP about
some

lots of
inc 750 MHz
to 96 Hz
inc to support
higher freq

Single cycle to 14 stage
f 750 MHz
 $V = 0.8$
 $V \rightarrow 1.2$
incr in power

$$\frac{9.1 \times 1.2^2}{.75 \times 0.8^2} = 27x$$

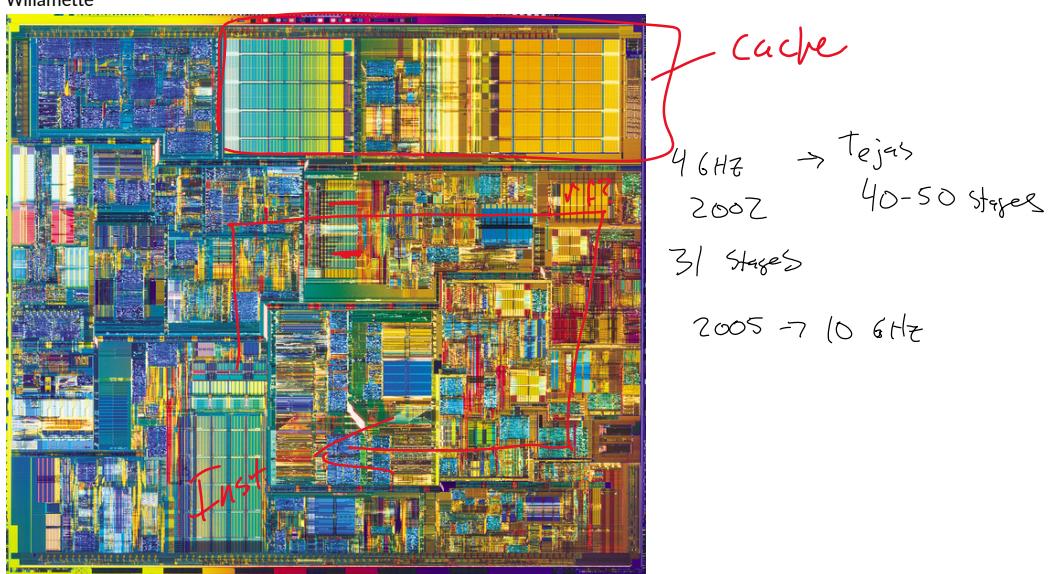
27x power incr
12x perf incr
 $27x \downarrow 12x$
 $E = P \cdot t = 27x$ incr
in energy for computation

multicore more power
efficient. Could have
used 12 single cycle

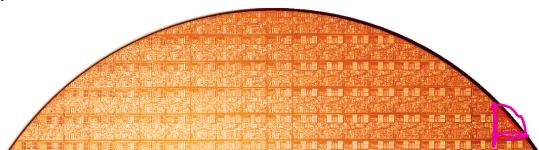
cooling problem
Using much more energy

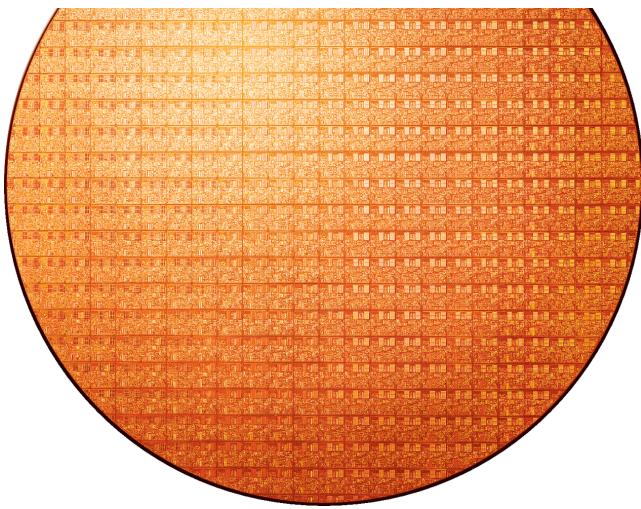
Pentium 4 (NetBurst)

Willamette

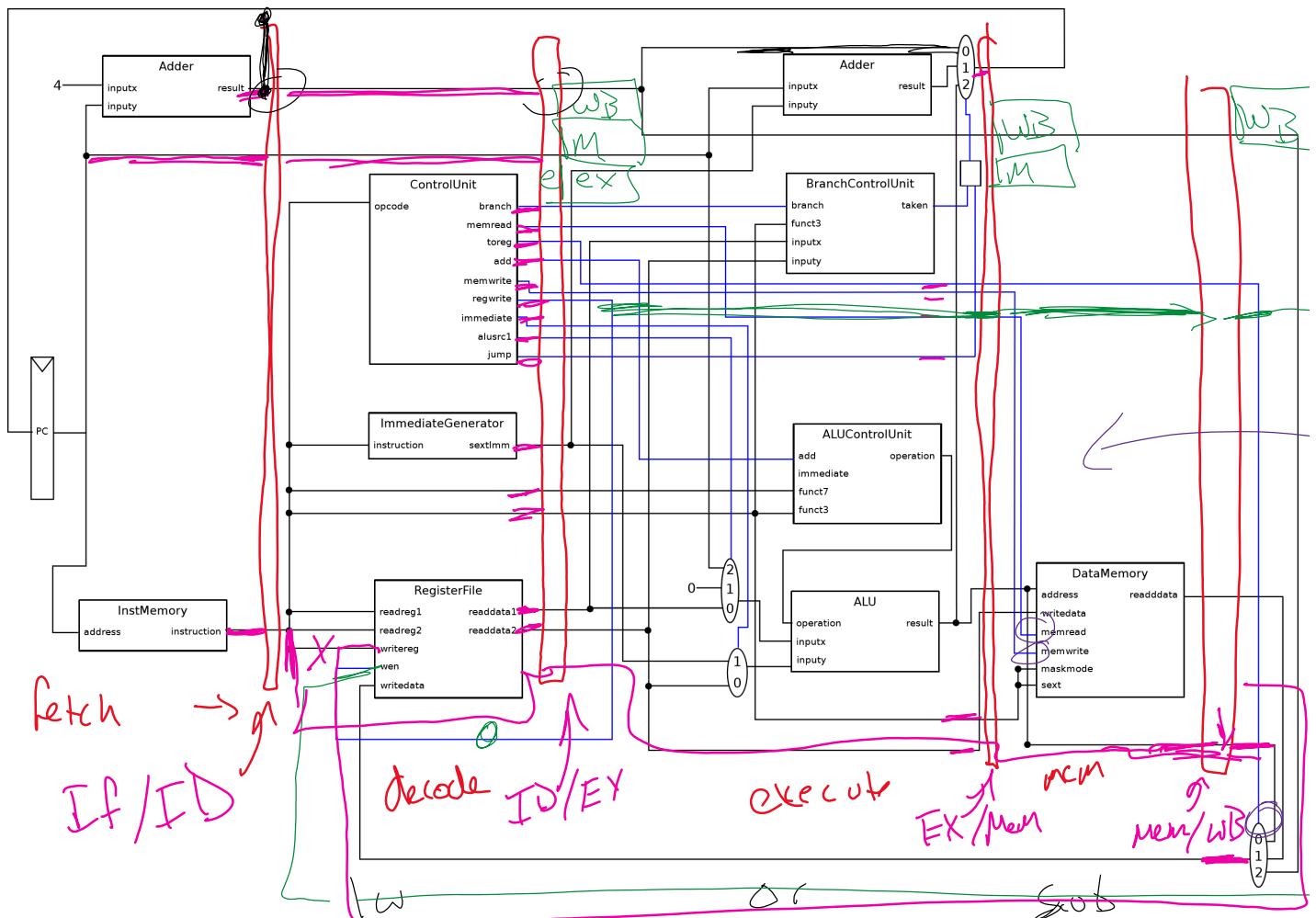


Wafer:





More multicycle/pipeline details



What will limit the PVT of above?

add x_2, x_3, x_4
 sub x_5, x_6, x_7
 or x_8, x_3, x_6
 sll x_9, x_8, x_4

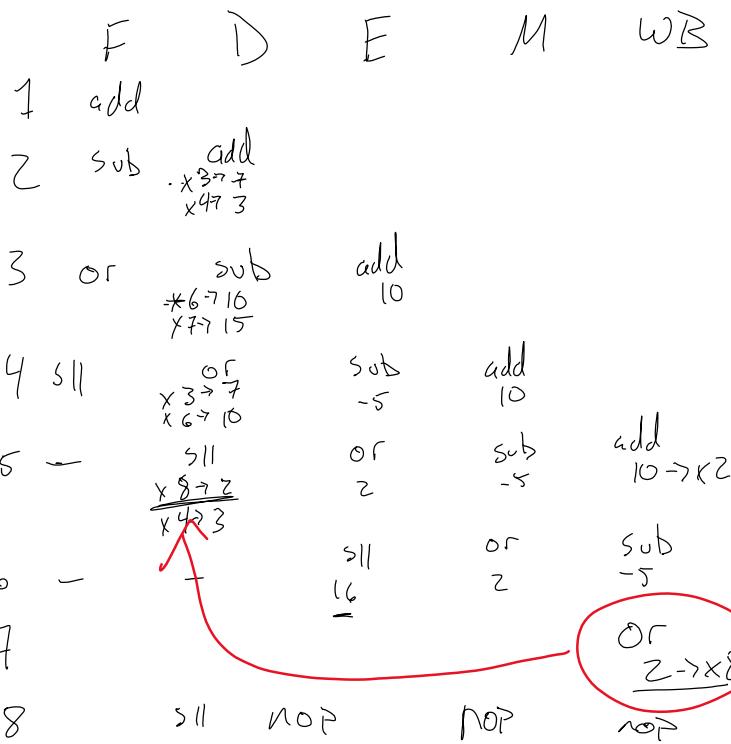
$$\begin{aligned} \rightarrow x_2 &= 10 \\ \rightarrow x_5 &= -5 \\ \rightarrow x_8 &= 2 \\ \rightarrow x_9 &= 16 \end{aligned}$$

sll depends
on or

Data dependency

add
 sub
 or
 sll
 nop
 sll

need to stall
3 cycles



Since we must
stall we call this
a data hazard

add
 $10 \rightarrow x_2$

sub
 -5

or
 2

sub
 -5

add
 $10 \rightarrow x_2$

sub
 -5

or
 2

sub
 -5

or
 $2 \rightarrow x_8$