

Lecture 9: Pipelining intro

Monday, January 28, 2019 9:06 AM

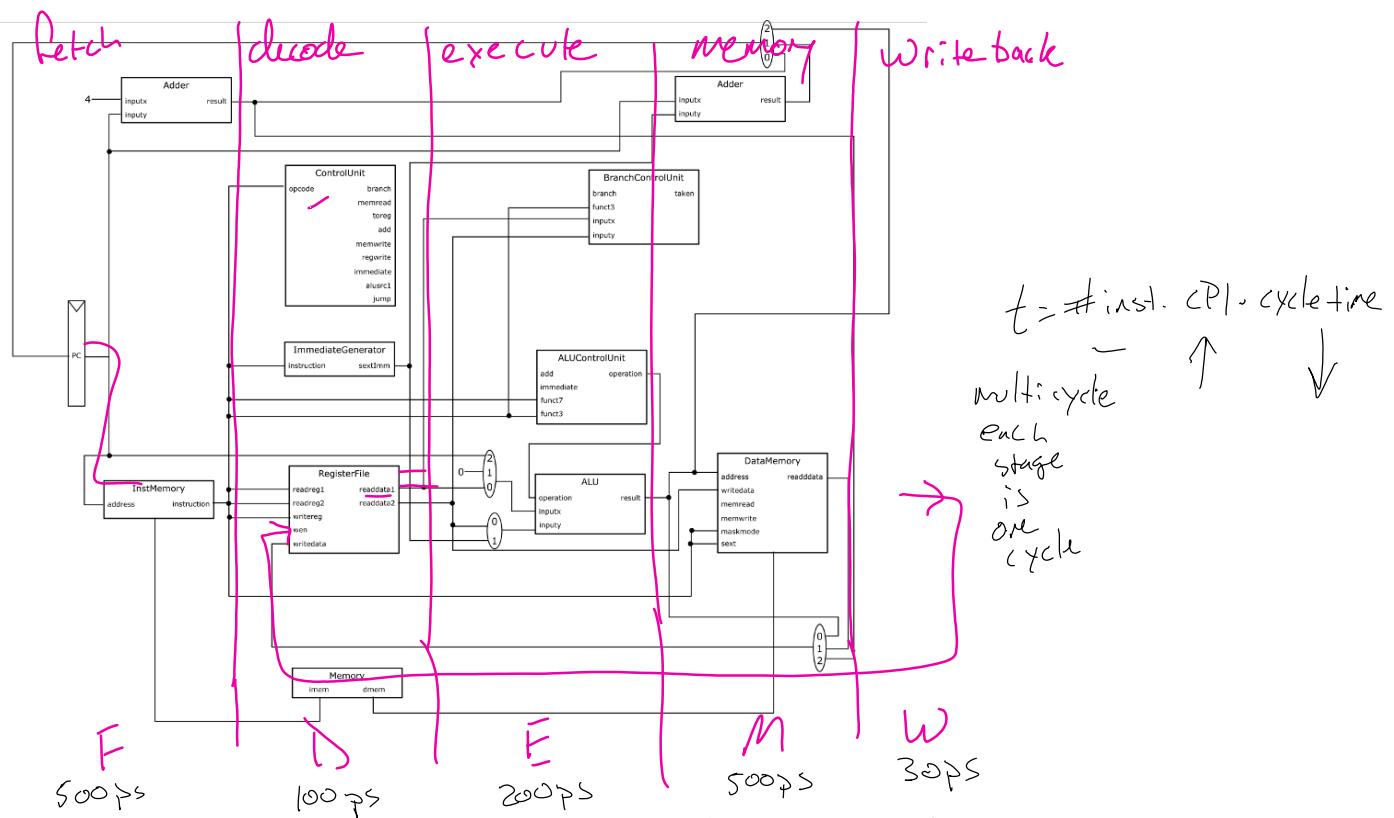
Outline

- Multicycle CPU
 - Performance
- Pipelined CPU
 - Performance

INSTALLING THE XKCD DEVELOPMENT ENVIRONMENT

- SPIN UP A VM
- SPIN UP A VM INSIDE THAT VM
- CONTINUE SPINNING UP NESTED VMs AND CONTAINERS UNTIL YOU GET FIRED

Multi cycle CPU



Single cycle CPU design

\hookrightarrow Cycle time? $\rightarrow 1330\text{ps}$

$$t = \frac{1}{f} \cdot CPI \cdot \#inst$$

$$\frac{t}{\#inst} = CPI \cdot \frac{\sum \text{cycle time}}{\#inst}$$

lw $\rightarrow 1330\text{ps}$

20%

5

"Ideal"

1 CPI processor part
adaptive or weight cycle time

bt-type $\rightarrow 830\text{ps}$

60%

4

br $\rightarrow 800\text{ps}$

10%

3

sw $\rightarrow 1300\text{ps}$

10%

4

jal $\rightarrow 830\text{ps}$

5%

4

jalr $\rightarrow 830\text{ps}$

5%

4

$$\frac{t}{\#inst} \text{ for Single cycle} = 1 \cdot 1330\text{ps}$$

average cycle time

$$\frac{t}{\#inst} \text{ for ideal} = 1 \cdot [1330 \cdot .2 + 830 \cdot .6 + 800 \cdot .1 + 1300 \cdot .1]$$

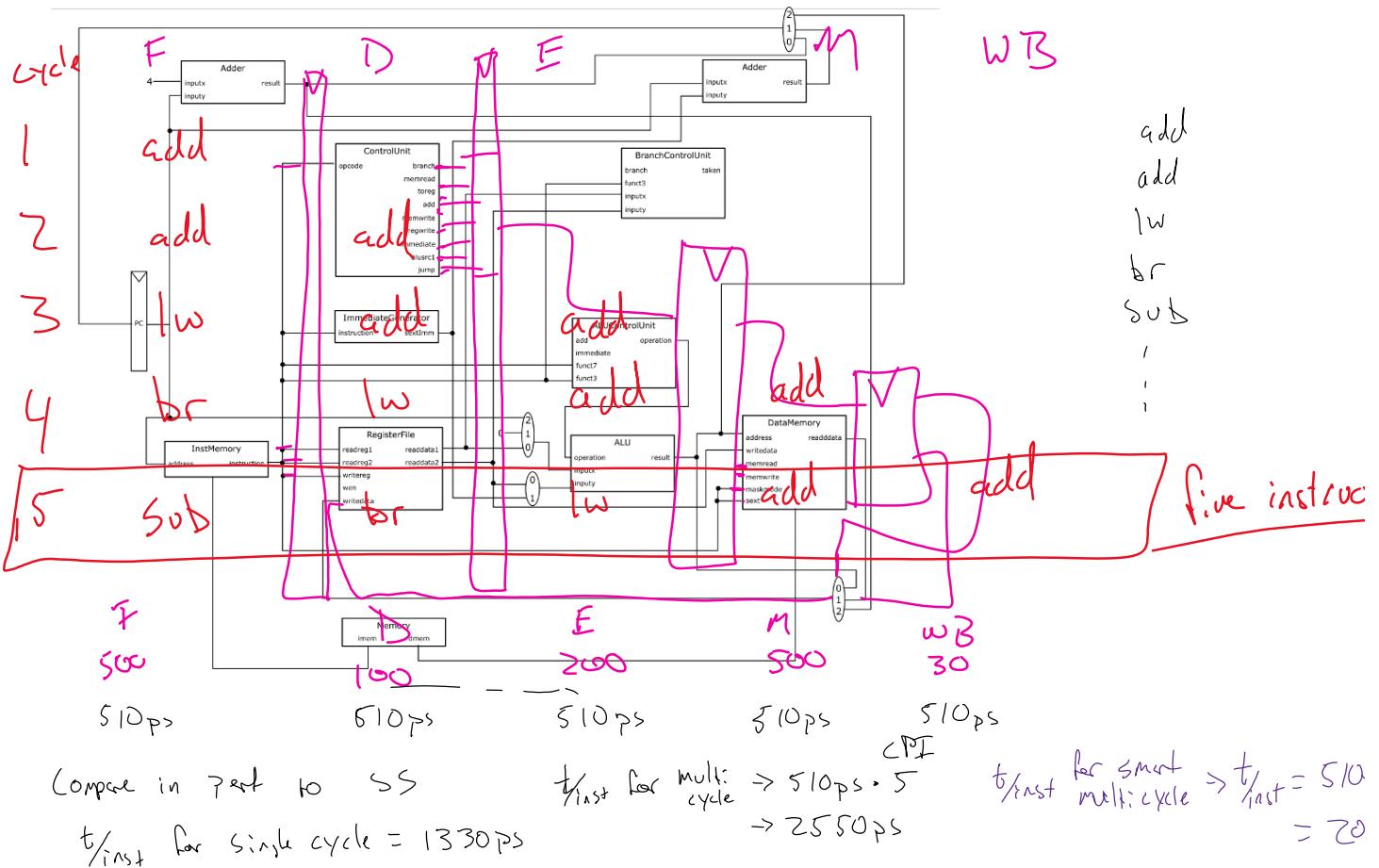
Speedup of ideal over single cycle

$$= 974\text{ps}$$

average CPI
for multicycle

$$\hookrightarrow 5 \cdot .2 + 4 \cdot .7 + 3 \cdot .1 \\ = 4.1$$

$$\frac{\text{old}}{\text{new}} = \frac{1330}{974} = 1.37x$$



Pipelined CPU performance

Parallelism

Pipelining \rightarrow CPI?

$$t_{inst} = 1 \text{ CPI} \cdot 510 \text{ ps/cycle}$$

$$= 510 \frac{\text{ps}}{\text{inst}}$$

Why not 5x?

\hookrightarrow limited by longest stage + thr's waste

Unbalanced Pipeline



speedup of pipelining compared to single cycle $\rightarrow \frac{1330}{510} = 2.6x$

speedup of pipelining compared to "ideal" SS variable cycle time $\rightarrow \frac{974}{510} = 1.91x$?

how is Pipeling faster than Ideal?

Better utilization through **parallelism**

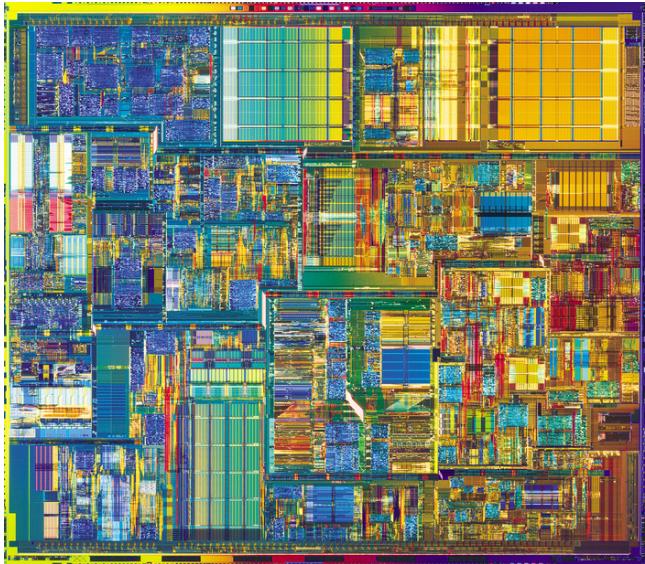
\hookrightarrow instruction-level parallelism

14 stage pipeline

speedup of 14 stage

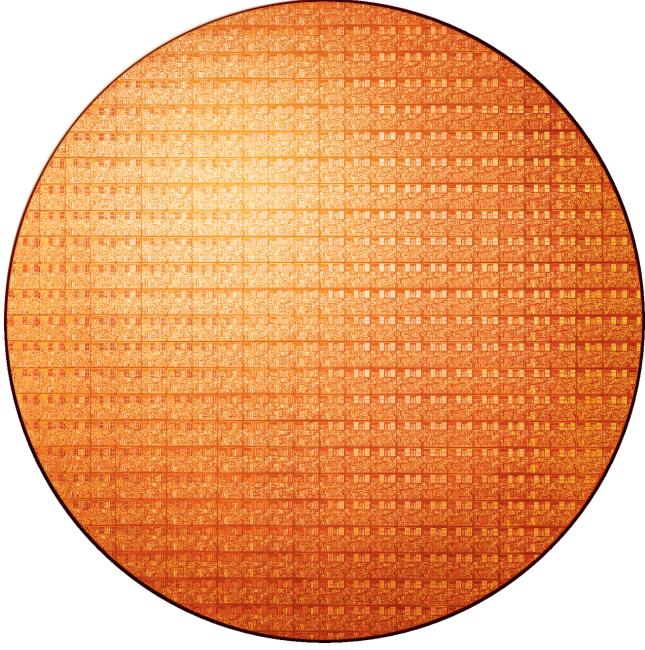
Pentium 4 (NetBurst)

Willamette



$$t_{\text{inst}} \rightarrow 1 \cdot 110 \quad \text{over } 55$$
$$\cancel{1330} \rightarrow 17.1x$$
$$\cancel{110}$$

Wafer:



Power for pipelined processors