Lab 7
Multiple Output Systems

Lab report due before your lab period on October 19–21

- For this lab, only use the 74HC08, 74HC32, and 74HC04 ICs to implement your logic, the bar LEDs as outputs, and the switches as inputs
- Find the minimal SOP expression of J and K using Karnaugh maps when you optimize the equations separately

$$J(w,x,y,z) = \sum m(1,3,9,11,12,13,14,15)$$

$$K(w,x,y,z) = \sum m(0,1,3,12,14)$$

- Calculate how many gates and total gate inputs are required to implement J and K when optimized separately
- Calculate how many gates and total gate inputs are required to implement J and K when optimized separately and when you can only use 2-input gates
- Jointly optimize J and K to use the minimum number of gates using Karnaugh maps
- Calculate how many gates and total gate inputs are required to implement J and K when jointly optimized and when you can only use 2-input gates
- Implement your jointly optimized solution using ICs
  - Verify your implementation yields the correct outputs using a truth table
  - Demonstrate your implementation to your lab TA

The report for this lab should include the following sections:

1. Description/Objectives
2. Procedure, which must include
   (a) The Karnaugh maps you used to separately minimize J and K
   (b) The Karnaugh maps you used to jointly minimize J and K
   (c) The calculations or other work showing gate and input counts
   (d) The truth table you used to test your implementation
3. Observations
4. Conclusions