Lab 2
Verification of Equivalent Logic Functions

Due before your lab period on Sept. 14–16

1. Using Logisim, implement the following logic function in gates:

$$ab + c' + abc \tag{1}$$

   - Use pins for inputs and outputs
   - Follow the tutorial (check the Help menu) if you need help

2. Generate the truth table by hand for (1) and use it to verify the operation of your circuit
3. Implement the following logic function in Logisim:

$$ab + c' \tag{2}$$

4. Verify your implementation of (2) produces the same output as your implementation of (1)
5. Show how to simplify (1) to yield (2) using only the properties on page 55 of your text. You must show *every* step and indicate which property applies to each step.

The report for this lab should include the following sections:

1. Description/Objectives
2. Procedure, which must include
   (a) The truth table you generated
   (b) Screenshot of your implementation of (1)
   (c) Screenshot of your implementation of (2)
   (d) Reduction of (1) to (2)
3. Observations
4. Conclusions