Lab 13
Sequential Taillights

Lab report due before your lab period on December 7–9
Demo before the end of lab December 7–9

- Read the description for Problem 16.27
- Use Verilog to write a module that controls the sequential taillights
  - Your Verilog module must have the following format

    ```
    module taillights(input clk, L, R, H, output reg [2:0] TL, TR);
    endmodule
    ```

  - When `L=1`, the output `TL` cycles through the sequence: 3'000, 3'b001, 3'b011, 3'b111, 3'b000, etc.
  - When `R=1`, the output `TR` cycles through the sequence: 3'000, 3'b100, 3'b110, 3'b111, 3'b000, etc.
- Demonstrate your implementation to your TA

The report for this lab should include the following sections:

1. Description/Objectives
2. Procedure
3. Observations
4. Conclusions
5. Appendix
   (a) The Verilog code for your implementation (not your testbench)