EECE 144
Fall 2011

Lab Report #7
Section 4
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1 Description/Objectives

The purpose of this lab is to find the min SOP expressions of equations J & K (Equation 1 and 2) using a minimal amount of gates and to build a circut combining the two equations using only two input gates.

$$J(w,x,y,z) = \sum m(1,3,9,11,12,13,14,15) \tag{1}$$

$$K(w,x,y,z) = \sum m(0,1,3,12,14) \tag{2}$$

2 Procedure

The first step in accomplishing this task was to create separate Karnaugh Map for expressions J & K in order to find the min SOPs of the equations and to determine the number of gates needed to implement each equation separately. The next step was to jointly optimize the two equations through the use Karnaugh Maps to produce a circuit using the minimum number of gates. Lastly, we used the Truth table (Table 1) in order to test and verify the functionality of the circuit.

The minimal SOP expression for J was found by the use of a Karnaugh Map (Figure 1) resulting in equation 3.

$$J = wx + x'z \tag{3}$$

Index	w	x	y	z	J	K
0	0	0	0	0	0	1
1	0	0	0	1	1	1
2	0	0	1	0	0	0
3	0	0	1	1	1	1
4	0	1	0	0	0	0
5	0	1	0	1	0	0
6	0	1	1	0	0	0
7	0	1	1	1	0	0
8	1	0	0	0	0	0
9	1	0	0	1	1	0
10	1	0	1	0	0	0
11	1	0	1	1	1	0
12	1	1	0	0	1	1
13	1	1	0	1	1	0
14	1	1	1	0	1	1
15	1	1	1	1	1	0

Table 1: Truth table of functions J and K.

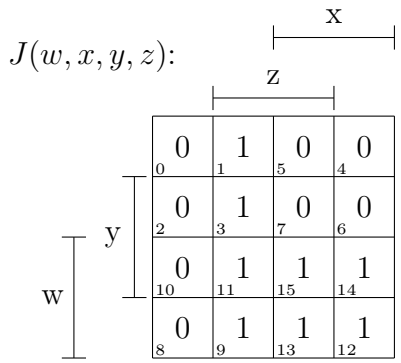

Figure 1: Karnaugh map of function J (Equation 1).

The minimal SOP expression for K was found by the use of a Karnaugh Map (Figure 2) resulting in equation 4.

$$K = w'x'y' + w'x'z + wxz' \tag{4}$$

A gifted mind of electronics can probably deduce the number of gates and gate inputs from the expressions alone. But here we appeal to the not so brilliant of us by using circuit diagrams to clearly elucidate the metrics we are seeking.

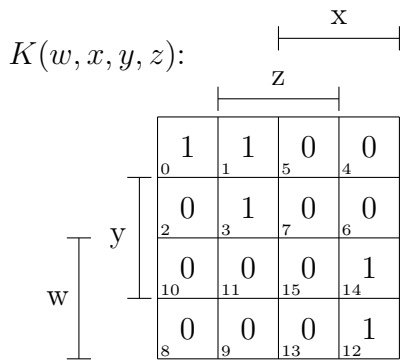

Figure 2: Karnaugh map of function K (Equation 2).

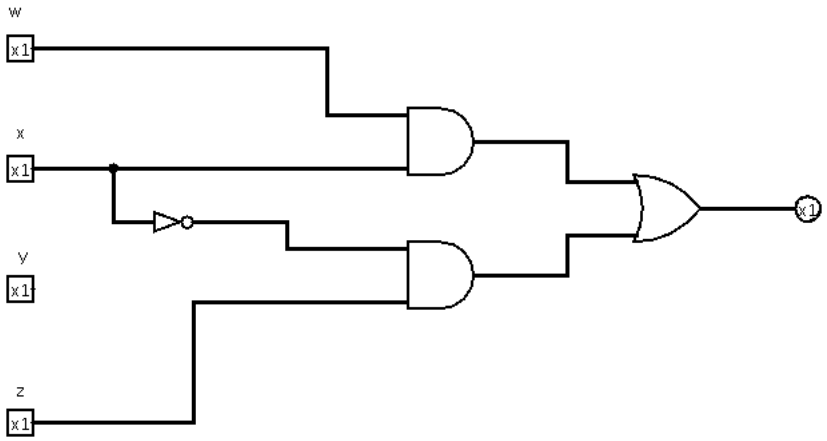

Figure 3: Circuit diagram of the minimal SOP solution of J.

Referring to the circuit for J in Figure 3 we can see that there are 2 AND gates, 1 OR gate, and 1 NOT gate. And there are 4 inputs to the AND gates, 2 inputs to the OR gate, and 1 input to the NOT gate.

Referring to the circuit for K in Figure 4 we can see that there are 3 AND gates, 1 OR gate and 4 NOT gates. And there are 9 inputs to the AND gates, 3 inputs to the OR gate, and 4 inputs to the NOT gates.

When limited to two gates the previous solution for J is the same. For K the circuit must be modified as shown in Figure 5. This results in 4 NOT gates, 6 AND gates and 2 OR gates. And there are 4 inputs to the NOT gates, 12 inputs to the AND gates and 4 inputs to the OR gates.

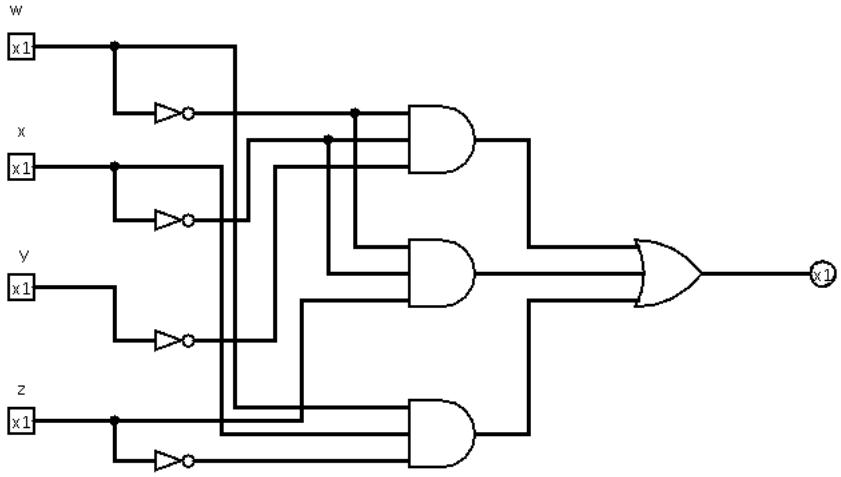

Figure 4: Circuit diagram of the minimal SOP solution of K.

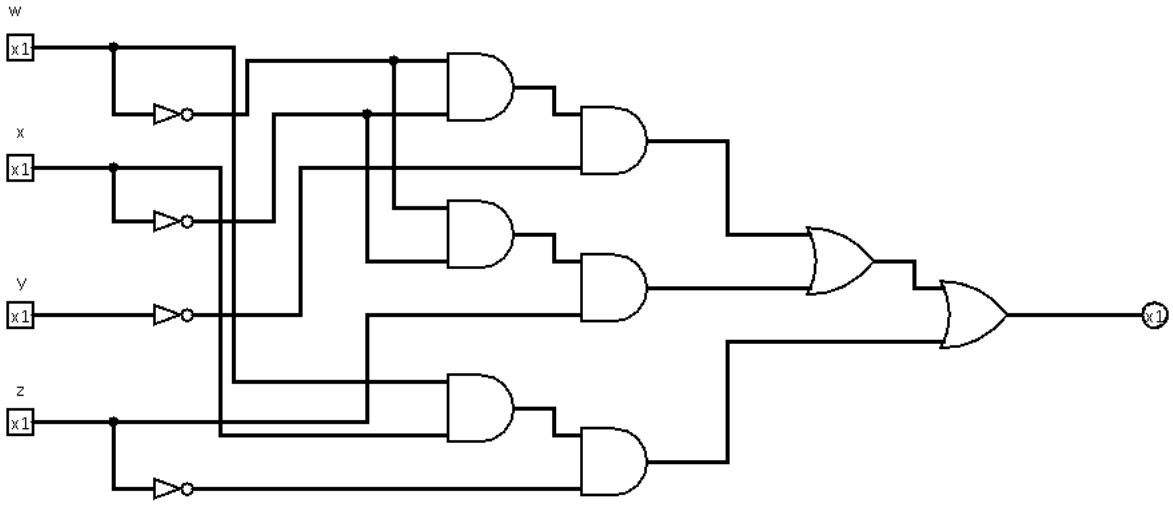

Figure 5: Circuit diagram of the minimal SOP solution of K when limited to two input gates.

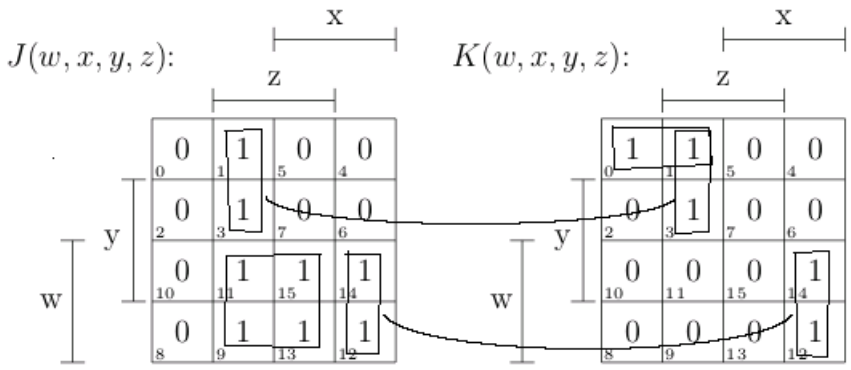

Figure 6: Jointly optimized Karnaugh maps for J and K.

A jointly optimized solution of J and K is created by combining shared terms used by both SOP expressions of J and K as show in Figure 6. And Equation 5 is the resulting expressions.

$$\begin{aligned} J &= w'x'z + wxz' + wz \\ K &= w'x'z + wxz' + w'x'y' \end{aligned} \tag{5}$$

And the circuit diagram of the jointly optimized solution is given in Figure 7. It can be seen that there are 4 NOT gates, 7 AND gates and 4 OR gates. There are 4 NOT gate inputs, 14 AND gate inputs, and 8 OR gate inputs.

Finally this jointly optimized solution (Figure 7 can be implemented using the 74HC04(NOT), 74HC08(AND), and 74HC32(OR) ICs. Pull down resistors (1k ohms works well) must be used on the switch inputs. The current through the LED outputs should be limited using a 270 ohm resistor. And if the LED outputs do not work try reversing their direction (remember they behave like diodes).

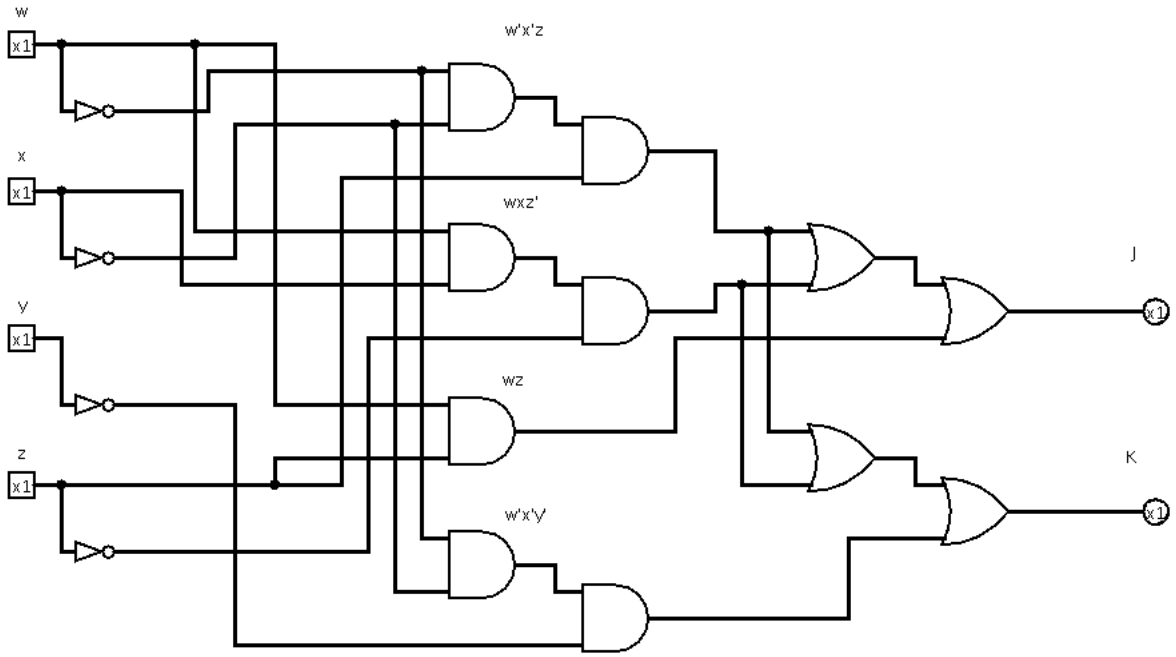

Figure 7: Circuit diagram of the jointly optimized solution of J and K when limited to two input gates.

3 Observations

The jointly optimized solution (Figure 7) of functions J and K reproduced the expected truth table values (Table 1).

The jointly optimized solution did reduce the number of gates albeit slightly. It can be seen from Table 2 that implementing J and K independently resulted in 16 gates and 27 inputs. Implementing these jointly resulted in 15 gates and 26 inputs, a savings of 1 gate and 1 input.

J by itself

gate type	# gates	# inputs
AND	2	4
OR	1	2
NOT	1	1
TOTAL	4	7

J and K independently

gate type	# gates	# inputs
AND	8	16
OR	3	6
NOT	5	5
TOTAL	16	27

K by itself, 2 input gates

gate type	# gates	# inputs
AND	6	12
OR	2	4
NOT	4	4
TOTAL	12	20

J and K jointly

gate type	# gates	# inputs
AND	7	14
OR	4	8
NOT	4	4
TOTAL	15	26

Table 2: Metrics of gate and input counts for various configurations of J and K.

4 Conclusion

The lab was a success in demonstrating that shared hardware can be used to implement separate expressions and still produce the desired outcome.