EECE 144
Fall 2011

Lab Report #5
Section 4
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1   Description/Objectives

The objective of this lab is to derive a simplified form of a canonical SOP equation using a Karnaugh Map and to implement it in hardware.

2   Procedure

The canonical SOP form of the equation used in this lab is given in Equation 1.

$$f(a, b, c) = \sum m(0, 2, 3, 4, 6) \tag{1}$$
$$= m_0 + m_2 + m_3 + m_4 + m_6$$
$$= a'b'c' + a'bc' + a'bc + ab'c' + abc'$$

The truth table produced from Equation 1 is shown in Figure 1. And the Karnaugh Map produced from the truth table is shown in Figure 2. Using the groupings produced by the Karnaugh Map in Figure 2 results in the simplified form in Equation 2. The implementation of the logic function using gates is shown in Figure 3.

$$f(a, b, c) = c' + a'b \qquad (2)$$

Index	a	b	c	f
0	0	0	0	1
1	0	0	1	0
2	0	1	0	1
3	0	1	1	1
4	1	0	0	1
5	1	0	1	0
6	1	1	0	1
7	1	1	1	0

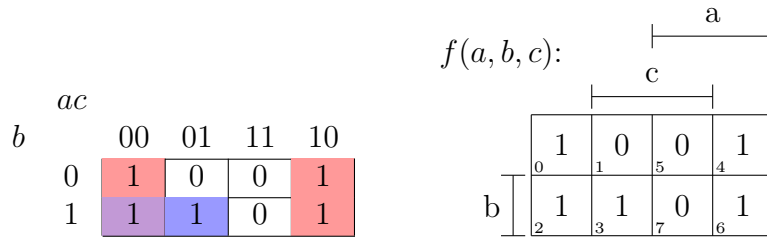Figure 1: Truth table of Equation 1.

Figure 2: Two equivalent Karnaugh Map representations of Equation 1. The first shows the explicit values of a, b, and c along with red and blue coloring to denote the groupings. The second is a Veitch [1] diagram.
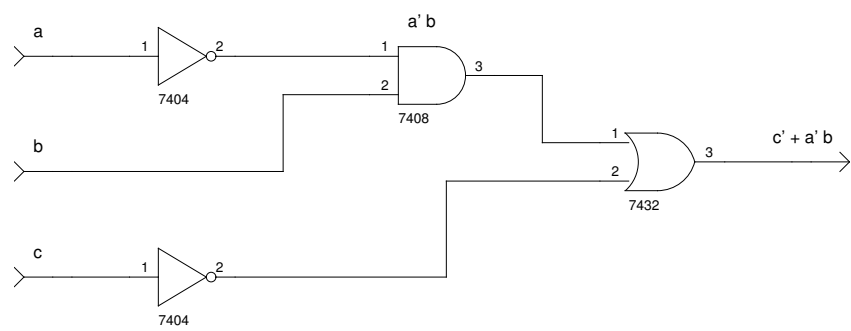
Figure 3: Circuit definition of equation 2.

3 Observations

The output of each logic function implemented in hardware (Figure 3) agreed with the expected values of the truth table (Figure 1).

4 Conclusion

This lab was a success in showing that simplification of a logic function using a Karnaugh map produces produces a equivalent function which can be implemented in hardware.

5 References

[1] E. W. Veitch, "A chart method for simplifying truth functions," in <u>Proceedings of the 1952 ACM national meeting (Pittsburgh)</u>, ACM '52, (New York, NY, USA), pp. 127–133, ACM, 1952.