EECE 144
Fall 2011

Lab Report #7
Section 4
10/19/2011

Submitted by: Marvanee Johnson

Signature	Printed Name	Date
	Jeremiah Mahler	**Oct 19, 2011**
	Marvanee Johnson	**Oct 19, 2011**

1 Description/Objectives

TODO: What is the objective of this lab? (Equation 1 and 2).

$$J(w,x,y,z) = \sum m(1,3,9,11,12,13,14,15) \tag{1}$$

$$K(w,x,y,z) = \sum m(0,1,3,12,14) \tag{2}$$

2 Procedure

TODO: Describe the procedure used to complete this lab. What analysis techniques are used (e.g. Karnaugh Maps). What was calculated?

(Table 1)

TODO: Describe how the minimal SOP expression for J was found. (Figure 1) (Equation 3).

$$J = wx + x'z \tag{3}$$

TODO: Describe how the minimal SOP expression for K was found. (Figure 2) (Equation 4).

$$K = w'x'y' + w'x'z + wxz' \tag{4}$$

Index	w	x	y	z	J	K
0	0	0	0	0	0	1
1	0	0	0	1	1	1
2	0	0	1	0	0	0
3	0	0	1	1	1	1
4	0	1	0	0	0	0
5	0	1	0	1	0	0
6	0	1	1	0	0	0
7	0	1	1	1	0	0
8	1	0	0	0	0	0
9	1	0	0	1	1	0
10	1	0	1	0	0	0
11	1	0	1	1	1	0
12	1	1	0	0	1	1
13	1	1	0	1	1	0
14	1	1	1	0	1	1
15	1	1	1	1	1	0

Table 1: Truth table of functions J and K.

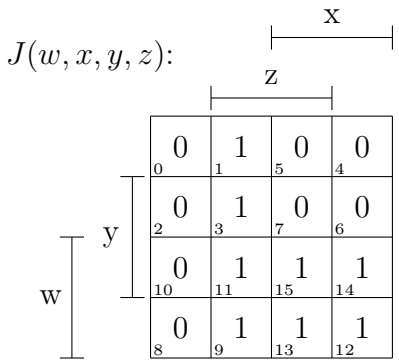

Figure 1: Karnaugh map of function J (Equation 1).

TODO: How are the number of gates and gate inputs determined? What are these counts for expression J? (Figure 3)

TODO: Similar to J, how is this done for K? (Figure 4)

TODO: What about the version K limited to 2 input gates? (Figure 5)

$K(w, x, y, z)$:

wy \ xz	00	01	11	10
00	1 (0)	1 (1)	0 (5)	0 (4)
01	0 (2)	1 (3)	0 (7)	0 (6)
11	0 (10)	0 (11)	0 (15)	1 (14)
10	0 (8)	0 (9)	0 (13)	1 (12)

Figure 2: Karnaugh map of function K (Equation 2).

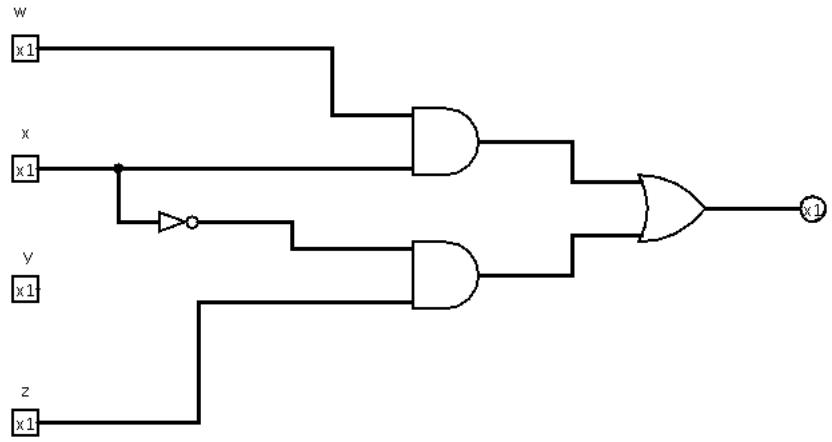

Figure 3: Circuit diagram of the minimal SOP solution of J.

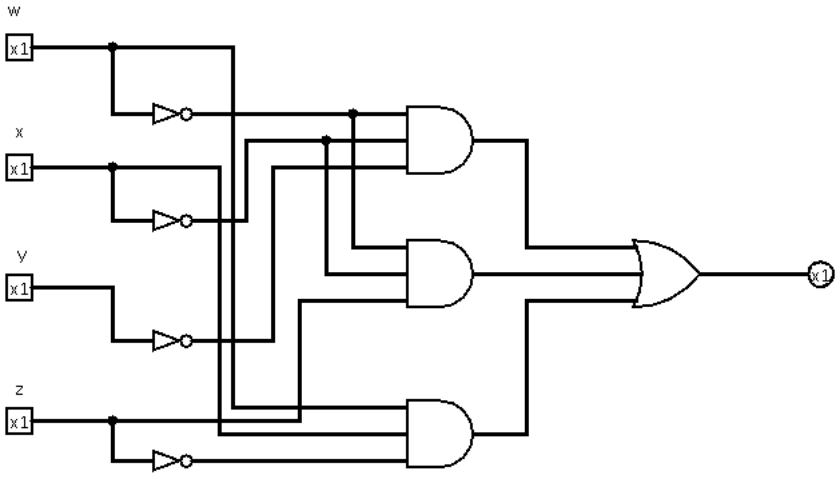

Figure 4: Circuit diagram of the minimal SOP solution of K.

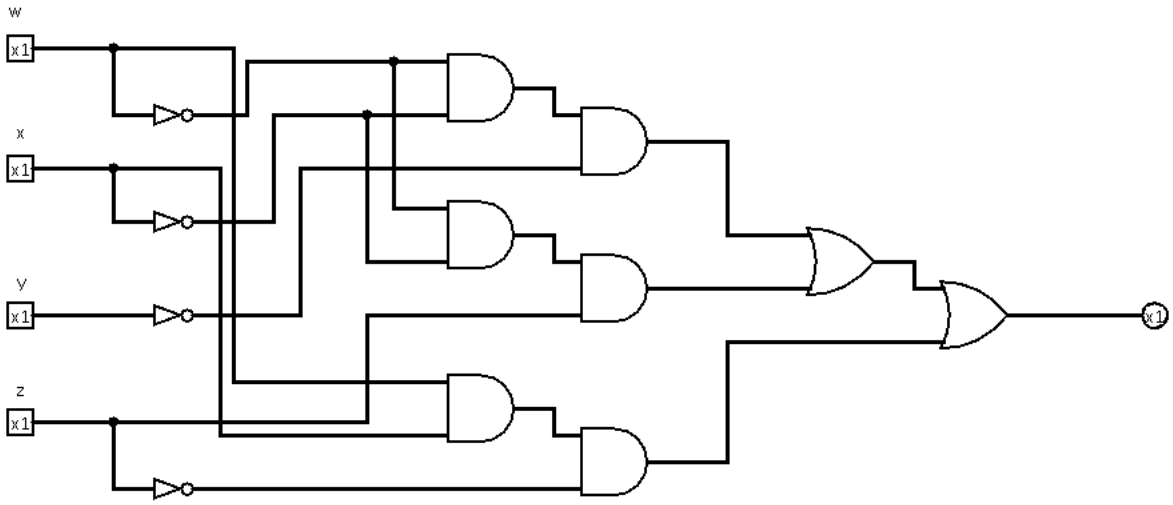

Figure 5: Circuit diagram of the minimal SOP solution of K when limited to two input gates.

TODO: What about for the jointly optimized solution of J and K? (Figure 6) (Equation 5)

$$
\begin{aligned}
J &= w'x'z + wxz' + wz \\
K &= w'x'z + wxz' + w'x'y'
\end{aligned} \tag{5}
$$

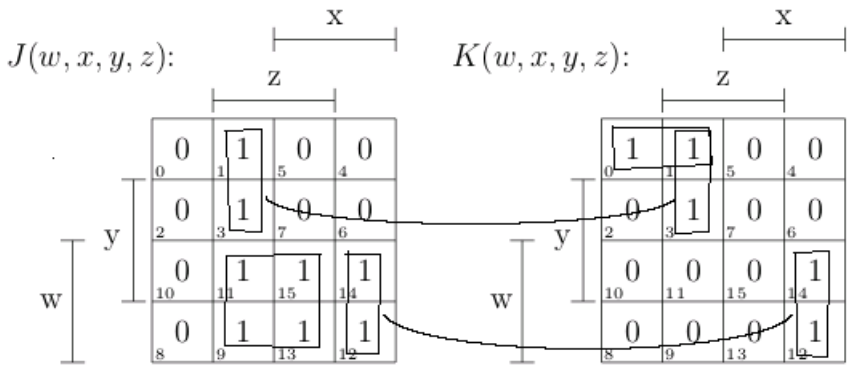

Figure 6: Jointly optimized Karnaugh maps for J and K.

TODO: How many gates, how many inputs for the joint solution? (Figure 7).

TODO: describe the hardware implementation. (Figure 7

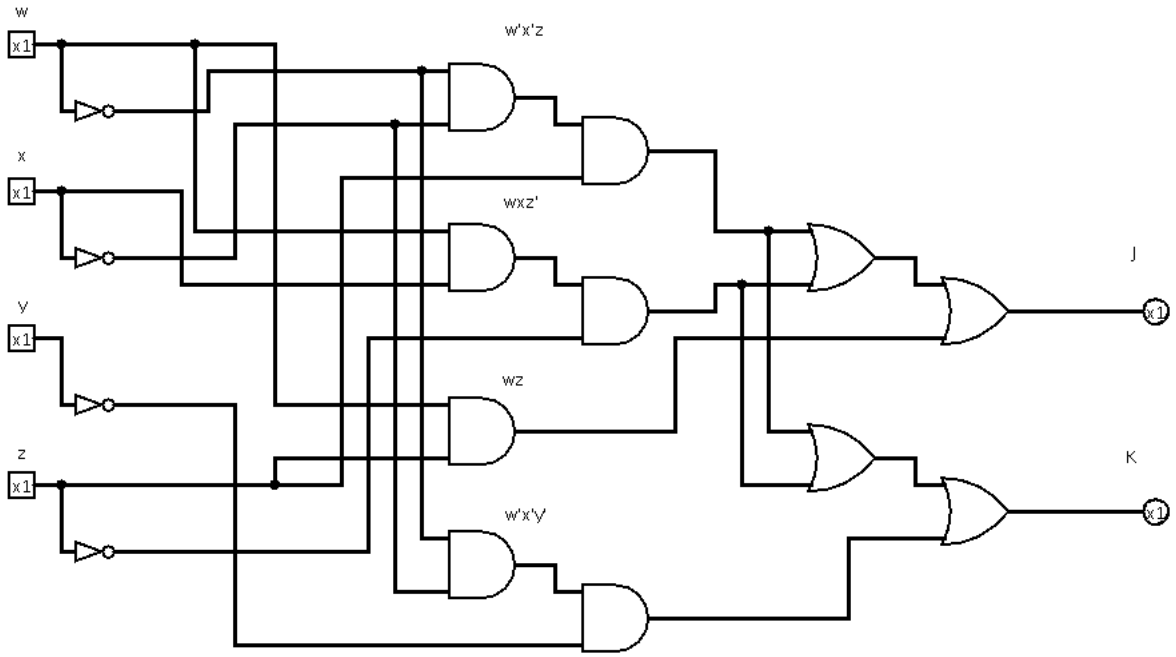

Figure 7: Circuit diagram of the jointly optimized solution of J and K when limited to two input gates.

3 Observations

TODO: How do the counts of various implementations compare? Does the resulting function match the truth table?

J by itself

gate type	# gates	# inputs
AND	2	4
OR	1	2
NOT	1	1
TOTAL	4	7

J and K independently

gate type	# gates	# inputs
AND	8	16
OR	3	6
NOT	5	5
TOTAL	16	27

K by itself, 2 input gates

gate type	# gates	# inputs
AND	6	12
OR	2	4
NOT	4	4
TOTAL	12	20

J and K jointly

gate type	# gates	# inputs
AND	7	14
OR	4	8
NOT	4	4
TOTAL	15	26

Table 2: Metrics of gate and input counts for various configurations of J and K.

4 Conclusion

TODO: Was this lab a success in achieving the objective?