EECE 144
Fall 2011

Lab Report #4
Section 4
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Submitted by:

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1 Description/Objectives

The objective of this lab is to derive the equivalent versions of a logic function in both the minterm canonical SOP form and the maxterm canonical POS form. And then implement both of these versions in hardware and verify their outputs.

2 Procedure

The minterm canonical SOP form for the logic function used in this experiment is given in Equation 1. The equivalent maxterm canonical POS form is given in Equation 2. Both functions produce an equivalent truth table as given in Figure 1.

$$\begin{aligned} f(x,y) &= \sum m(0,2) \\ &= m_0 + m_2 \\ &= x'y' + xy' \end{aligned} \tag{1}$$

$$
\begin{aligned}
f(x,y) &= \prod M(1,3) \\
&= M_1 M_3 \\
&= (x + y')(x' + y')
\end{aligned} \tag{2}
$$

x	y	$f(x,y)$
0	0	1
0	1	0
1	0	1
1	1	0

Figure 1: Truth table of the equivalent functions in Equation 1 and 2.

The design of these logic functions implemented with gates is shown in Figure 2 and 3. Interestingly, the only change made between the two diagrams is that of swapping the AND gates with OR gates and vice versa.

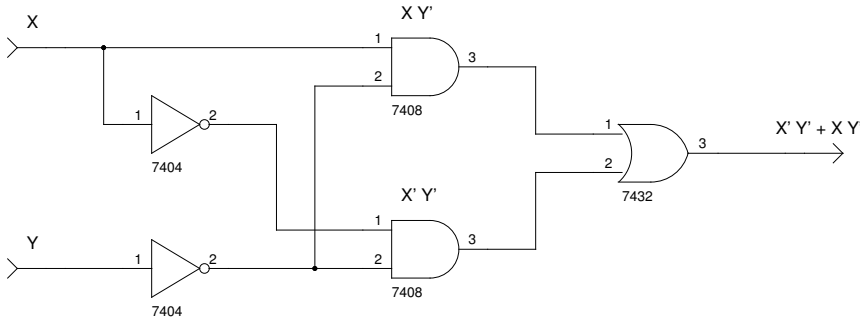

Figure 2: Diagram of equation 1; minterm canonical SOP form.

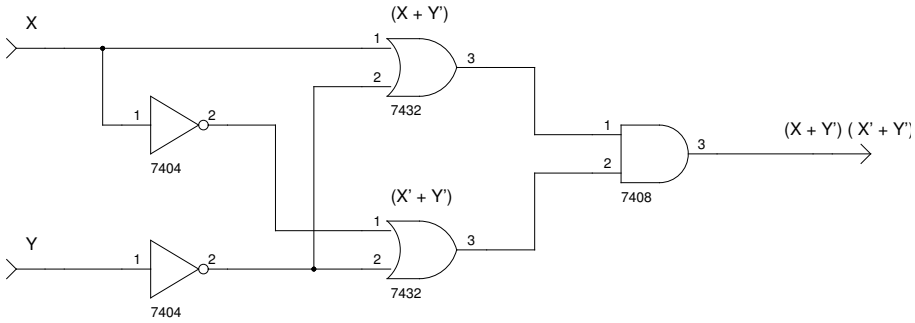

Figure 3: Diagram of equation 2; maxterm canonical POS form.

2.1 Wiring

The task of wiring the chips is tedious but it is nearly impossible without a plan (see Section 2).

To wire the chips it is necessary to have all the pertinent data sheets. These describe the function of each pin, the voltage characteristics and the orientation of the pins. The general procedure is as follows:

- Choose a subset of the circuit to implement from Figure **??**.
- Refer to the data sheet for the pin identification of the chip involved.
- Connect wires.
- Repeat until all subsets of the circuit have been implemented.

As an example, the diagram (Figure 2) showed that each pin was connected to the NOT gates first. So the first step was to connect each of the switches which represented the inputs x and y to the corresponding pins on the 7404 NOT gate chip.

The final output should be connected to an LED along with a resistor that limits the current to no more than 20 mA. Be sure to use pull down resistors on the mechanical switch inputs to guarantee a near 0 volt logic low. A 1k pull down resistor works correctly in most cases.

3 Observations

The output of each logic function implemented in hardware agreed with the truth table. To switch between the minterm POS to maxterm SOP it was only necessary to swap the 7432 OR gate with the 7408 AND gate. This is possible because the layouts are identical for each chip.

4 Conclusion

This lab was a success in showing the equivalence of minterm SOP form and maxterm POS form by implementing the function in hardware.

5 References

[1] C. Roth Jr., Fundamentals of Logic Design. Cengage Learning, 2009.