EECE 144
Fall 2011

Lab Report #7
Section 4
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1 Description/Objectives

The purpose of this lab is to find the min SOP expressions of equations J & K using a minimal amount of gates and to build a circut combining the two equations using only two input gates. (Equation 1 and 2).

$$J(w,x,y,z) = \sum m(1,3,9,11,12,13,14,15) \tag{1}$$

$$K(w,x,y,z) = \sum m(0,1,3,12,14) \tag{2}$$

2 Procedure

The first step in accomplishing this task was to create seperate Karnaugh Map for expressions J & K in order to find the min SOPs of the equations and to determin the number of gates needed to implement each equation seperately. The next step was to jointly optimaize the two equations through the use Karnaugh Maps to produce a circut using the minimum number of gates. Lastly, we used the Truth table in order to test and verify the funtionality of the curcuit. (Table 1) The minimal SOP expression for J was found by the use of a Karnaugh Map. (Figure 1) (Equation 3).

$$J = wx + x'z \tag{3}$$

The minimal SOP expression for K was found by the use of a Karnaugh Map. (Figure 2) (Equation 4).

$$K = w'x'y' + w'x'z + wxz' \tag{4}$$

Firgure 1 shows the Karnaugh map used for equation J in order to determine the number of gates and gate inputs needed A total of 4 gates would be need to implement expression

Index	w	x	y	z	J	K
0	0	0	0	0	0	1
1	0	0	0	1	1	1
2	0	0	1	0	0	0
3	0	0	1	1	1	1
4	0	1	0	0	0	0
5	0	1	0	1	0	0
6	0	1	1	0	0	0
7	0	1	1	1	0	0
8	1	0	0	0	0	0
9	1	0	0	1	1	0
10	1	0	1	0	0	0
11	1	0	1	1	1	0
12	1	1	0	0	1	1
13	1	1	0	1	1	0
14	1	1	1	0	1	1
15	1	1	1	1	1	0

Table 1: Truth table of functions J and K.

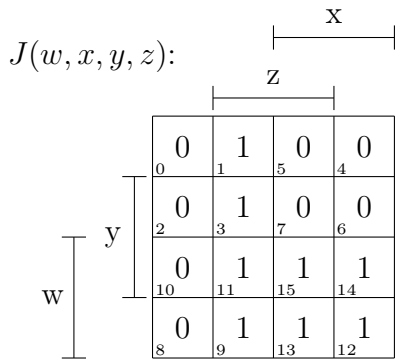

Figure 1: Karnaugh map of function J (Equation 1).

J? (Figure 3) Firgure 4 shows the Karnaugh map used for equation K in order to determine the number of gates and gate inputs needed A total of 8 gates would be need to implement expression J? (Figure 4) TODO: What about the version K limited to 2 input gates? (Figure 5)

$K(w, x, y, z)$:

wy \ xz	00	01	11	10
00	1 (0)	1 (1)	0 (5)	0 (4)
01	0 (2)	1 (3)	0 (7)	0 (6)
11	0 (10)	0 (11)	0 (15)	1 (14)
10	0 (8)	0 (9)	0 (13)	1 (12)

Figure 2: Karnaugh map of function K (Equation 2).

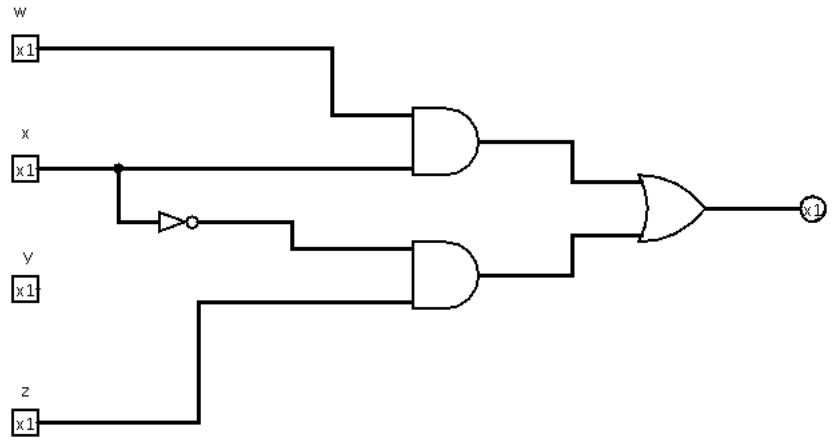

Figure 3: Circuit diagram of the minimal SOP solution of J.

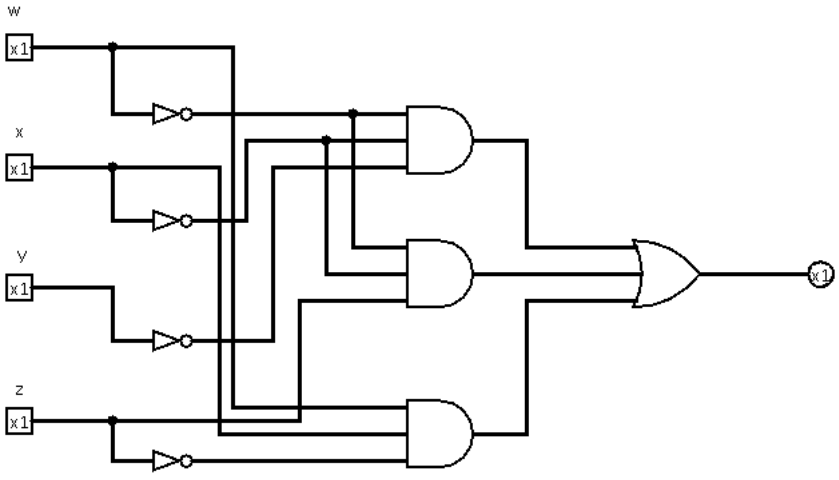

Figure 4: Circuit diagram of the minimal SOP solution of K.

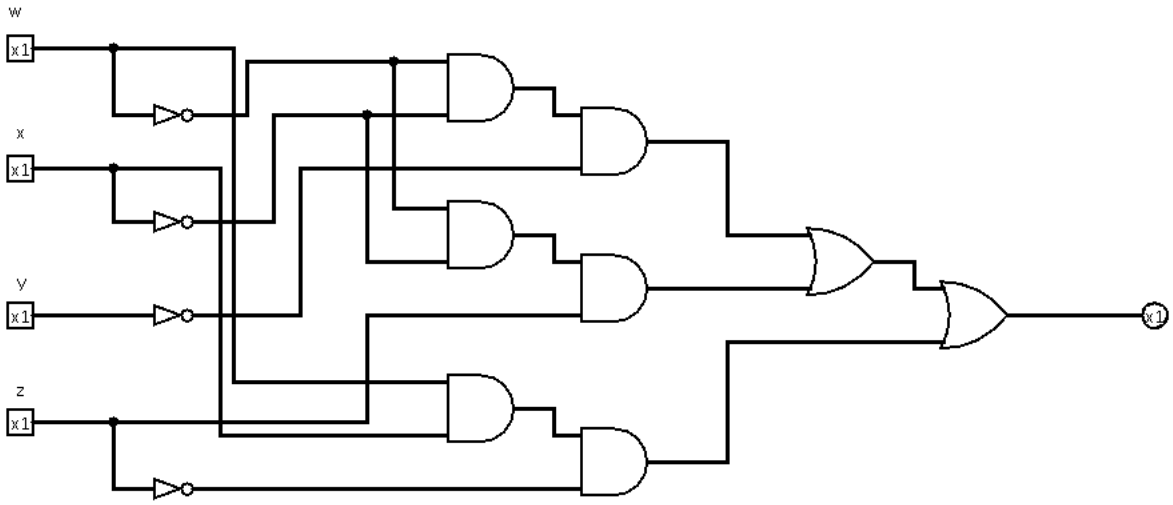

Figure 5: Circuit diagram of the minimal SOP solution of K when limited to two input gates.

A jointly optimized solution of J and K is created by combining shared term used by both SOP espressions of J and K. (Figure 6) (Equation 5)

$$\begin{aligned} J &= w'x'z + wxz' + wz \\ K &= w'x'z + wxz' + w'x'y' \end{aligned} \tag{5}$$

15 gates, and 7 inputs is the result of J and K joint solution (Figure 7). 4 NOT gates, 7

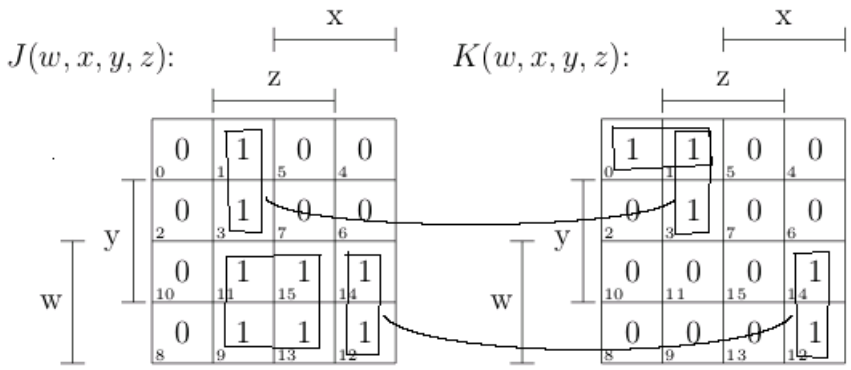

Figure 6: Jointly optimized Karnaugh maps for J and K.

AND gates and 4 OR gates where used to implement the J and K combined circuit. (Figure 7

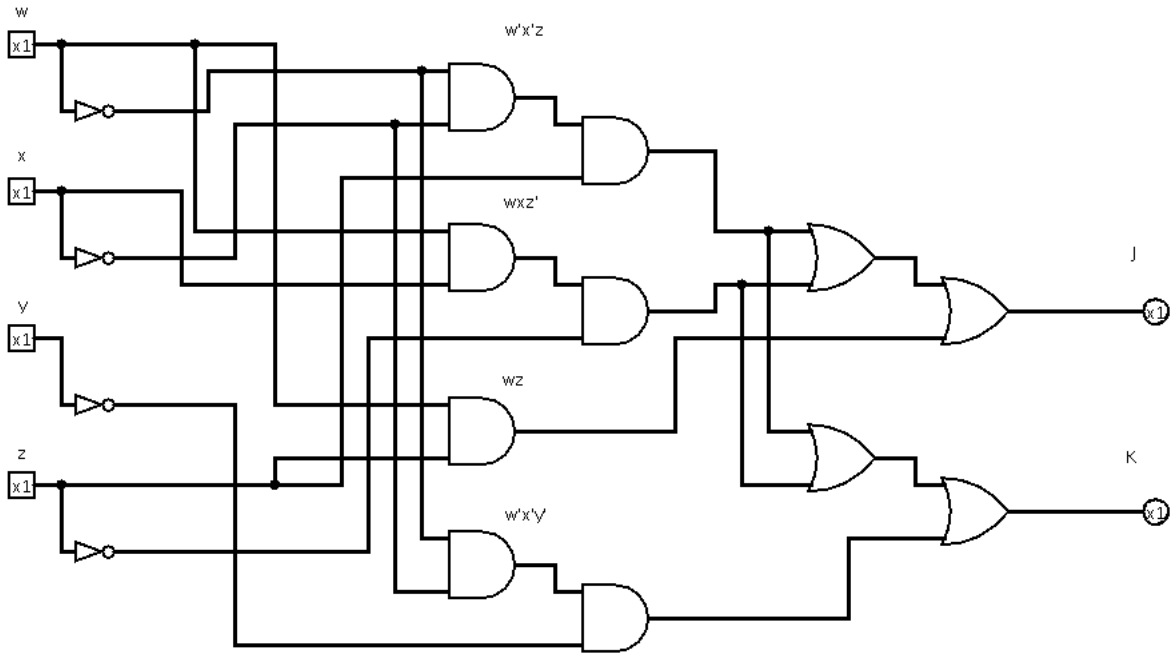

Figure 7: Circuit diagram of the jointly optimized solution of J and K when limited to two input gates.

3 Observations

The results of the implemented circuit in Figure 7 lines up with the Truth Table and produces the expected results.

J by itself

gate type	# gates	# inputs
AND	2	4
OR	1	2
NOT	1	1
TOTAL	4	7

J and K independently

gate type	# gates	# inputs
AND	8	16
OR	3	6
NOT	5	5
TOTAL	16	27

K by itself, 2 input gates

gate type	# gates	# inputs
AND	6	12
OR	2	4
NOT	4	4
TOTAL	12	20

J and K jointly

gate type	# gates	# inputs
AND	7	14
OR	4	8
NOT	4	4
TOTAL	15	26

Table 2: Metrics of gate and input counts for various configurations of J and K.

4 Conclusion

The lab was a success in demonstrating that shared hardware can be used to implement seperate expressions and still produce the desired outcome.