EECE 144
Fall 2011

Lab Report #11
Section 4
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1 Description/Objectives

The objective of this lab is to design a three bit binary counter that iterates over the following non-sequential sequence in ascending order from top to bottom when $X = 0$ and in descending order when $X = 1$. The design must use one JK, one T, and one D flip-flop.

$$\begin{array}{ccc} 0 & 0 & 0 \\ 0 & 1 & 0 \\ 1 & 1 & 0 \\ 0 & 1 & 1 \\ 1 & 0 & 1 \\ 0 & 0 & 1 \\ 1 & 0 & 0 \\ 1 & 1 & 1 \end{array}$$

2 Procedure

To implement this counter one flip flop is used for each bit. Any type of flip flop can be used for any bit but in this specific implementation we will use a JK flip-flop for the most significant bit followed by a T and a D.

The first step is to build a state table which describes all the required counter states along with the flip-flop inputs necessary to produce the desired outputs as shown in Table 1. From this table the mapping from the inputs (Q_2, Q_1, Q_0) to gate inputs (J_2, K_2, T_1, D_0) can be determined.

n	X	Q_2	Q_1	Q_0	Q_2^+	Q_1^+	Q_0^+	J_2	K_2	T_1	D_0
0	0	0	0	0	0	1	0	0	x	1	0
1	0	0	0	1	1	0	0	1	x	0	0
2	0	0	1	0	1	1	0	1	x	0	0
3	0	0	1	1	1	0	1	1	x	1	1
4	0	1	0	0	1	1	1	x	0	1	1
5	0	1	0	1	0	0	1	x	1	0	1
6	0	1	1	0	0	1	1	x	1	0	1
7	0	1	1	1	0	0	0	x	1	1	0
8	1	0	0	0	1	1	1	1	x	1	1
9	1	0	0	1	1	0	1	1	x	0	1
10	1	0	1	0	0	0	0	0	x	1	0
11	1	0	1	1	1	1	0	1	x	0	0
12	1	1	0	0	0	0	1	x	1	0	1
13	1	1	0	1	0	1	1	x	1	1	1
14	1	1	1	0	0	1	0	x	1	0	0
15	1	1	1	1	1	0	0	x	0	1	0

Table 1: State table for the 3-bit counter using a JK, T and D flip-flop in order with the JK as the most significant bit. The "don't care" values are denoted by an x.

2.1 bit Q_2 using JK flip-flop

The Karnaugh Maps for bit Q_2 are shown in Figure 1. From this table it can be seen that J_2 and K_2 are disjoint so they can be merged in to a single function that represents them both. This results in the SOP equation shown below.

$$J_2/K_2 = X'Q_1 + X'Q_0 + Q_2Q_1Q_0' + Q_2'Q_0 + XQ_1'$$

2.2 bit Q_1 using T flip-flop

The Karnaugh Map for bit Q_1 is shown in Figure 2. This results in the SOP equation shown below.

$$T_1 = X'Q_1'Q_0' + X'Q_1Q_0 + XQ_2Q_0 + XQ_2'Q_0'$$

2.3 bit Q_0 using D flip-flop

The Karnaugh Map for bit Q_0 is shown in Figure 3. This results in the SOP equation shown below.

$$D_0 = Q_2Q_1' + X'Q_2Q_0' + XQ_1' + X'Q_2'Q_1Q_0$$

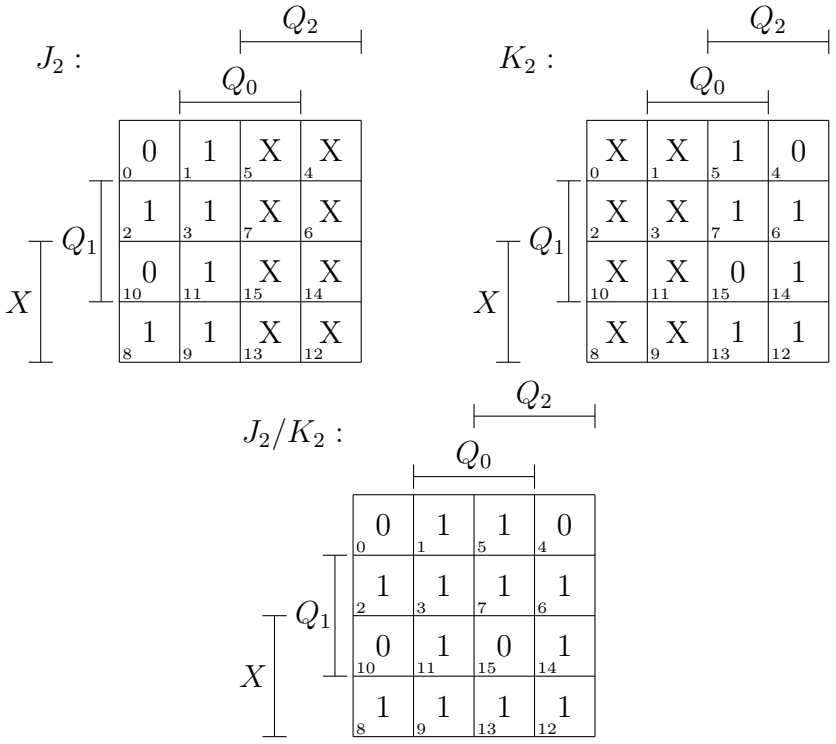

Figure 1: Karnaugh Maps for bit Q_2 used to describe the mapping from the inputs (Q_2, Q_1, Q_2, X) to the input of the JK flip-flop (J_2, K_2). In this case J_2 and K_2 are disjoint so they can be merged in to a single table (J_2/K_2).

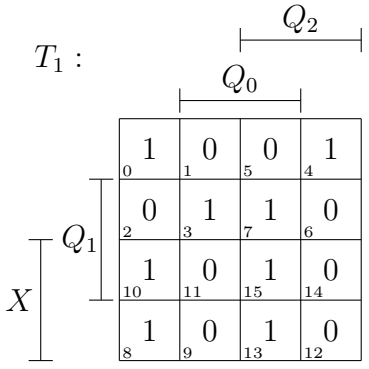

Figure 2: Karnaugh Map for bit Q_1 used to describe the mapping from the inputs (Q_2, Q_1, Q_2, X) to the input of the T flip-flop T_1.

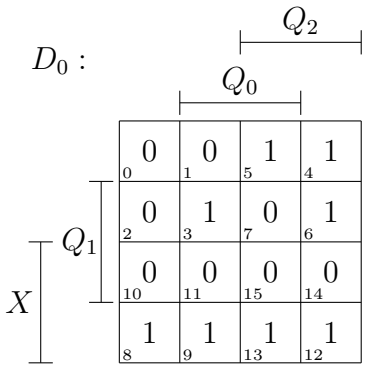

Figure 3: Karnaugh Map for bit Q_0 used to describe the mapping from the inputs (Q_2, Q_1, Q_2, X) to the input of the D flip-flop D_0.

2.4 circuit construction

After all the equations for each bit has been found these can be combined together to produce a complete solution that works for all bits and implements the 3-bit, non-sequential counter. In this case Logisim[1] will be used to build and simulate the circuit.

This implementation has many interconnections so its construction can be quite tedious. The resulting circuit is shown in Figure 4. Every single combination should be verified against the state table (Table 1) to ensure every connection is right.

In the event of an error it is best to methodically diagnose the error rather than removing all or some and starting over. Starting over does nothing to find the problem and it is possible that the problem could be built again if the design is wrong. A good strategy for finding problems is to try and isolate the problem. For example, if the bit Q_2 is wrong it would make sense to check the JK flip-flop since that is the bit it controls.

3 Observations

The counter, when simulated in Logisim, reproduced the desired sequence in both the up and down directions.

Due to the tedious nature of this design several errors did occur while building the circuit which had to be fixed. The strategy of trying to isolate the problem to a specific bit or part of the circuit worked well.

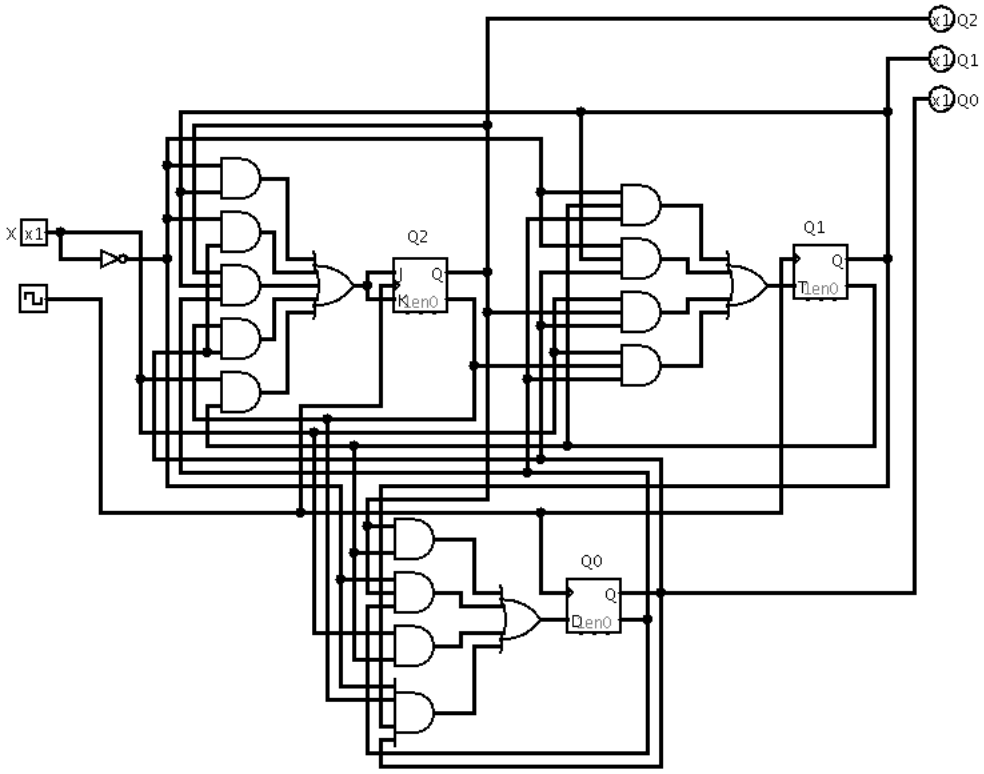

Figure 4: Circuit diagram of 3 bit-counter.

The complexity of this design suggests that there may be a simpler solution. One possible avenue for optimization is the input gates to the flip-flops. Perhaps these can be aggregated together to use fewer gates. Another possibility is to try different gate types in different positions. Perhaps a JK would require fewer gates as bit 1 instead of bit 2 for example.

4 Conclusion

This lab was a success in designing and implementing a three bit non-sequential up/down counter in Logisim using three flip-flops of different types. It is indeed possible to build a counter with three different types of flip-flops along with several additional gates.

5 References

[1] Logisim, "Logisim, a graphical tool for designing and simulating logic circuits." `http://ozark.hendrix.edu/~burch/logisim/`, 2011.