EECE 144
Fall 2011

Lab Report #8
Section 4
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1 Description/Objectives

The objective of this lab is to design circuit to implement Equation 1 using only a 3 to 8 line inverting decoder ('138) and a 8 input multiplexer ('251) [1]. .

$$\begin{aligned} F(a,b,c,d) &= \prod M(2,5,8,15) \\ &= M(2)M(5)M(8)M(15) \\ &= (a'+b'+c+d')(a'+b+c'+d)(a+b'+c'+d')(a+b+c+d) \end{aligned} \tag{1}$$

2 Procedure

The truth table for the functions is given in Table 1. Here we are constructing a POS solution so we will only focus on those rows with zeros (2, 5, 8, 15). Any non-zero combination will become a 1.

This lab can be nearly impossible without a conceptual idea of how to solve it. The circuit to be designed should be considered a "black box" with 4 inputs and 1 output (Figure 1). These inputs will connect to at least one of the select inputs on either the decoder or the multiplexer. Since there are 4 inputs and 6 select bits between the chips there will be unused pins. These must be set to either high or low.

Once a combination of the outer connections to select bits has been chosen the next step is to find the connections between the output bits of the decoder to the input bits of the multiplexer.

[1] Any family of chips can be used, such as TTL (74HC) or CMOS (74LS), but the chips from different families must not be interchanged or else damage may result.

Index	a	b	c	d	F
0	0	0	0	0	1
1	0	0	0	1	1
2	0	0	1	0	0
3	0	0	1	1	1
4	0	1	0	0	1
5	0	1	0	1	0
6	0	1	1	0	1
7	0	1	1	1	1
8	1	0	0	0	0
9	1	0	0	1	1
10	1	0	1	0	1
11	1	0	1	1	1
12	1	1	0	0	1
13	1	1	0	1	1
14	1	1	1	0	1
15	1	1	1	1	0

Table 1: Truth table of F (Equation 1

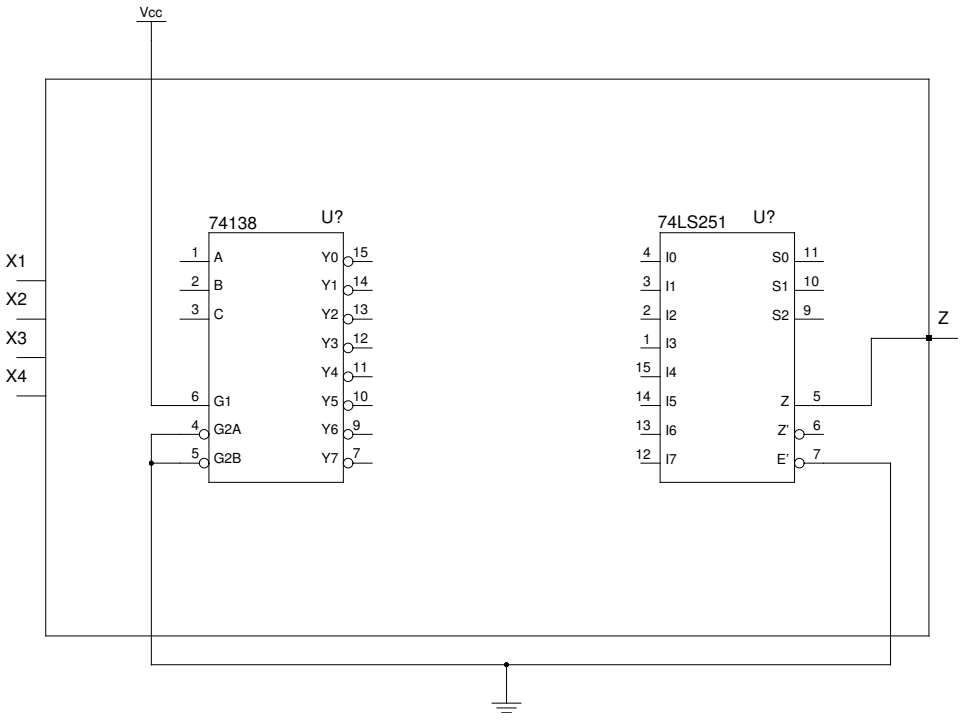


Figure 1: Conceptual design without any interconnections. Both chips are enabled. See Appendix A for a printer friendly version of this page which can be used to solve combinations.

id	A	B	C	$S0$	$S1$	$S2$	valid?
0	$X1$	$X2$	$X3$	$X4$	0	0	no
1	$X1$	$X2$	$X3$	$X4$	0	1	no
2	$X1$	$X2$	$X3$	$X4$	1	0	no
3	$X1$	$X2$	$X3$	$X4$	1	1	no
4	$X1$	$X2$	$X3$	0	$X4$	0	no
5	$X1$	$X2$	$X3$	0	$X4$	1	no
6	$X1$	$X2$	$X3$	1	$X4$	0	no
7	$X1$	$X2$	$X3$	1	$X4$	1	no
8	$X1$	$X2$	$X3$	0	0	$X4$	no
9	$X1$	$X2$	$X3$	0	1	$X4$	no
10	$X1$	$X2$	$X3$	1	1	$X4$	no
11	$X1$	$X2$	$X3$	1	0	$X4$	no
12	$X1$	$X2$	0	$X3$	$X4$	0	no
13	$X1$	$X2$	0	$X3$	$X4$	1	yes
14	$X1$	$X2$	1	$X3$	$X4$	0	unknown
15	$X1$	$X2$	1	$X3$	$X4$	1	unknown
16	$X1$	$X2$	0	$X3$	0	$X4$	no
17	$X1$	$X2$	0	$X3$	1	$X4$	yes
18	$X1$	$X2$	1	$X3$	0	$X4$	unknown
19	$X1$	$X2$	1	$X3$	1	$X4$	unknown
20	$X1$	$X2$	0	0	$X3$	$X4$	unknown
21	$X1$	$X2$	0	1	$X3$	$X4$	unknown
22	$X1$	$X2$	1	0	$X3$	$X4$	unknown
23	$X1$	$X2$	1	1	$X3$	$X4$	unknown
24	...						

Table 2: A few of the possible combinations of outermost connections. Refer to Figure 1 for the terminal designations. This sample only has ordered combinations but they could be out of order as well (e.g. $X3$ could be before $X0$).

To determine one connection, apply one of the maxterms to the outermost inputs. Then make a connection from the decoder to the multiplexer such that the final output will be zero (POS). If the connection would join together two outputs of the decoder this is an invalid combination [2]. It is also possible that two inputs could be joined together. Even though this would not damage the chip it is still an invalid combination. To try a different combination the outermost pins must be reconfigured and the process repeated. See Table 2 for a listing of a few combinations. The worksheet in Appendix A can be used to try out the combinations.

One solved combination is shown in Figure 2.

[2]The outputs of ICs are not designed to be connected together and doing so will most likely destroy it.

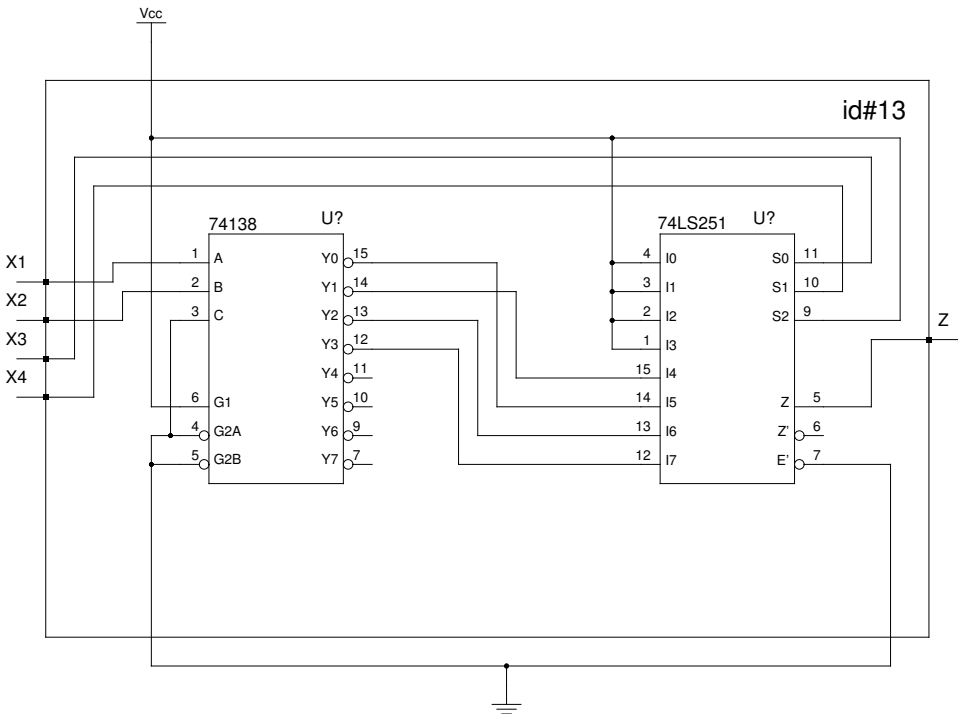


Figure 2: Solved circuit using combination with id#13 (Table 2).

There are several caveats to avoid when implementing this with ICs. The encoder has three enable pins where two are inverted. All these pins must be activated: the inverted pins should be connected to ground and the other to Vcc. The multiplexer also has an inverted enable pin that must be connected to ground. Unused inputs to the multiplexer should be connected to Vcc.

3 Observations

There is potentially a huge number of possible combinations which may or may not work (Table 2). Only the first 20 or so combinations were examined but it would be interesting to determine the number of possible combinations as well as the number of valid combinations.

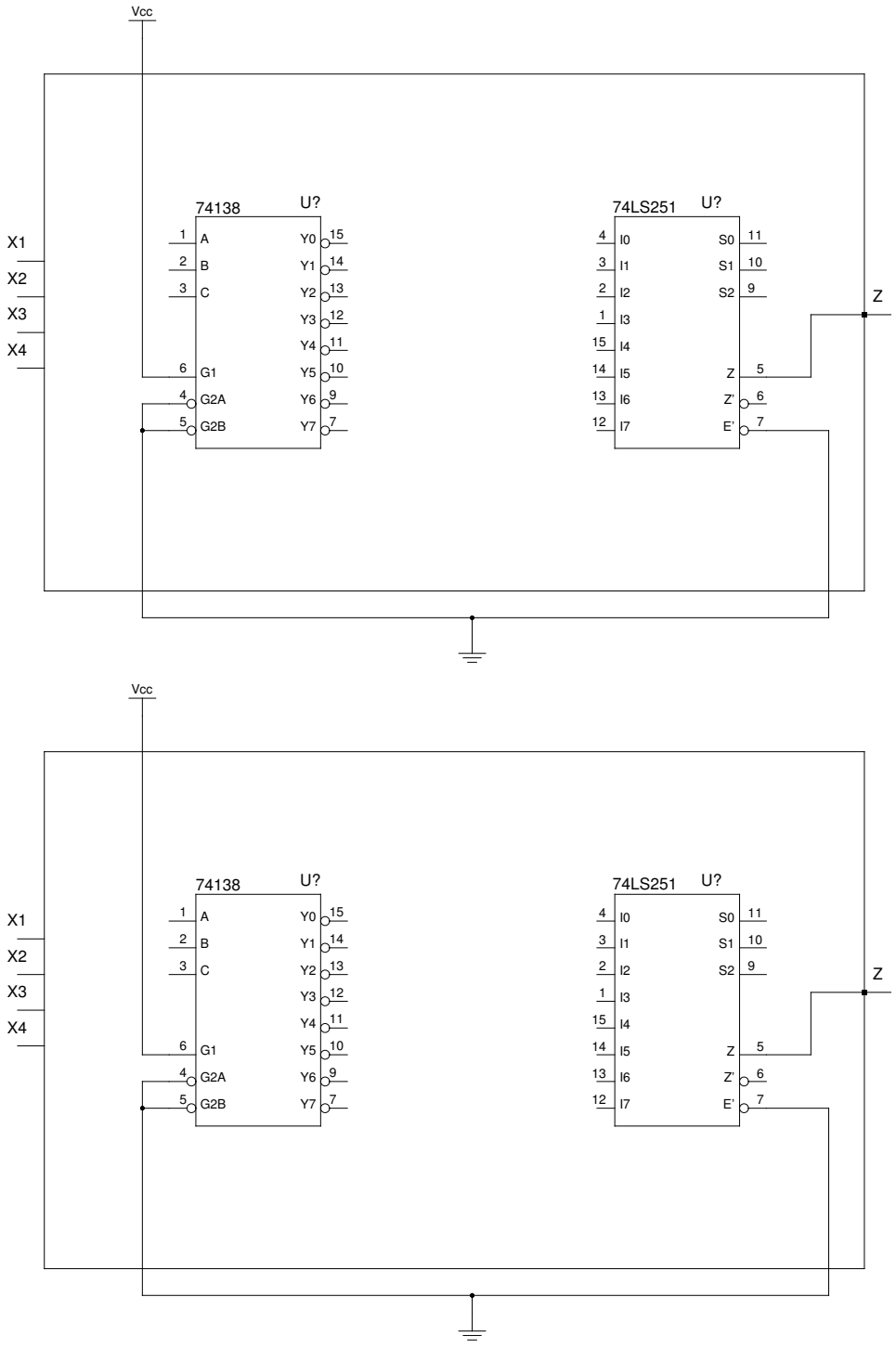
A working combination was found (Figure 2) and when built using ICs it did reproduce the truth table (Table 1) of the function (Equation 1).

4 Conclusion

With only a limited knowledge of decoders and multiplexers and without a conceptual idea of how to design the circuit this lab was nearly impossible. But it was shown that is possible to build a POS equation using a decoder and a multiplexer that would be impossible to implement with either of them individually.

A Circuit Combination Worksheet

Print this page out and use it to test the various connection combinations.



Vcc
74138
U?
A
B
C
G1
G2A
G2B
Y0
Y1
Y2
Y3
Y4
Y5
Y6
Y7
74LS251
U?
I0
I1
I2
I3
I4
I5
I6
I7
S0
S1
S2
Z
Z'
E'
X1
X2
X3
X4
Z