EECE 144
Fall 2011

Lab Report #7
Section 4
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Submitted by: Jeremiah Mahler

Signature	Printed Name	Date
	Jeremiah Mahler	**Oct 19, 2011**
	Marvanee Johnson	**Oct 19, 2011**

1 Description/Objectives

The objective of this lab is to develop an optimized hardware implementation of two distinct logic functions (Equation 1 and 2). First the logic functions will be analyzed/optimized individually. Then they will be combined in to a jointly optimized solution. The jointly optimized solution will then be implemented in hardware using 74HC04(NOT), 74HC08(AND), and 74HC32(OR) gates.

Once completed it should be possible to confirm that the jointly optimized solution behaves identically to the singly optimized solution.

$$J(w,x,y,z) = \sum m(1,3,9,11,12,13,14,15) \tag{1}$$

$$K(w,x,y,z) = \sum m(0,1,3,12,14) \tag{2}$$

2 Procedure

The procedure consists of several steps:

1. Find the minimal SOP expression of J and K separately using Karnaugh maps.
2. Calculate the number of gates and number of gate inputs required to implement these functions using gates with any number of inputs.
3. Calculate the number of gates and number of gate inputs required to implement these functions using only two input gates.
4. Find a jointly optimized solution of J and K which minimizes the number of gates using Karnaugh maps.
5. Calculate the number of gates and number of gate inputs required to implement this function using only two input gates.
6. Implement the jointly optimized function in hardware and verify it against a truth table of the original functions (Table 1).

Index	w	x	y	z	J	K
0	0	0	0	0	0	1
1	0	0	0	1	1	1
2	0	0	1	0	0	0
3	0	0	1	1	1	1
4	0	1	0	0	0	0
5	0	1	0	1	0	0
6	0	1	1	0	0	0
7	0	1	1	1	0	0
8	1	0	0	0	0	0
9	1	0	0	1	1	0
10	1	0	1	0	0	0
11	1	0	1	1	1	0
12	1	1	0	0	1	1
13	1	1	0	1	1	0
14	1	1	1	0	1	1
15	1	1	1	1	1	0

Table 1: Truth table of functions J and K.

The first step is to find a minimal SOP expression for J. Using the Karnaugh map for J (Figure 1) results in two prime implicants as shown in Equation 3.

$$J = wx + x'z \tag{3}$$

Similarly, finding a minimal SOP expression for K using its Karnaugh map (Figure 2) results in three prime implicants as shown in Equation 4.

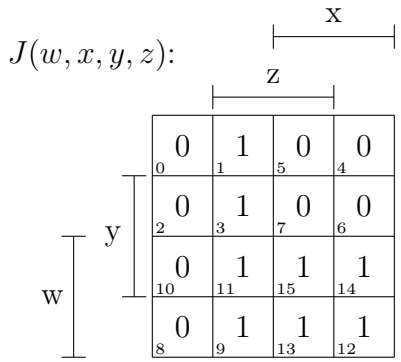

Figure 1: Karnaugh map of function J (Equation 1).

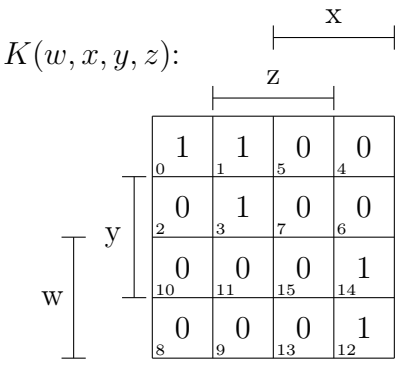

Figure 2: Karnaugh map of function K (Equation 2).

$$K = w'x'y' + w'x'z + wxz' \tag{4}$$

A gifted mind of electronics can probably deduce the number of gates and gate inputs from the expressions alone. But here we appeal to the not so brilliant of us by using circuit diagrams to clearly elucidate the metrics we are seeking.

Referring to the circuit for J in Figure 3 we can see that there are 2 AND gates, 1 OR gate, and 1 NOT gate. And there are 4 inputs to the AND gates, 2 inputs to the OR gate, and 1 input to the NOT gate.

Referring to the circuit for K in Figure 4 we can see that there are 3 AND gates, 1 OR gate and 4 NOT gates. And there are 9 inputs to the AND gates, 3 inputs to the OR gate, and 4 inputs to the NOT gates.

When limited to two gates the previous solution for J is the same. For K the circuit must be modified as shown in Figure 5. There are 4 NOT gates, 6 AND gates and 2 OR gates. And there are 4 inputs to the NOT gates, 12 inputs to the AND gates, and 4 inputs to the OR gates.

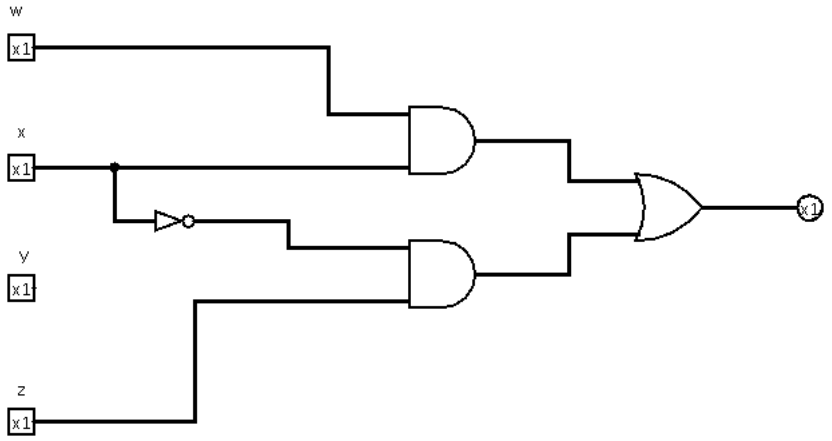

Figure 3: Circuit diagram of the minimal SOP solution of J.

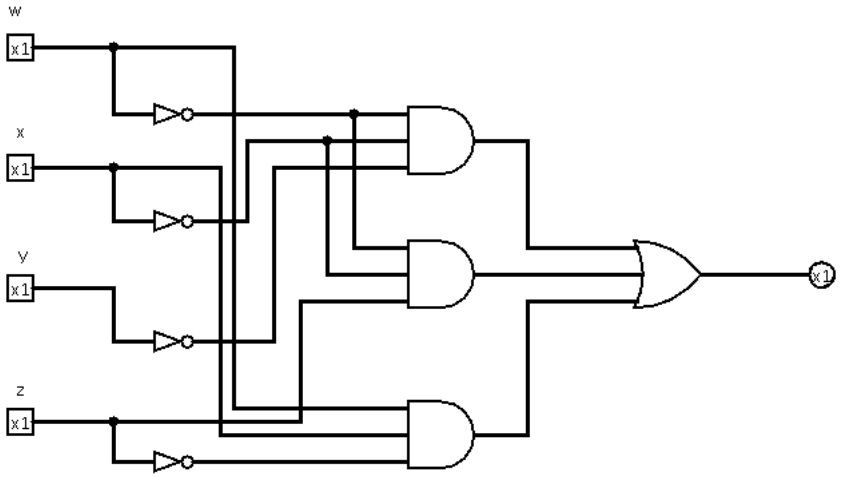

Figure 4: Circuit diagram of the minimal SOP solution of K.

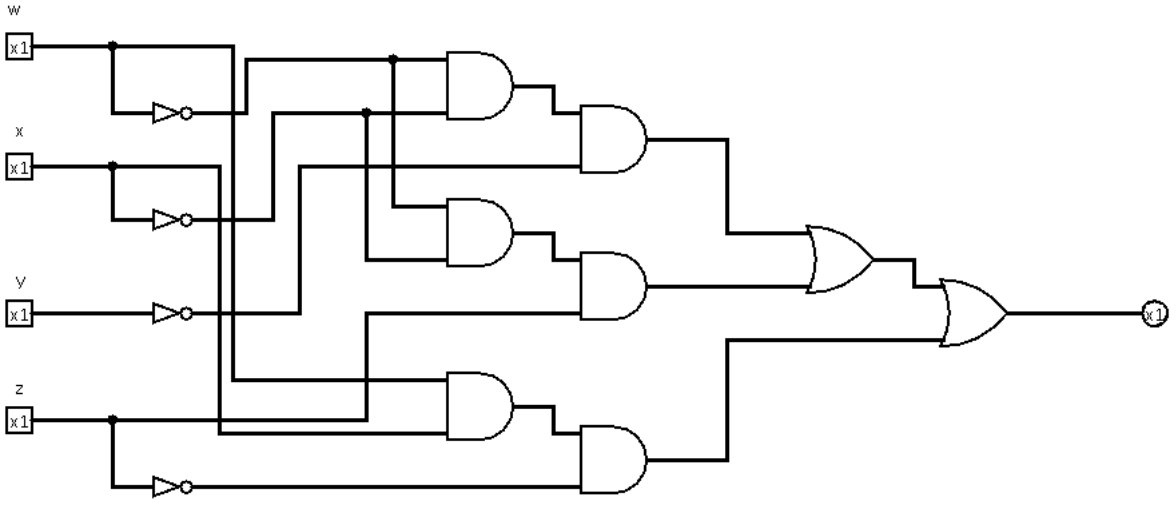

Figure 5: Circuit diagram of the minimal SOP solution of K when limited to two input gates.

Jointly optimizing both J and K together is somewhat more complex than either individually. The general strategy is to find essential prime implicants and then to find implicants which are common to both functions.

Figure 6 shows the implicants in a Karnaugh map of a jointly optimized solution. And Equation 5 is the resulting expressions.

$$\begin{aligned} J &= w'x'z + wxz' + wz \\ K &= w'x'z + wxz' + w'x'y' \end{aligned} \tag{5}$$

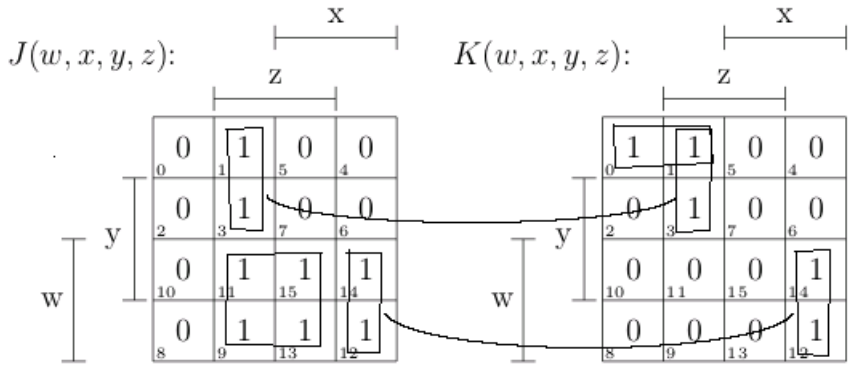

Figure 6: Jointly optimized Karnaugh maps for J and K.

And the circuit diagram of the jointly optimized solution is given in Figure 7. It can be seen that there are 4 NOT gates, 7 AND gates and 4 OR gates. There are 4 NOT gate inputs, 14 AND gate inputs, and 8 OR gate inputs.

Finally this jointly optimized solution (Figure 7 can be implemented in hardware using the 74HC04(NOT), 74HC08(AND), and 74HC32(OR) gates. Be sure to use pull down resistors (1k ohms works well) on the switch inputs and to limit the current through the LED outputs with a 290 ohm resistor. And if the LED outputs do not work try reversing their direction (remember they behave like diodes).

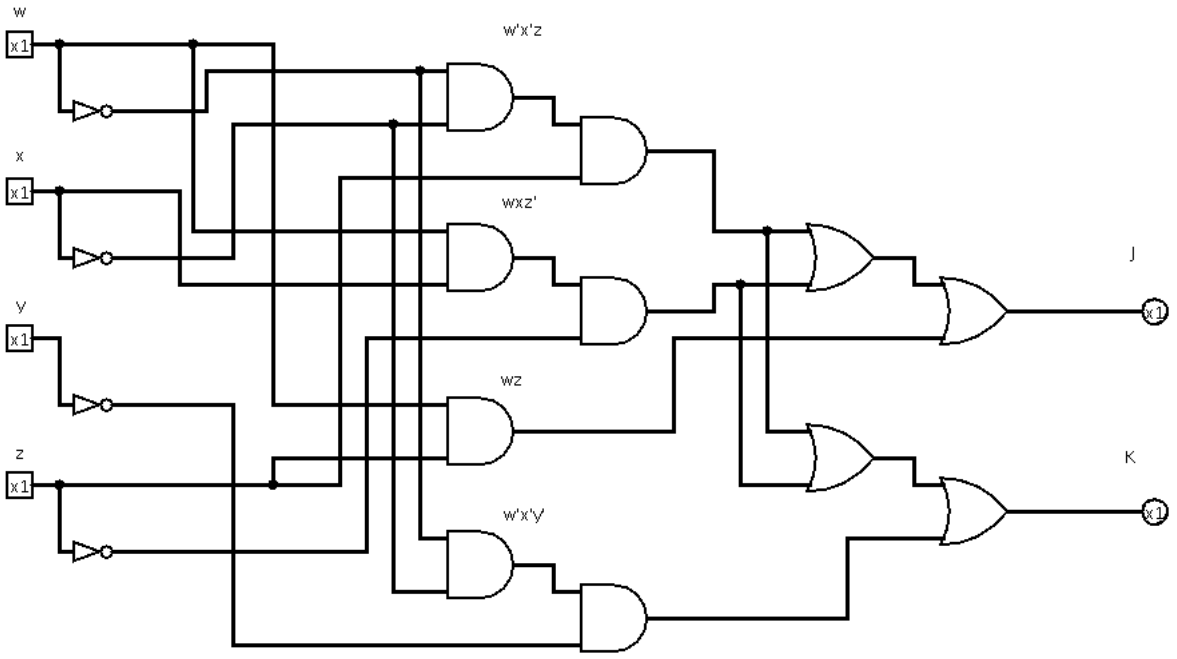

Figure 7: Circuit diagram of the jointly optimized solution of J and K when limited to two input gates.

3 Observations

The jointly optimized solution (Figure 7) of functions J and K reproduced the expected truth table values (Table 1).

The jointly optimized solution did reduce the number of gates albeit slightly. It can be seen from Table 2 that implementing J and K independently resulted in 16 gates and 27 inputs. Implementing these jointly resulted in 15 gates and 26 inputs, a savings of 1 gate and 1 input.

J by itself

gate type	# gates	# inputs
AND	2	4
OR	1	2
NOT	1	1
TOTAL	4	7

J and K independently

gate type	# gates	# inputs
AND	8	16
OR	3	6
NOT	5	5
TOTAL	16	27

K by itself, 2 input gates

gate type	# gates	# inputs
AND	6	12
OR	2	4
NOT	4	4
TOTAL	12	20

J and K jointly

gate type	# gates	# inputs
AND	7	14
OR	4	8
NOT	4	4
TOTAL	15	26

Table 2: Metrics of gate and input counts for various configurations of J and K.

4 Conclusion

The lab was a success in developing a optimized hardware implementation of two distinct logic functions. The jointly optimized solution resulted in a slight, but still significant, reduction in the number of gates and gate inputs.