Lab 9
Two-Bit Adder in Verilog

Lab report due before your lab period on November 2–4

- Read and follow the Icarus Verilog *Getting Started Guide* at http://iverilog.wikia.com/wiki/Getting_Started
- Read and follow the GTKWave introduction at http://iverilog.wikia.com/wiki/GTKWAVE
- After you have an understanding of the Verilog HDL and the Icarus Verilog and GTKWave tools, implement a two-bit adder in Verilog
  - Use dataflow modeling for your implementation (primitives and operators only)
  - A two-bit adder takes in two two-bit values and produces a three-bit result, as follows:

A_1	A_0	B_1	B_0	C	S_1	S_0
0	0	0	0	0	0	0
0	0	0	1	0	0	1
0	0	1	0	0	1	0
0	0	1	1	0	1	1
0	1	0	0	0	0	1
0	1	0	1	0	1	0
0	1	1	0	0	1	1
0	1	1	1	1	0	0
1	0	0	0	0	1	0
1	0	0	1	0	1	1
1	0	1	0	1	0	0
1	0	1	1	1	0	1
1	1	0	0	0	1	1
1	1	0	1	1	0	0
1	1	1	0	1	0	1
1	1	1	1	1	1	0

- Test your adder using Icarus Verilog and GTKWave, which should involve creating a testbench for your adder

The report for this lab should include the following sections:

1. Description/Objectives
2. Procedure, which must include
   (a) A screenshot from GTKWave showing correct operation of your adder
3. Observations
4. Conclusions
5. Appendix
   (a) The Verilog code for your adder (not your testbench)