EECE 144
Fall 2011

Lab Report #6
Section 4
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1 Description/Objectives

The objective of this lab is to simplify a function in to two equivalent forms, one using NAND's and the other using NOR's, then implement this in hardware.

2 Procedure

The procedure for this lab consists of several parts. First, using the given logic function, it is simplified using Karnaugh Maps. Then this simplified function is manipulated in to two forms with one using only NAND's and the other using only NOR's.

The canonical SOP form of the equation used in this lab is given in Equation 1.

$$\begin{aligned} f(a,b,c,d) &= \sum m(0,2,8,10,12,13,14,15) \\ &= m_0 + m_2 + m_8 + m_{10} + m_{12} + m_{13} + m_{14} + m_{15} \\ &= a'b'c'd' + a'b'cd' + ab'c'd' + ab'cd' + abc'd' + abc'd + abcd' + abcd \end{aligned} \tag{1}$$

The truth table produced from Equation 1 is shown in Figure 1. And the Karnaugh Map produced from the truth table is shown in Figure 2. Using the groupings produced by the Karnaugh Map results in the simplified form in Equation 2.

$$f(a, b, c, d) = ab + b'd' \tag{2}$$

Index	a	b	c	d	f
0	0	0	0	0	1
1	0	0	0	1	0
2	0	0	1	0	1
3	0	0	1	1	0
4	0	1	0	0	0
5	0	1	0	1	0
6	0	1	1	0	0
7	0	1	1	1	0
8	1	0	0	0	1
9	1	0	0	1	0
10	1	0	1	0	1
11	1	0	1	1	0
12	1	1	0	0	1
13	1	1	0	1	1
14	1	1	1	0	1
15	1	1	1	1	1

Figure 1: Truth table of Equation 1.

Using the simplified logic function (Equation 2) this can be converted to use only NAND (not and) operations. Equation 3 shows this result. An implementation of this function using gates is shown in Figure 3.

$$\begin{aligned} f(a, b, c, d) &= ab + b'd' && \text{(original equation)} \\ &= (ab + b'd'')'' \\ &= ((ab)'(b'd'))' && \text{(NAND form)} \end{aligned} \tag{3}$$

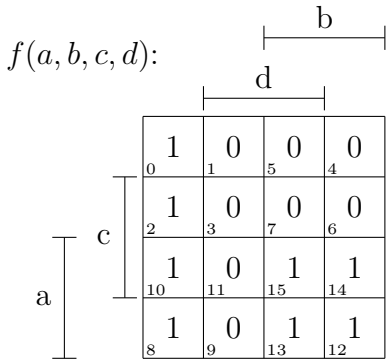

Figure 2: Karnaugh Map representations of Equation 1.

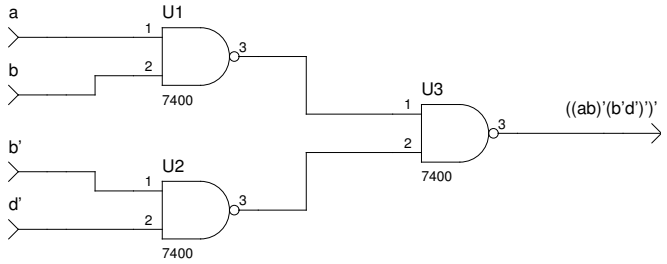

Figure 3: Circuit definition of NAND (Equation 3).

Again using the simplified logic function (Equation 2) this can be converted to use only NOR (not or) operations. Equation 4 shows this result. An implementation of this function using gates is shown in Figure 4.

$$\begin{aligned} f(a,b,c,d) &= ab + b'd' && \text{(original equation)} \\ &= (ab)'' + (b'd')'' \\ &= [(a' + b')' + (b + d)']'' && \text{(NOR form)} \end{aligned} \tag{4}$$

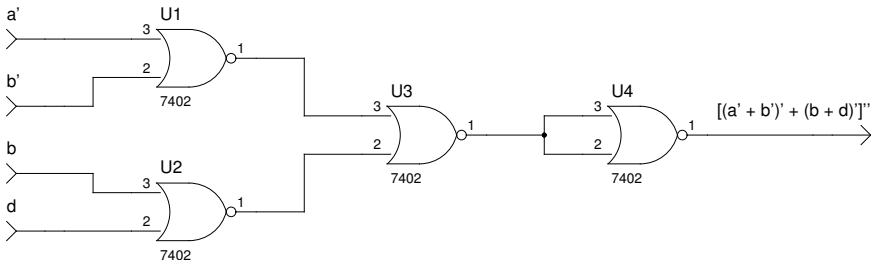

Figure 4: Circuit definition of NOR (Equation 4).

3 Observations

The output of each logic function implemented in hardware (Figure 3, Figure 4) agreed with the expected values of the truth table (Figure 1).

4 Conclusion

This lab was a success in showing that a simplified function, implemented in hardware using only NAND's or only NOR's, will produce an equivalent function.