EECE 311
Fall 2011

Lab Report #5
Modeling and Analyzing RLC circuits with SPICE
10/11/2011

Signature	Printed Name	Date
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Contents

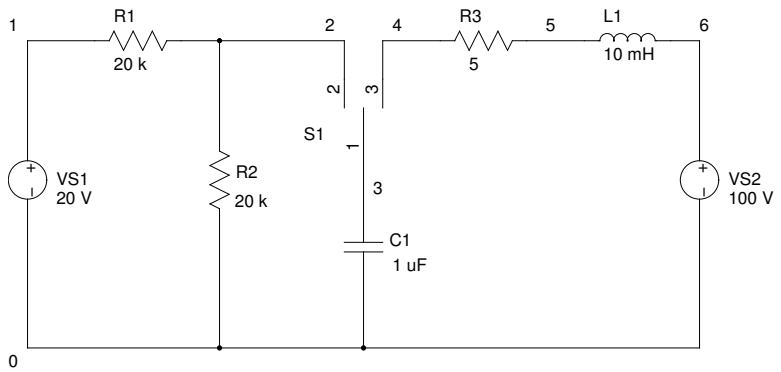

Figure 1: Circuit definition. Nodes denoted by numbers with 0 as common. The switch (S1) starts at $t = 0^-$ connected from terminals 1 to 2. At $t = 0$ it disconnects from 1 to 2 and connects to 1 to 3.

1 Objective

The objective of this laboratory exercise is to learn and gain experience analyzing and simulating the behavior of first order RC or RL circuits and second order RLC circuits under transient conditions using a SPICE simulator.

2 Equipment

To perform the circuit simulation the Ngspice[1] SPICE[2] simulator was used. Other SPICE simulators such as Pspice[3] and Orcad[4] should work as well.

3 Procedure

The circuit to be analyzed (Figure 1) consists of resistors, voltage sources, a capacitor, a inductor and a switch. The switch alternates the capacitor between two parts of the circuit.

Unfortunately, due to the limitations of SPICE, the circuit can not be implemented directly and must be modified. The first difficulty is that there is no single pole double throw (SPDT) switch. An equivalent can be accomplished using two single pole single throw (SPST) switches. The second problem is that switches cannot be triggered by time, they can only be triggered by voltage changes. The effect of triggering over time be accomplished using a pulsing voltage. In order to read this pulsing voltage without disrupting the circuit being analyzed an additional circuit will be added. The modified version of this circuit is shown in Figure 2.

The SPICE definition is shown in Figure 3.

In general a SPICE simulation can be run using Ngspice with the command

```
ngspice -b your_file.cir
```

where `your_file.cir` replaced by the name of your file containing the SPICE definition. To save the output to a file a redirect can be used as in:

```
ngspice -b your_file.cir > your_file.out
```

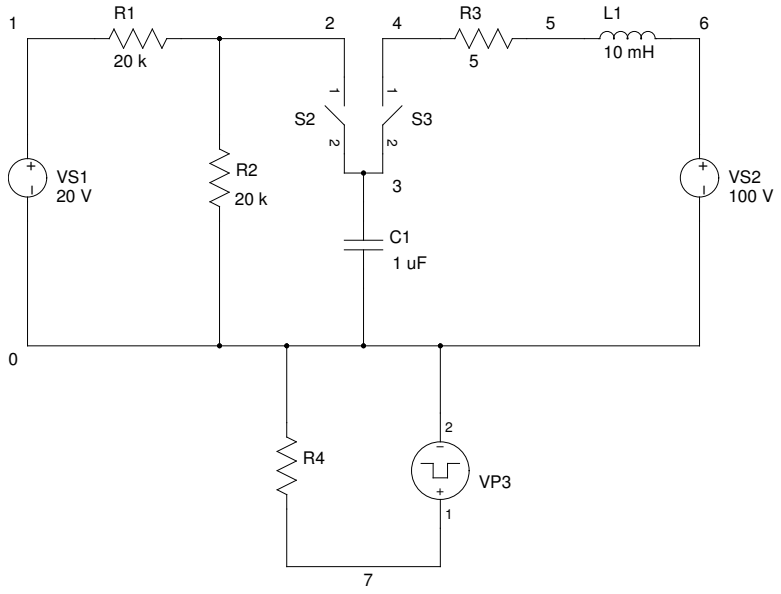

Figure 2: Modification of original circuit definition (Figure 1) to overcome the limitations of SPICE. S2 and S3 are voltage controlled SPST switches that switch simultaneously. At $t = 0^-$ S2 is closed and S3 is open. At $t = 0$ S2 opens and S3 closes. VP3 is a pulsing voltage source used to trigger the switches S2 and S3. R4 is some resistor of arbitrary valued used to establish a measurable voltage from VP3.

```
Switched RLC circuit

VS1 1 0 DC 20V

R1 1 2 20k
R2 0 2 20k

R3 4 5 5
L1 5 6 10mH IC=0

VS2 6 0 DC 100V

S2 2 3 7 0 SMOD
S3 4 3 7 0 TMOD

C1 3 0 1uF IC=10V

* pulsed voltage used to trigger switches
* PULSE(min_v max_v time_delay rise_time fall_time pulse_width period)
*VP3 7 0 DC PULSE(0V 5V 10MS 5US 5US 10MS 20MS)
VP3 7 0 DC PULSE(0V 5V 30MS 5US 5US 30MS 60MS)
R4 7 0 1k

* two switch models:
* One switches from hi to low, and the other from low to hi.
* OrCad
*.MODEL SMOD VSWITCH(RON=0.01   ROFF=105E+5  VON=0.1V VOFF=0V)
*.MODEL TMOD VSWITCH(RON=105E+5 ROFF=0.01    VON=0.1V VOFF=0V)
* ngspice
.MODEL SMOD SW RON=0.01       ROFF=100E+5  VT=1 VH=0.2
.MODEL TMOD SW RON=100E+5     ROFF=0.01    VT=1 VH=0.2

* Uncomment to select the mode you are using:
*--> Non-interactive mode <-----------------------------------------------------
*  ngspice -b <this file>

** .TRAN step end_time
*.TRAN 5us 20ms UIC
*.PLOT TRAN V(1) V(2) V(3)
*.PROBE
*--> Interactive mode <---------------------------------------------------------
*  ngspice <this file>

.CONTROL

*TRAN 5us 100ms UIC
*TRAN 5us 80ms UIC
TRAN 5us 120ms UIC

* pulsed voltage
GNUPLOT plot-v7 V(7)
* capacitor voltage
GNUPLOT plot-v3 V(3)
* gnuplot -persist <file.plt> # (outputs to <file.eps>)

QUIT

.ENDC
*-------------------------------------------------------------------------------
.END
```

Figure 3: SPICE definition of modified circuit definition (Figure 2).

4 Results

To assist in the analysis the time period was adjusted so that a steady state was reached before the circuit was situated. This also made it match the initial conditions. Figure 4 shows the voltage across the capacitor during two periods. It can be seen that there are two components: the under-damped RLC component which oscillates rapidly and the RC component which gradually changes without oscillation.

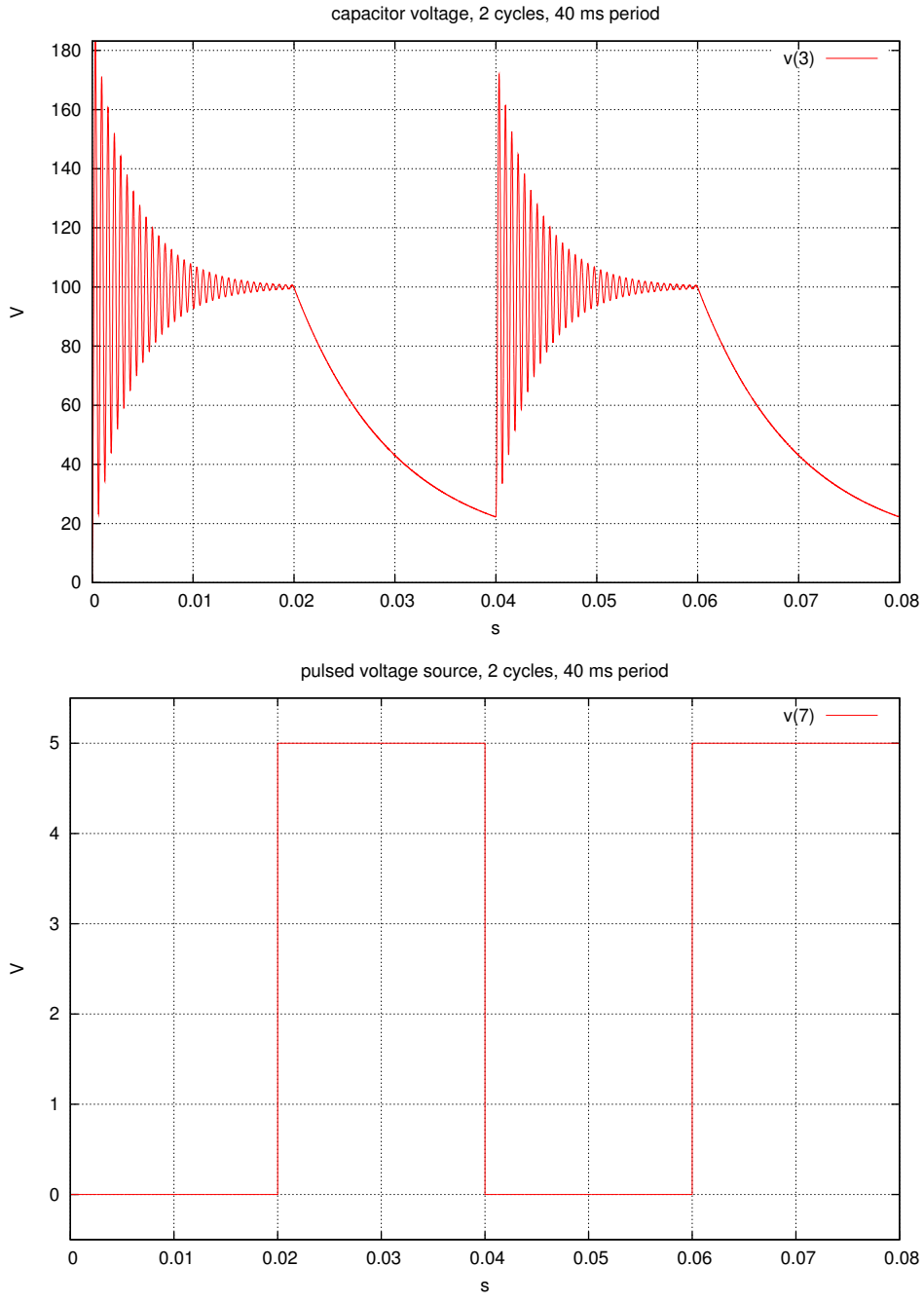

Figure 4: Capacitor voltage and pulsed voltage which controls the switch over the same time period. Two periods are shown (1 period equals 40 ms) and steady state conditions are reached at each point (0, 40 ms, 80 ms).

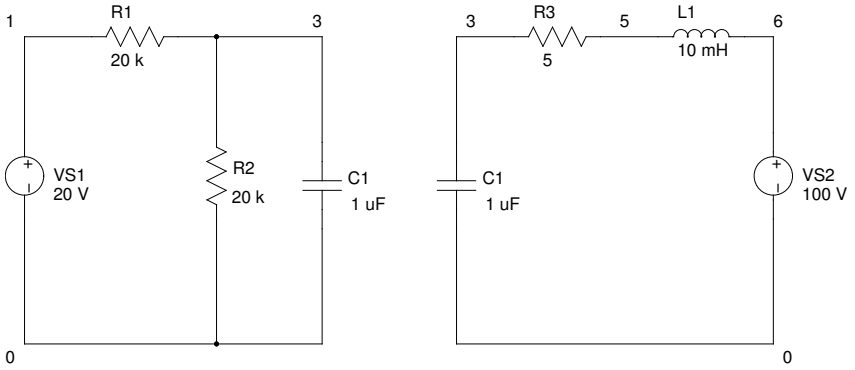

Figure 5: The two states of the modified circuit (Figure 2). When the switch is connected to the left hand side the left most circuit is active and similarly for the right hand side.

5 Correlation with theory

To assist conceptually, the two states of the modified circuit (Figure 2) are shown in Figure 5.

Starting with the left hand side (Figure 5) this circuit is equivalent to a RC circuit with a forced voltage. Construction the equation for the step response of an RC circuit results in Equation 1. Substitution a time period of 20 ms results in a value of 22.1 volts which is nearly the same as the value in Figure 4.

$$\begin{aligned}
\frac{dv_C}{dt} + \frac{v_C}{RC} &= \frac{I_s}{C} \\
v_c &= I_s R + (V_0 - I_s R)e^{-t/RC} \\
v_c(t) &= (1mA)(10k) + (100 - (1mA)(10k))e^{-t/(10k)(1uF)} \\
v_c(t) &= 10 + 90e^{-100t} \qquad (1)
\end{aligned}$$

The right hand side of (Figure 5) behaves like a under-damped series RLC circuit with a forced component as can be seen by the rapid oscillations in Figure 4. Solving the equations results in the following:

$$\begin{aligned}
\alpha &= \frac{R}{2L} \\
&= 250 \\
\omega_0 &= \frac{1}{\sqrt{LC}} \\
&= 10000 \\
\alpha &< \omega_0 \qquad \text{(under-damped)} \\
\omega_d &= \sqrt{\omega_0^2 - \alpha^2} \\
&= 10.0 \times 10^3 \quad \text{[rad/s]}
\end{aligned}$$

$$
\begin{aligned}
v_c(0^+) &= 22.1 \\
v_f(\infty) &= 100 \\
\frac{dv_c(0^+)}{dt} &= 0 \\
v(0) &= v_f + \beta_1 \\
\beta_1 &= 22.1 - 100 \\
&= -77.9 \\
0 &= -\alpha\beta_1 + \omega_d\beta_2 \\
&= 1.95 \times 10^4 + (10 \times 10^3)\beta_2 \\
\beta_2 &= 1.94
\end{aligned}
$$

$$
v(t) = 100 + e^{-250t}\left[-77.9\cos(10 \times 10^3 t) + 1.94\sin(10 \times 10^3 t)\right] \tag{2}
$$

And substituting values in to Equation 2 shows that it behaves approximately according to figure 4.

6 Conclusion

This experiment was a success in analyzing the behavior of first order RC and RL circuits and second order RLC circuits under transient conditions using a SPICE simulator. The calculated values approximately matched the plotted values from the SPICE output and agreed with the theory.

7 References

[1] Ngspice, "Ngspice, spice circuit simulator." `http://ngspice.sourceforge.net`, 2011.

[2] Wikipedia, "Spice — Wikipedia, the free encyclopedia." `http://en.wikipedia.org/wiki/SPICE`, 2011. [Online; accessed 19-September-2011].

[3] Wikipedia, "Pspice — Wikipedia, the free encyclopedia." `http://en.wikipedia.org/wiki/Pspice`, 2011. [Online; accessed 8-October-2011].

[4] "Orcad, electronic design automation software." `http://www.cadence.com/orcad/`, 2011. Cadence Design Systems.