Imperial College London

Department of Electrical & Electronic Engineering

ADIC MSc Laboratory
Mastering Digital Design – Feedback Sheet

Name of Student:

Names of Assessors: Date of Assessment:

BASED ON THE EXPERIMENT **Overall Experiment Grade:**

1. How much has the student done?

☐ Beyond expectation ☐ Some extra ☐ Compulsory ☐ Some missing ☐ Lots missing

2. Logbook Effectiveness

☐ Highly effective ☐ Effective ☐ Acceptable ☐ Contrived ☐ Unreal

3. Ability to find answers from Logbook

☐ Confident ☐ Mostly ☐ Acceptable ☐ Sometimes ☐ Unsure

4. Understanding of materials inside Logbook

☐ Complete ☐ Mostly ☐ Acceptable ☐ Sometimes ☐ Unsure

BASED ON UNDERSTANDING **Overall Understanding Grade:**

5. Mastery of Verilog

☐ Excellent ☐ V. Good ☐ Acceptable ☐ Poor ☐ V. Poor

6. Understand of FPGA and Quartus tools

☐ Excellent ☐ V. Good ☐ Acceptable ☐ Poor ☐ V. Poor

7. Depth of understanding in general

☐ Broad and Deep ☐ Good ☐ Average ☐ Less than average ☐ Poor

FEEDBACK TO STUDENTS: **Overall Grade:**