Analogue and Digital IC Design MSc Course

Mastering Digital Design in Verilog using FPGAs
Experiment Specification Document

Objectives:

1. To ensure all students on the MSc course reaches a common competence level in RTL design using FPGAs in a hardware description language;
2. To act as revision exercise for those who are already competent in Verilog and FPGA.

Format and Assessment:

This laboratory module is in the form of a laboratory experiment where students will be working in pairs randomly assigned. There will be five sessions, each 3-hours long. Most of the content will be delivered in the form of practical exercises divided into FOUR parts. You are expected to complete each part at the beginning of the following week.
Assessment will be in the form of a 15-minutes oral examination to establish whether you have achieved the required attainment level. The assessment forms part of the entire laboratory assessment of the MSc course.

Learning Outcomes:

Part 1: Basic competence in using Intel/Altera's Quartus design systems for Cyclone-V FPGA; appreciate the superiority of hardware description language over schematic capture for digital design; use of case statement to specify combinatorial circuit; use higher level constructs in Verilog to specify complex combinatorial circuits; develop competence in taking a design from description to hardware.

Part 2: Use Verilog to specify sequential circuits; design of basic building blocks including: counters, linear-feedback shift-registers to generate pseudo-random numbers, basic state machines; using enable signals to implement globally synchronisation.

Part 3: Understand how digital components communicate through synchronous serial interface; interfacing digital circuits to analogue components such as ADC and DAC; use of block memory in FPGAs; number system and arithmetic operations such as adders and multipliers; digital signal generation.

Part 4: Understand how to implement a FIFO using counters as pointer registers and Block RAM as storage; implement a relatively complex digital circuit using different building blocks including: counters, finite state machines, registers, encoder/decoder, address computation unit, memory blocks, digital delay elements, synchronisers etc.; learn how to debug moderately complex digital circuits.

Location and Facilities:

Scheduled laboratory sessions (with short lectures) will take place in the ADIC MSc Lab on Level 9 (Room 909). You are welcome to load the design software (Quartus system) on your own laptop. Every pair of students will be allocated an Altera DE1-SoC board with an analogue interface card for the duration of this laboratory experiment.