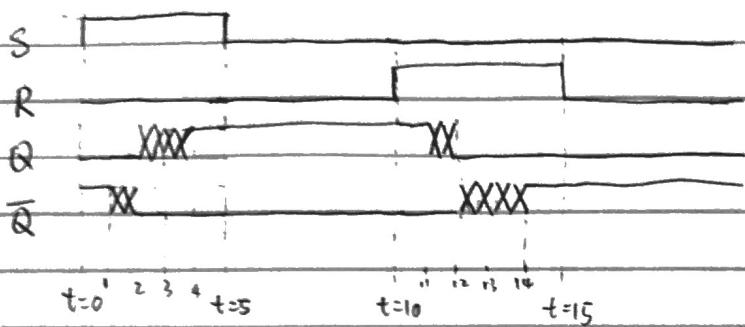


# PSET 3 Solution

1.0(a)



1.0(b)

If  $S=R=0$ ,  $Q$  and  $\bar{Q}$  retain their values.

We can divide the problem into two cases:

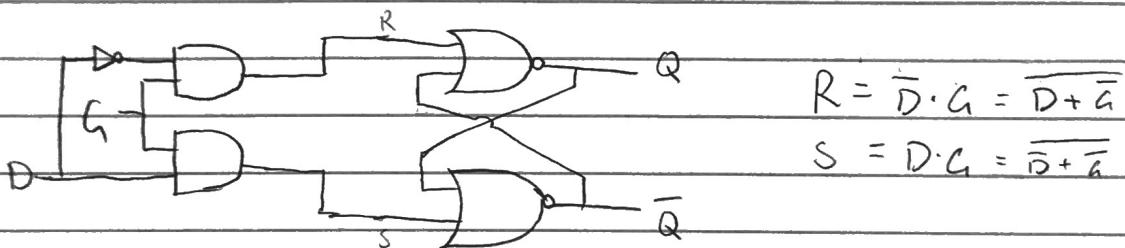
(i)  $Q=1$ ,  $\bar{Q}=0$ , for lower NOR,  $\overline{QS}=0=\bar{Q}$ , upper NOR:  $\overline{RQ'}=1=Q$

(ii)  $Q=0$ ,  $\bar{Q}=1$ , for lower NOR,  $\overline{QS}=1=\bar{Q}$ , upper NOR:  $\overline{RQ'}=0=Q$

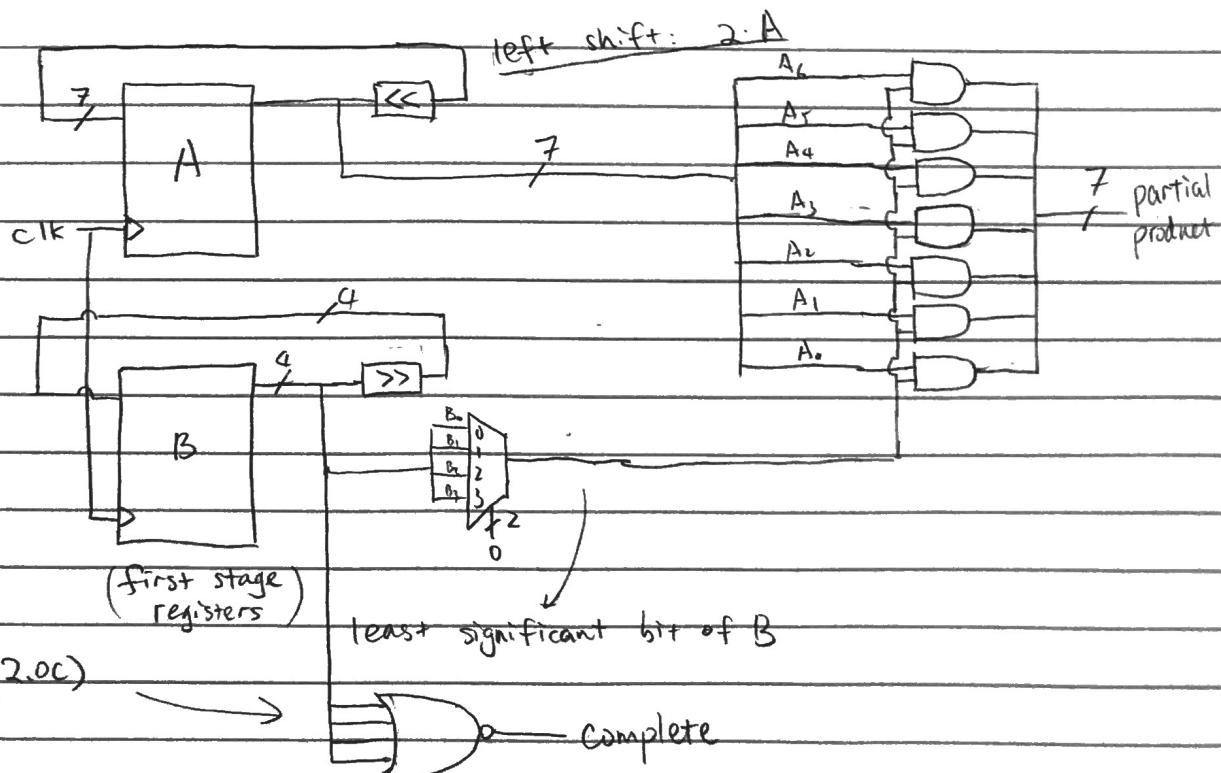
Dynamic Discipline: a.  $S=R=1$ : not allowed

b. Hold each value at least 4 time units

1.0(c)



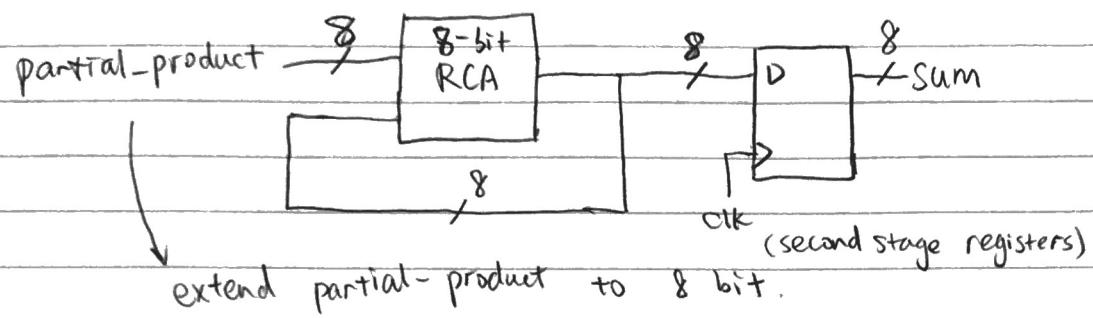
2.0(a)



(2.0c)

complete

2.01(b)



2.0(c) Please see (2.0 a) for figure

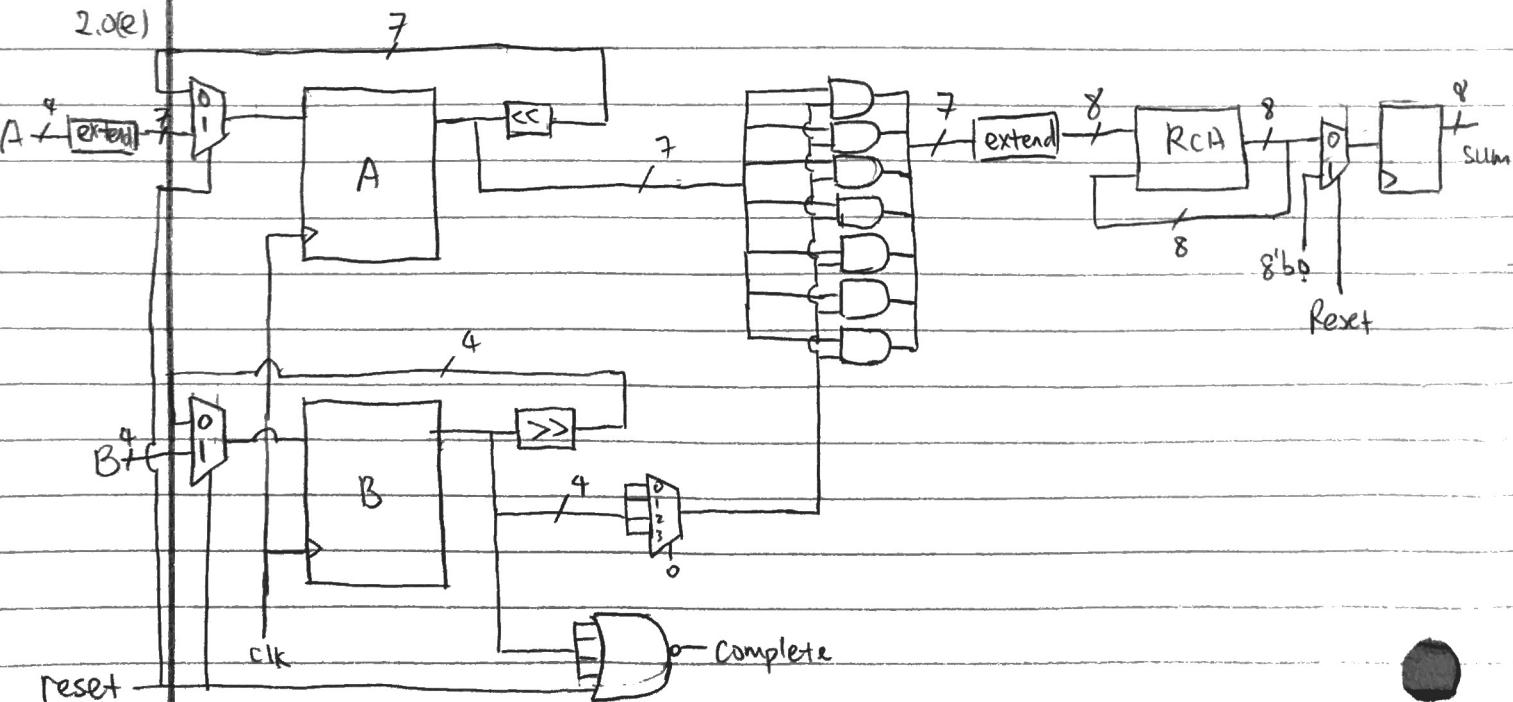
once all bits of B are 0, the sum has been generated.

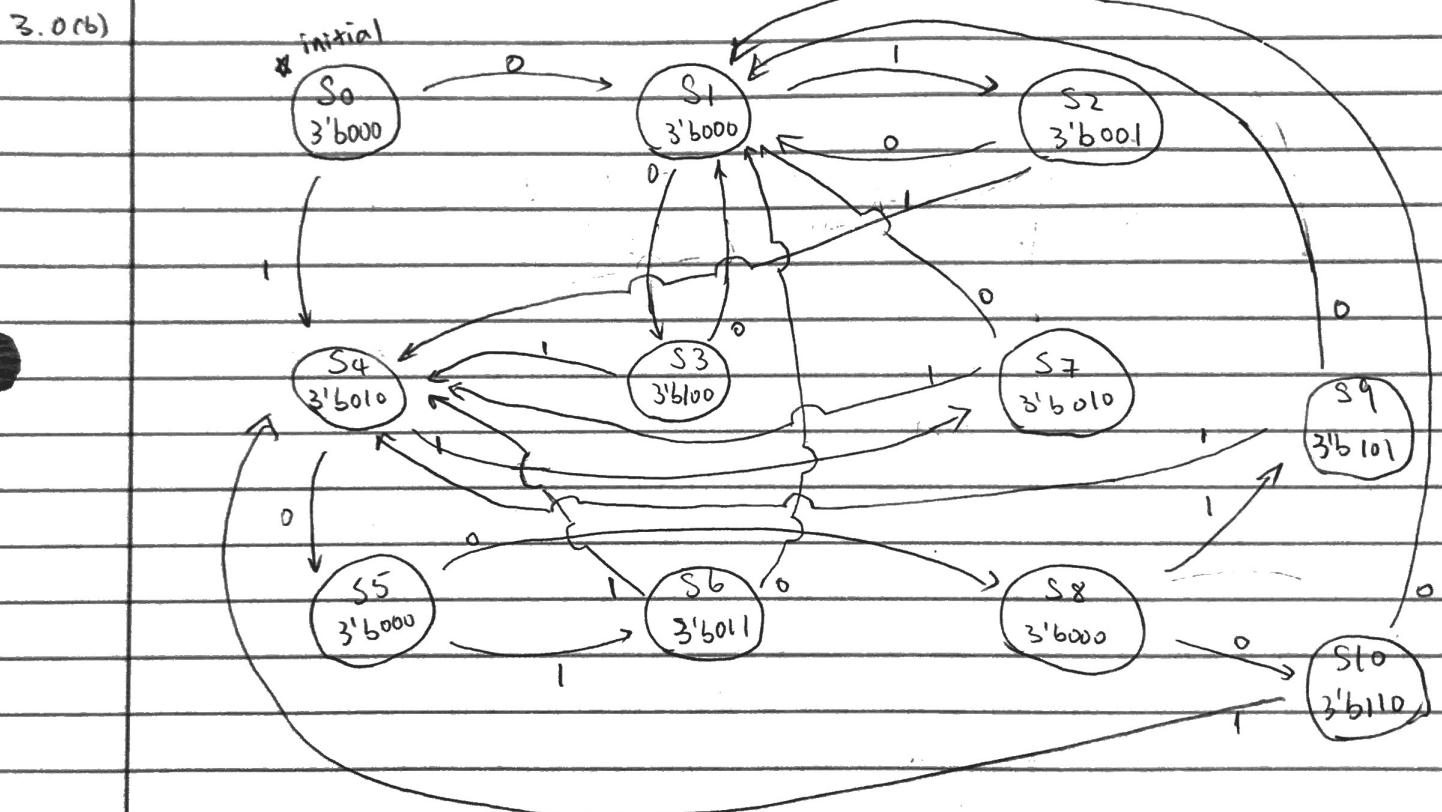
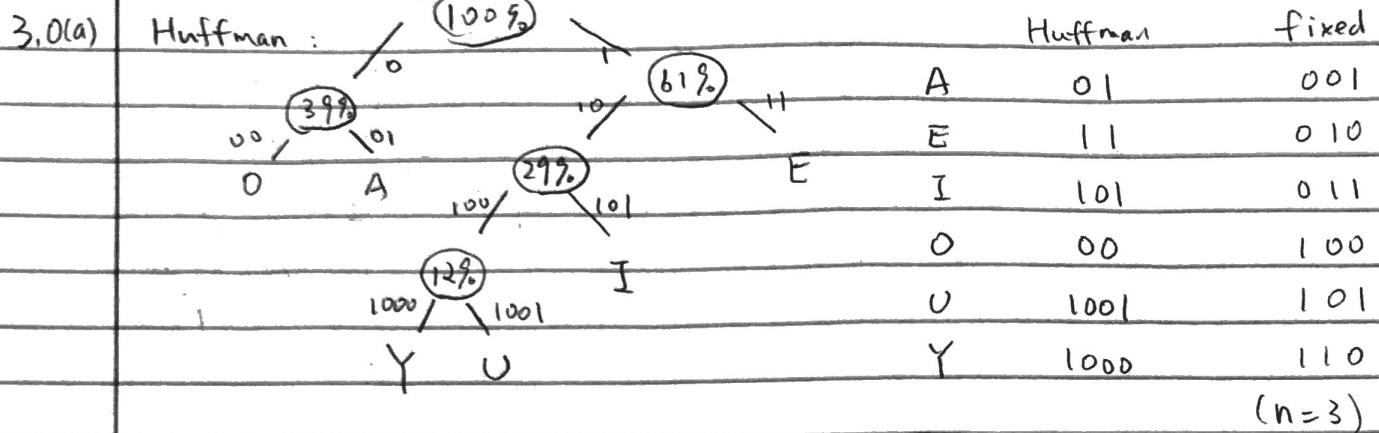
2.0(d) The whole system has 2 stages. Let the  $t_{CD}$ ,  $t_{PO}$  be total delay of the combinational logic between the two stage, i.e. shift registers, AND gates and RCA block between A,B Registers and the accumulator. Let clock cycle be  $T_{clk}$ .

$$\begin{cases} T_{Clk} > t_{pp} + t_{\text{setup}} \\ t_{\text{hold}} < t_{cd} \end{cases} \rightarrow \begin{array}{l} \text{Setup time constraint} \\ \text{Hold time constraint} \end{array}$$

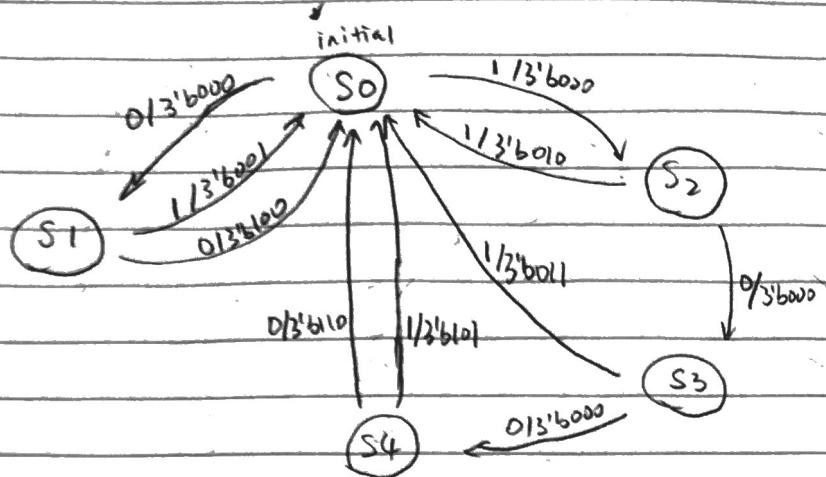
assume  $\text{clk} \rightarrow q$  delay of D-register is considered in the logic delay.

2.0(e)





3.0(c)



3.0(d)

State	input	next state	output
(S0) 000	0	S1	3'b000 / -
	1	S2	3'b000 / -
(S1) 001	0	S0	3'b100 / "0"
	1	S0	3'b001 / "A"
(S2) 010	0	S3	3'b000 / -
	1	S0	3'b010 / "E"
(S3) 011	0	S4	3'b000 / -
	1	S0	3'b011 / "I"
(S4) 100	0	S0	3'b110 / "Y"
	1	S0	3'b101 / "U"

3.0(e)

