EEM16/CSM51A (Fall 2017)

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Final 8am Monday Dec. 11, 2017 (Moore 100)

First half

Functional specification

- Binary signals **(Lec01 PDF)**
  - Positional number systems [10.1]
    - base 10, 2, 8, 16
  - Positive and negative integers [10.3]
  - Fixed point [11.2]
  - Floating point [11.3]
  - Encoders / decoders [8.2 / 8.4]
    - binary <-> one-hot
- Information and coding **(6.004 L01)**
  - Bits as information content
  - Entropy of a signal
- Boolean algebra **(Lec02 PDF)**
  - Axioms [3.1]
  - Properties [3.2]
- Boolean representation of functional relationship **(6.004 L04)**
  - Truth table [6.3]
  - minterm / maxterm representation = canonical normal forms [3.4]
  - K-map [6.5]
  - Boolean expression / gates [3.5]

Physical system implementation (6.004 L02-L03)

- Noise / noise margins [1.2]
- Static discipline [6.1, 6.2]
- CMOS transistors [4.2]
- CMOS gates [4.3]
- Timing: t_{pd}, t_{cd} [5.1, 15.1]
- Glitches and leniency [6.10]

Combinational logic synthesis (6.004 L04)

- K-map implicants : SOP / POS [6.6-6.9]
- Muxes [8.3]
- ROMs [8.8]

Examples of CL systems

- Addition [10.2]
- Subtraction [10.3]
- Multiplication [10.4]
- Comparison [8.6]

Second half

Encodings (6.004 L01)

- Fixed-length encodings
- Variable-length (e.g. Huffman) encoding
- FSM decoder

Sequential logic implementation (6.004 L05)

- Memory using CMOS feedback [27]
  - D-latch [27.1]
  - D-register [27.2]
- Single clock SL [14.2]
- Dynamic discipline: $t_{setup}, t_{hold}, t_{clk}$ [15.3]
- Clock skew, jitter: [15.4]

Finite state machines (6.004 L06)

- Moore vs Mealy machine [14.2]
- Datapath FSMs [16.1, 16.2]
- Controller FSMs [16.3]
- State diagrams [14.2]
- State transition table [14.2]
- Sequential logic synthesis [14.4, 14.5]

Pipelining (6.004 L07)

- k-pipeline of combinational logic [23]
  - Well-formed pipelines [23.1]
  - Throughput and latency [23.1]
  - Parallelizing slow blocks [23.6]
- Pipelining Sequential logic
  - Single clock (synchronous, local timing)
  - Multiple clocks (synchronous, global timing)
  - Signalling / pipeline stalls
- Timing (pipeline) diagrams

Examples of SL systems

- Counter (with up/down/pause/reset)
- Shift register (serial-to-parallel and parallel-to-serial converters)
- Divisible-by or modulo n (e.g. 3, 4, 12)
- Multiplier
- Pipelined adder
- General FSM

System performance (6.004 L08)

- Throughput
- Latency
- Area
- Energy
- Power
- Design effort

Additional (optional) references

Sections in Dally and Harting 2012, *Digital Design: A Systems Approach*, indicated in [brackets] above

- 1.1-1.2
- 2.1
- 3
- 4.2-4.3
- 5.1
- 6
- 8.1-8.8
- 10.1-10.4
- 11.2-11.3
- 14.1-14.2, 14.4-14.5
- 15.1-15.4
- 16
- 23.1-23.5
- 27.1-27.3