EEM16/CSM51A (Fall 2017)

Logic Design of Digital Systems

Prof. Ankur Mehta
mehtank@ucla.edu

Syllabus (tentative)

	Monday	**Wednesday**
Week 1	**October 2, 2017** Course introduction Number systems	**October 4, 2017** Boolean algebra
Week 2	**October 9, 2017** Information and coding	**October 11, 2017** Digital abstraction
Week 3	**October 16, 2017** CMOS	**October 18, 2017** Combinational logic design
Week 4	**October 23, 2017** Verilog (combinational)	**October 25, 2017** Combinational building blocks
Week 5	**October 30, 2017** Arithmetic and numbers	**November 1, 2017** Midterm
Week 6	**November 6, 2017** Sequential logic (1)	**November 8, 2017** Verilog and FSM
Week 7	**November 13, 2017** Sequential logic (2)	**November 15, 2017** Controller/datapath
Week 8	**November 20, 2017** FPGA synthesis	**November 22, 2017** Timing and synchronization
Week 9	**November 27, 2017** Performance measures	**November 29, 2017** Pipelining
Week 10	**December 4, 2017** Systems	**December 6, 2017** Final review

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Staff

- Instructor: Ankur Mehta
  - Professor in ECE department
  - email: mehtank@ucla.edu
  - office: 6730D Boelter Hall
- TAs:
  - Albert Lee
  - Ghaith Hattab
  - Tianwei Xing

Schedule

- Lecture MW 4-6pm, Kinsey 1220B
- Discussion sections
  - 1A: PUB AFF 2319 / F 2:00pm-3:50pm (TA: Albert Lee)
  - 1B: PAB 1434A / F 10:00am-11:50am (TA: Tianwei Xing)
  - 1C: PAB 1434A / F 12:00pm-1:50pm (TA: Albert Lee)
  - 1D: FRANZ 1260 / R 4:00pm-5:50pm (TA: Ghaith Hattab)
  - 1E: ROLFE 3126 / F 8:00am-9:50am (TA: Ghaith Hattab)
- Office hours
  - Instructor: MR 2-3pm, 6730D Boelter Hall
  - TAs: TBD

Resources:

- No textbook!
- No paper
- Online lecture notes and videos
- Online assignments and submissions

Grading structure:

- Problem Sets (4 equal weight): 17% total
- Design labs (3 unequal weight): 17% total
- Participation (Lecture, discussion, forums): 8%
- Midterm (1.5 hr, 11/1 in class): 23%
- Final (3 hr, 12/11 8am): 35%