# 3-D Stacked Die: Now or Future?

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## PANEL SUMMARY

The continuation of Moore's law by conventional CMOS scaling is becoming challenging. 3D Packaging with 3D through silicon vias (TSV) interconnects is showing promise for extending scaling using mature silicon technology, providing another path towards the "More than Moore". Two years ago, the big unceasing question was "Why 3D?" Today, as we move forward with the concrete implementation of the technology, the questions are now "When 3D?" and "How 3D?" There are quite a few brave souls who have taken this disruptive interconnect technology and are investing in it today to gain benefit from it. However, for many the lingering questions remain "Are we there yet?" "Is it now or the future?"

This panel brings together key thought leaders in the area of 3D Packaging with 3D TSV interconnects to tell us how they see 3D IC shaping up in the coming year(s) and the challenges that lie ahead associated with TSV in practical design.

### Categories and Subject Descriptors
B.7.1 [Integrated Circuits] Types and Design Styles
- Advanced technologies

### General Terms
Performance & Design

### Keywords
3-D, integrated circuits



## PANELIST VIEWPOINTS

**Myung-Soo Jang:** 3D IC integration using TSV interconnections is becoming a critical component to overcome the technology scaling barriers and low power requirements in mobile devices. We expect that the demand for changing from conventional system in a package (SiP) to TSV-SiP will be on the rise because TSV process technology and design methodologies are being provided by leading companies. Logic to memory die stacking is a good example of the benefits of TSV interconnections compared with a PoP structure. From the viewpoint of design solution for TSV-SiP, EDA vendors may prefer utilizing their existing tools, where each die is implemented individually using a single die solution with modeling for the other dies. Since TSV-SiP is still a chip-to-chip connection and only stacks a few die, such a coarse integration method can be a tentative solution.

However, we are facing challenges that require advanced design and analysis tools with seamless integration flow for better analysis accuracy and reduced turn around time. At the same time, here have been many academic research efforts focusing on true 3D IC designs. We might not see in the near future a true 3D IC, however, that shares clocks and power among multi-dies as long as the technology scaling continues to be competitive in terms of manufacturing and implementation cost. Hence, we hope to see more practical research topics in the literature that meet the industrial needs.

**LC Lu:** 3DIC/TSV is an industry trend gaining momentum due to the ever-converging alignment of the technology's benefits and market/application demands for "More than Moore." Products using this technology will be rolled out in many different market segments. TSMC has been actively developing the technology according to customer and market needs. Different forms of 3DIC/TSV such as die-on-wafer and die-on-die stacking are currently in the works. This development includes not just the fabrication process, but a complete solution which will allow customers to realize the maximum value from TSMC's 3DIC/TSV technology. Activities in design, packaging, testing, methodologies and infrastructure are ongoing with many

ecosystem partners. Innovation on new design methodologies is needed to address new challenges such as good die sorting, multiple process variations, and thermal/mechanical stress. TSMC will deliver the 3DIC/TSV solution with high quality and in large volume, the same way TSMC has delivered other technologies in the past.

**Marchal Pol:** 3D technology will hit the market in the next two to three years. The technology has great benefits for the three main application drivers of the semiconductor industry: convergence, high performance and memory systems. At IMEC, we have road maps for the design and technology challenges for each of these application domains. A common challenge is to co-optimize the technology and design in order to maximize yield and guarantee reliability. We'll introduce the main trade-offs involved, and indicate where EDA must contribute: specifically, an integrated design flow enabling the co-optimization of chip and package design for SI/PI as well as mechanical/thermal integrity.

**Philippe Magarshack:** TSV as a process technology is now in production at ST and other CMOS Image Sensors (CIS) Manufacturers. This capability has yet to be translated into successful and viable products in other markets. The "killer app" using TSVs will solve either form factor issues, or address low-power in a more efficient way, or enable more communication bandwidth among a SOC processor and its associated memory cache. It may have to solve all of the above issues in order to make it through all the hurdles associated with bringing such a disruptive technology to the industry. Consensus is building that such an application may be a SOC or processor with a stacked DRAM via the "Wide-IO" standard. In any case, the EDA tools to enable the architecture partitioning, 3D-Floorplanning and 3D physical timing closure are yet to be developed. ST is partnering with selected EDA vendors, OSATs, Memory makers and Standards bodies to enable an eco-system addressing 3D-design needs for the future killer-app.

**Riko Radojcic:** It is clear that through silicon via-based 3D integration technology offers some very promising advantages over the more conventional 2D CMOS implementation. In the wireless application space, the intrinsic advantages include power, performance and form factor, which in the short term come with a penalty of some increased cost and risk. At the same time, it is not clear if, and/or when the traditional 2D scaling may become prohibitive. Consequently, we believe that the TSV 3D stacking technology is an 'in addition to' rather than 'instead of' technology option and that successful products will use 3D stacking of heterogeneous die in conjunction with implementation in leading edge technology on die that merit the corresponding cost-performance trade off. Furthermore, the path to successful implementation will necessarily involve architectures which cannot be reasonably implemented with more conventional technology solutions. The principal barriers to implementation include: identification of a technology sweet spot, definition of an optimized architecture, and demonstration of the value proposition that balances out the increased short term cost and risk penalty