```c
/* Memory Map */
#define CONFIG      0x00
#define EN_AA       0x01
#define EN_RXADDR   0x02
#define SETUP_AW    0x03
#define SETUP_RETR  0x04
#define RF_CH       0x05
#define RF_SETUP    0x06
#define STATUS      0x07
#define OBSERVE_TX  0x08
#define CD          0x09
#define RX_ADDR_P0  0x0A
#define RX_ADDR_P1  0x0B
#define RX_ADDR_P2  0x0C
#define RX_ADDR_P3  0x0D
#define RX_ADDR_P4  0x0E
#define RX_ADDR_P5  0x0F
#define TX_ADDR     0x10
#define RX_PW_P0    0x11
#define RX_PW_P1    0x12
#define RX_PW_P2    0x13
#define RX_PW_P3    0x14
#define RX_PW_P4    0x15
#define RX_PW_P5    0x16
#define FIFO_STATUS 0x17
#define DYNPD       0x1C

/* Bit Mnemonics */

/* configuration register */
#define MASK_RX_DR  6
#define MASK_TX_DS  5
#define MASK_MAX_RT 4
#define EN_CRC      3
#define CRCO        2
#define PWR_UP      1
#define PRIM_RX     0

/* enable auto acknowledgment */
#define ENAA_P5     5
#define ENAA_P4     4
#define ENAA_P3     3
#define ENAA_P2     2
#define ENAA_P1     1
#define ENAA_P0     0

/* enable rx addresses */
#define ERX_P5      5
#define ERX_P4      4
#define ERX_P3      3
#define ERX_P2      2
```

```c
 53  #define ERX_P1        1
 54  #define ERX_P0        0
 55
 56  /* setup of address width */
 57  #define AW            0 /* 2 bits */
 58
 59  /* setup of auto re-transmission */
 60  #define ARD           4 /* 4 bits */
 61  #define ARC           0 /* 4 bits */
 62
 63  /* RF setup register */
 64  #define PLL_LOCK      4
 65  #define RF_DR         3
 66  #define RF_PWR        1 /* 2 bits */
 67
 68  /* general status register */
 69  #define RX_DR         6
 70  #define TX_DS         5
 71  #define MAX_RT        4
 72  #define RX_P_NO       1 /* 3 bits */
 73  #define TX_FULL       0
 74
 75  /* transmit observe register */
 76  #define PLOS_CNT      4 /* 4 bits */
 77  #define ARC_CNT       0 /* 4 bits */
 78
 79  /* fifo status */
 80  #define TX_REUSE      6
 81  #define FIFO_FULL     5
 82  #define TX_EMPTY      4
 83  #define RX_FULL       1
 84  #define RX_EMPTY      0
 85
 86  /* dynamic length */
 87  #define DPL_P0        0
 88  #define DPL_P1        1
 89  #define DPL_P2        2
 90  #define DPL_P3        3
 91  #define DPL_P4        4
 92  #define DPL_P5        5
 93
 94  /* Instruction Mnemonics */
 95  #define R_REGISTER    0x00 /* last 4 bits will indicate reg. address */
 96  #define W_REGISTER    0x20 /* last 4 bits will indicate reg. address */
 97  #define REGISTER_MASK 0x1F
 98  #define R_RX_PAYLOAD  0x61
 99  #define W_TX_PAYLOAD  0xA0
100  #define FLUSH_TX      0xE1
101  #define FLUSH_RX      0xE2
102  #define REUSE_TX_PL   0xE3
103  #define ACTIVATE      0x50
104  #define R_RX_PL_WID   0x60
```

```
105  #define NOP            0xFF
106
```