```
1
 2 #define UCPHA0 1
 3 #define BAUD RATE 9600UL
 4 #define UBRR_VALUE ((F_CPU)/(2UL*BAUD_RATE))-1
 6 #include "nrf24.h"
7 #include "Command Handler.h"
9 uint8_t payload_len;
10 uint8_t selectedChannel;
11
12 uint8_t MOTORIZED_BOARD_ADDR[5] =
                                         {0xF0,0xF0,0xF0,0xF0,0xC9};
13 uint8 t MAIN BOARD ADDR[5] =
                                              \{0xA4,0xA4,0xA4,0xA4,0xA4\};
14 uint8 t POWER BOARD ADDR[5] =
                                         \{0xF0,0xF0,0xF0,0xF0,0xF0\};
15
16 uint8_t* BOARD_ADDRESS[3] = {&MAIN_BOARD_ADDR[0], &POWER_BOARD_ADDR[0],
      &MOTORIZED_BOARD_ADDR[0]};
   uint8 t* CURRENT BOARD ADDRESS = &MOTORIZED BOARD ADDR[0];
17
18
19
   uint8_t GENERAL_RF_CHANNEL = 112;
20
21
22
23 void nrf24_init()
24 {
25
        nrf24_setupPins();
26
        nrf24_ce_digitalWrite(LOW);
27
        nrf24_csn_digitalWrite(HIGH);
28 }
29
30 void nrf24_config(uint8_t channel, uint8_t pay_length)
31 {
32
        /* Use static payload length ... */
33
        payload_len = pay_length;
34
        selectedChannel = channel;
35
        // Set RF channel
36
        nrf24_configRegister(RF_CH,channel);
37
        // Set length of incoming payload
38
        nrf24_configRegister(RX_PW_P0, 0x00); // Auto-ACK pipe ...
39
        nrf24_configRegister(RX_PW_P1, payload_len); // Data payload pipe
        nrf24_configRegister(RX_PW_P2, 0x00); // Pipe not used
40
41
        nrf24_configRegister(RX_PW_P3, 0x00); // Pipe not used
42
        nrf24_configRegister(RX_PW_P4, 0x00); // Pipe not used
        nrf24_configRegister(RX_PW_P5, 0x00); // Pipe not used
43
44
        // 1 Mbps, TX gain: 0dbm
45
        nrf24_configRegister(RF_SETUP, (0<<RF_DR)|((0x03)<<RF_PWR));</pre>
46
        // CRC enable, 1 byte CRC length
47
        nrf24_configRegister(CONFIG,nrf24_CONFIG);
48
        // Auto Acknowledgment
49
        nrf24_configRegister(EN_AA,(1<<ENAA_P0)|(1<<ENAA_P1)|(0<<ENAA_P2)|</pre>
          (0 < \langle ENAA P3 \rangle) | (0 < \langle ENAA P4 \rangle) | (0 < \langle ENAA P5 \rangle);
        // Enable RX addresses
50
```

```
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```

```
2
```

```
51
        nrf24 configRegister(EN RXADDR,(1<<ERX P0)|(1<<ERX P1)|(0<<ERX P2)|</pre>
          (0<<ERX_P3)|(0<<ERX_P4)|(0<<ERX_P5));
52
        // Auto retransmit delay: 1000 us and Up to 15 retransmit trials
53
        nrf24_configRegister(SETUP_RETR,(0x04<<ARD)|(0x0F<<ARC));</pre>
54
        // Dynamic length configurations: No dynamic length
55
        nrf24_configRegister(DYNPD,(0<<DPL_P0)|(0<<DPL_P1)|(0<<DPL_P2)|(0<<DPL_P3)|</pre>
          (0<<DPL P4)|(0<<DPL P5));
56
57
   }
58
59
   bool nrf24_checkConfig(){
        // Check all registers
60
61
        if (nrf24_checkRegister(RF_CH, selectedChannel,1)==false) return false;
62
        if (nrf24 checkRegister(RX PW P0, 0x00,1)==false) return false;
63
        if (nrf24_checkRegister(RX_PW_P1, payload_len,1)==false) return false;
64
        if (nrf24_checkRegister(RX_PW_P2, 0x00,1)==false) return false;
65
        if (nrf24_checkRegister(RX_PW_P3, 0x00,1)==false) return false;
        if (nrf24 checkRegister(RX PW P4, 0x00,1)==false) return false;
66
        if (nrf24_checkRegister(RX_PW_P5, 0x00,1)==false) return false;
67
        if (nrf24_checkRegister(RF_SETUP, (0<<RF_DR)|((0x03)<<RF_PWR),1)==false)</pre>
68
                                                                                         P
          return false;
        if (nrf24_checkRegister(CONFIG,nrf24_CONFIG,1)==false) return false;
69
70
        if (nrf24_checkRegister(EN_AA,(1<<ENAA_P0)|(1<<ENAA_P1)|(0<<ENAA_P2)|
                                                                                         P
          (0<<ENAA_P3)|(0<<ENAA_P4)|(0<<ENAA_P5),1)==false) return false;
71
        if (nrf24 checkRegister(SETUP RETR,(0x04<<ARD)|(0x0F<<ARC),1)==false) return
          false;
        if (nrf24 checkRegister(DYNPD,(0<<DPL_P0)|(0<<DPL_P1)|(0<<DPL_P2)|</pre>
72
                                                                                         P
          (0<<DPL_P3)|(0<<DPL_P4)|(0<<DPL_P5),1)==false) return false;</pre>
73
74
        return true;
75 }
76
77
   bool nrf24_checkAvailability(){
78
        if (nrf24_checkRegister(RF_CH, selectedChannel,1)==true) { return true; }
          else { return false;}
79
   }
80
81
82
83
   void faultyRF Alarm(){
84
85
        CLEAR_FAULTY_RF_LED;
86
        for (uint8_t x = 0; x < 6; x++)
87
        {
88
            FLIP FAULTY_RF_LED;
89
            _delay_ms(125);
90
91
        _delay_ms(250);
92 }
93
94
95
```

```
96 /* Set the RX address */
 97 void nrf24_rx_address(uint8_t * adr)
 98 {
 99
        nrf24_ce_digitalWrite(LOW);
100
        nrf24_writeRegister(RX_ADDR_P1,adr,nrf24_ADDR_LEN);
101
        nrf24_ce_digitalWrite(HIGH);
102 }
103
104 /* Returns the payload length */
105 uint8_t nrf24_payload_length()
106 {
        return payload_len;
107
108 }
109
110 /* Set the TX address */
111 void nrf24_tx_address(uint8_t* adr)
112 {
         /* RX ADDR P0 must be set to the sending addr for auto ack to work. */
113
114
        nrf24_writeRegister(RX_ADDR_P0,adr,nrf24_ADDR_LEN);
115
        nrf24_writeRegister(TX_ADDR,adr,nrf24_ADDR_LEN);
116 }
117
118 /* Checks if data is available for reading */
119 /* Returns 1 if data is ready ... */
120 uint8_t nrf24_dataReady()
121 {
122
        // See note in getData() function - just checking RX_DR isn't good enough
123
        uint8_t status = nrf24_getStatus();
124
125
        // We can short circuit on RX_DR, but if it's not set, we still need
        // to check the FIFO for any pending packets
126
        if ( status & (1 << RX_DR) )</pre>
127
128
129
             return 1;
130
131
132
        return !nrf24_rxFifoEmpty();;
133 }
134
135 /* Checks if receive FIFO is empty or not */
136 uint8_t nrf24_rxFifoEmpty()
137 {
138
        uint8_t fifoStatus;
139
        nrf24_readRegister(FIF0_STATUS,&fifoStatus,1);
140
141
        return (fifoStatus & (1 << RX_EMPTY));</pre>
142
143 }
144
145 /* Returns the length of data waiting in the RX fifo */
146 uint8 t nrf24 payloadLength()
147 {
```

```
148
         uint8_t status;
149
         nrf24_csn_digitalWrite(LOW);
150
         spi transfer(R RX PL WID);
151
         status = spi_transfer(0x00);
152
         nrf24_csn_digitalWrite(HIGH);
153
         return status;
154 }
155
156 /* Reads payload bytes into data array */
157 void nrf24_getData(uint8_t* data)
158 {
159
         /* Pull down chip select */
160
         nrf24_csn_digitalWrite(LOW);
161
162
         /* Send cmd to read rx payload */
163
         spi_transfer( R_RX_PAYLOAD );
164
165
         /* Read payload */
166
         nrf24_transferSync(data,data,payload_len);
167
168
         /* Pull up chip select */
         nrf24_csn_digitalWrite(HIGH);
169
170
171
         /* Reset status register */
172
         nrf24_configRegister(STATUS,(1<<RX_DR));</pre>
173 }
174
175 /* Returns the number of retransmissions occured for the last message */
176  uint8_t nrf24_retransmissionCount()
177 {
178
         uint8_t rv;
179
         nrf24_readRegister(OBSERVE_TX,&rv,1);
180
         rv = rv \& 0x0F;
181
         return rv;
182 }
183
184 // Sends a data package to the default address. Be sure to send the correct
185 // amount of bytes as configured as payload on the receiver.
186 void nrf24_send(uint8_t* value)
187 {
188
         /* Go to Standby-I first */
         nrf24_ce_digitalWrite(LOW);
189
190
         /* Set to transmitter mode , Power up if needed */
191
192
         nrf24_powerUpTx();
193
         /* Do we really need to flush TX fifo each time ? */
194
195
         #if 1
196
             /* Pull down chip select */
            nrf24_csn_digitalWrite(LOW);
197
198
             /* Write cmd to flush transmit FIFO */
199
```

```
200
             spi_transfer(FLUSH_TX);
201
202
             /* Pull up chip select */
203
             nrf24_csn_digitalWrite(HIGH);
204
         #endif
205
206
         /* Pull down chip select */
         nrf24_csn_digitalWrite(LOW);
207
208
209
         /* Write cmd to write payload */
         spi_transfer(W_TX_PAYLOAD);
210
211
         /* Write payload */
212
213
         nrf24_transmitSync(value,payload_len);
214
         /* Pull up chip select */
215
         nrf24_csn_digitalWrite(HIGH);
216
217
         /* Start the transmission */
218
219
         nrf24_ce_digitalWrite(HIGH);
220 }
221
222 uint8_t nrf24_isSending()
223 {
224
         uint8 t status;
225
         /* read the current status */
226
         status = nrf24_getStatus();
227
228
229
         /* if sending successful (TX_DS) or max retries exceded (MAX_RT). */
230
         if((status & ((1 << TX_DS) | (1 << MAX_RT))))</pre>
231
         {
             return 0; /* false */
232
233
234
         return 1; /* true */
235
236
237 }
238
239 uint8_t nrf24_getStatus()
240 {
241
         uint8_t rv;
242
         nrf24_csn_digitalWrite(LOW);
         rv = spi_transfer(NOP);
243
244
         nrf24_csn_digitalWrite(HIGH);
245
         return rv;
246 }
247
248 uint8_t nrf24_lastMessageStatus()
249 {
250
         uint8_t rv;
251
```

```
252
         rv = nrf24_getStatus();
253
254
         /* Transmission went OK */
255
         if((rv & ((1 << TX_DS))))</pre>
256
         {
257
             return NRF24_TRANSMISSON_OK;
258
         }
         /* Maximum retransmission count is reached */
259
260
         /* Last message probably went missing ... */
261
         else if((rv & ((1 << MAX_RT))))</pre>
262
         {
263
             return NRF24_MESSAGE_LOST;
264
         }
265
         /* Probably still sending ... */
266
         else
267
         {
268
             return 0xFF;
269
         }
270 }
271
272 void nrf24_powerUpRx()
273 {
274
         nrf24 csn digitalWrite(LOW);
275
         spi_transfer(FLUSH_RX);
276
         nrf24 csn digitalWrite(HIGH);
277
         nrf24_configRegister(STATUS,(1<<RX_DR)|(1<<TX_DS)|(1<<MAX_RT));</pre>
278
279
280
         nrf24 ce digitalWrite(LOW);
281
         nrf24_configRegister(CONFIG,nrf24_CONFIG|((1<<PWR_UP)|(1<<PRIM_RX)));</pre>
         nrf24_ce_digitalWrite(HIGH);
282
283 }
284
285 void nrf24_powerUpTx()
286 {
         nrf24 configRegister(STATUS,(1<<RX DR)|(1<<TX DS)|(1<<MAX RT));</pre>
287
288
         nrf24_configRegister(CONFIG,nrf24_CONFIG|((1<<PWR_UP)|(0<<PRIM_RX)));</pre>
289
290 }
291
292 void nrf24_powerDown()
293 {
         nrf24_ce_digitalWrite(LOW);
294
295
         nrf24_configRegister(CONFIG,nrf24_CONFIG);
296 }
297
298 uint8 t spi transfer(uint8 t tx)
299 {
300
         uint8 t i = 0;
301
         uint8_t rx = 0;
302
303
         nrf24_sck_digitalWrite(LOW);
```

```
304
305
         for(i=0;i<8;i++)</pre>
306
307
308
             if(tx & (1<<(7-i)))</pre>
309
             {
310
                 nrf24_mosi_digitalWrite(HIGH);
311
             }
312
             else
313
             {
                  nrf24_mosi_digitalWrite(LOW);
314
315
             }
316
317
             nrf24_sck_digitalWrite(HIGH);
318
319
             rx = rx << 1;
320
             if(nrf24_miso_digitalRead())
321
             {
322
                  rx = 0x01;
323
             }
324
325
             nrf24_sck_digitalWrite(LOW);
326
327
         }
328
329
         return rx;
330 }
331
332 /* send and receive multiple bytes over SPI */
333 void nrf24_transferSync(uint8_t* dataout, uint8_t* datain, uint8_t len)
334 {
335
         uint8_t i;
336
337
         for(i=0;i<len;i++)</pre>
338
         {
             datain[i] = spi_transfer(dataout[i]);
339
340
         }
341
342 }
343
344 /* send multiple bytes over SPI */
345 void nrf24_transmitSync(uint8_t* dataout,uint8_t len)
346 {
347
         uint8_t i;
348
         for(i=0;i<len;i++)</pre>
349
350
351
             spi_transfer(dataout[i]);
         }
352
353
354 }
355
```

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```

```
356 /* Clocks only one byte into the given nrf24 register */
357 void nrf24_configRegister(uint8_t reg, uint8_t value)
358 {
359
        nrf24_csn_digitalWrite(LOW);
360
        spi_transfer(W_REGISTER | (REGISTER_MASK & reg));
361
        spi_transfer(value);
        nrf24 csn digitalWrite(HIGH);
362
363 }
364
365 /* Read single register from nrf24 */
366 void nrf24_readRegister(uint8_t reg, uint8_t* value, uint8_t len)
367 {
368
        nrf24 csn digitalWrite(LOW);
369
        spi transfer(R REGISTER | (REGISTER MASK & reg));
370
        nrf24_transferSync(value, value, len);
371
        nrf24_csn_digitalWrite(HIGH);
372 }
373
374 /* Write to a single register of nrf24 */
375 void nrf24_writeRegister(uint8_t reg, uint8_t* value, uint8_t len)
376 {
        nrf24_csn_digitalWrite(LOW);
377
378
        spi_transfer(W_REGISTER | (REGISTER_MASK & reg));
379
        nrf24_transmitSync(value,len);
380
        nrf24 csn digitalWrite(HIGH);
381 }
382
383 /* Check single register from nrf24 */
384 bool nrf24_checkRegister(uint8_t reg, uint8_t desiredValue, uint8_t len)
385 {
        uint8 t registerValue;
386
        nrf24_readRegister(reg,&registerValue,len);
387
388
        if (registerValue==desiredValue) { return true; } else { return false; }
389 }
390
391 #define RF DDR DDRC
392 #define RF_PORT PORTC
393 #define RF PIN PINC
394
395 #define set bit(reg,bit) reg |= (1<<bit)
396 #define clr_bit(reg,bit) reg &= ~(1<<bit)</pre>
397 #define check_bit(reg,bit) (reg&(1<<bit))</pre>
398
399 /* ------ */
400
401 void nrf24 setupPins()
402 {
403
        set_bit(RF_DDR,0); // CE output
404
        set_bit(RF_DDR,1); // CSN output
405
       set_bit(RF_DDR,2); // SCK output
       set bit(RF DDR,3); // MOSI output
406
        clr_bit(RF_DDR,4); // MISO input
407
```

```
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408 }
409 /* ----- */
410 void nrf24_ce_digitalWrite(uint8_t state)
411 {
412
      if(state)
413
      {
414
         set_bit(RF_PORT,0);
415
416
      else
417
      {
418
        clr_bit(RF_PORT,0);
419
420 }
421 /* ------*/
422 void nrf24_csn_digitalWrite(uint8_t state)
423 {
424
      if(state)
425
         set_bit(RF_PORT,1);
426
427
      }
428
      else
429
      {
         clr_bit(RF_PORT,1);
430
431
432 }
433 /* ------*/
434 void nrf24_sck_digitalWrite(uint8_t state)
435 {
436
      if(state)
437
438
         set_bit(RF_PORT,2);
439
     }
440
     else
441
      {
442
         clr_bit(RF_PORT,2);
443
444 }
445
446 void nrf24_mosi_digitalWrite(uint8_t state)
447 {
      if(state)
448
449
450
         set_bit(RF_PORT,3);
451
     }
452
      else
453
454
         clr_bit(RF_PORT,3);
455
456 }
457 /* ------*/
458 uint8_t nrf24_miso_digitalRead()
```

459 {

```
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```

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10
```

```
460
        return check_bit(RF_PIN,4);
461 }
462 /* ----- */
463
464 void nrf24_initRF_SAFE(uint8_t boardIndex,TransmissionMode initMode){
465
466
        initliazeMemory();
        bool successfulRfInit = false;
467
468
469
        while(successfulRfInit==false){
470
           nrf24_powerDown();
471
           nrf24_init();
           nrf24_config(GENERAL_RF_CHANNEL,32);
472
473
           if (nrf24_checkConfig()) { successfulRfInit = true; } else
             { faultyRF_Alarm(); }
474
        }
475
        if (initMode==TRANSMIT){
476
477
           nrf24_tx_address(CURRENT_BOARD_ADDRESS);
478
           nrf24_rx_address(BOARD_ADDRESS[boardIndex]);
479
           }else{
           nrf24_tx_address(BOARD_ADDRESS[boardIndex]);
480
481
           nrf24_rx_address(CURRENT_BOARD_ADDRESS);
482
483
        nrf24_powerUpRx();
484 }
```