```
 1
 2  #define UCPHA0 1
 3  #define F_CPU 8000000UL
 4  #define BAUD_RATE 9600UL
 5  #define UBRR_VALUE ((F_CPU)/(2UL*BAUD_RATE))-1
 6
 7  #include "nrf24.h"
 8  #include <avr/io.h>
 9
10  uint8_t payload_len;
11  uint8_t selectedChannel;
12
13  void nrf24_init()
14  {
15      nrf24_setupPins();
16      nrf24_ce_digitalWrite(LOW);
17      nrf24_csn_digitalWrite(HIGH);
18  }
19
20  void nrf24_config(uint8_t channel, uint8_t pay_length)
21  {
22      /* Use static payload length ... */
23      payload_len = pay_length;
24      selectedChannel = channel;
25      // Set RF channel
26      nrf24_configRegister(RF_CH,channel);
27      // Set length of incoming payload
28      nrf24_configRegister(RX_PW_P0, 0x00); // Auto-ACK pipe ...
29      nrf24_configRegister(RX_PW_P1, payload_len); // Data payload pipe
30      nrf24_configRegister(RX_PW_P2, 0x00); // Pipe not used
31      nrf24_configRegister(RX_PW_P3, 0x00); // Pipe not used
32      nrf24_configRegister(RX_PW_P4, 0x00); // Pipe not used
33      nrf24_configRegister(RX_PW_P5, 0x00); // Pipe not used
34      // 1 Mbps, TX gain: 0dbm
35      nrf24_configRegister(RF_SETUP, (0<<RF_DR)|((0x03)<<RF_PWR));
36      // CRC enable, 1 byte CRC length
37      nrf24_configRegister(CONFIG,nrf24_CONFIG);
38      // Auto Acknowledgment
39      nrf24_configRegister(EN_AA,(1<<ENAA_P0)|(1<<ENAA_P1)|(0<<ENAA_P2)|
          (0<<ENAA_P3)|(0<<ENAA_P4)|(0<<ENAA_P5));
40      // Enable RX addresses
41      nrf24_configRegister(EN_RXADDR,(1<<ERX_P0)|(1<<ERX_P1)|(0<<ERX_P2)|
          (0<<ERX_P3)|(0<<ERX_P4)|(0<<ERX_P5));
42      // Auto retransmit delay: 1000 us and Up to 15 retransmit trials
43      nrf24_configRegister(SETUP_RETR,(0x04<<ARD)|(0x0F<<ARC));
44      // Dynamic length configurations: No dynamic length
45      nrf24_configRegister(DYNPD,(0<<DPL_P0)|(0<<DPL_P1)|(0<<DPL_P2)|(0<<DPL_P3)|
          (0<<DPL_P4)|(0<<DPL_P5));
46
47  }
48
49  bool nrf24_checkConfig(){
```

```
50      // Check all registers
51      if (nrf24_checkRegister(RF_CH, selectedChannel,1)==false) return false;
52      if (nrf24_checkRegister(RX_PW_P0, 0x00,1)==false) return false;
53      if (nrf24_checkRegister(RX_PW_P1, payload_len,1)==false) return false;
54      if (nrf24_checkRegister(RX_PW_P2, 0x00,1)==false) return false;
55      if (nrf24_checkRegister(RX_PW_P3, 0x00,1)==false) return false;
56      if (nrf24_checkRegister(RX_PW_P4, 0x00,1)==false) return false;
57      if (nrf24_checkRegister(RX_PW_P5, 0x00,1)==false) return false;
58      if (nrf24_checkRegister(RF_SETUP, (0<<RF_DR)|((0x03)<<RF_PWR),1)==false)
          return false;
59      if (nrf24_checkRegister(CONFIG,nrf24_CONFIG,1)==false) return false;
60      if (nrf24_checkRegister(EN_AA,(1<<ENAA_P0)|(1<<ENAA_P1)|(0<<ENAA_P2)|
          (0<<ENAA_P3)|(0<<ENAA_P4)|(0<<ENAA_P5),1)==false) return false;
61      if (nrf24_checkRegister(SETUP_RETR,(0x04<<ARD)|(0x0F<<ARC),1)==false) return
          false;
62      if (nrf24_checkRegister(DYNPD,(0<<DPL_P0)|(0<<DPL_P1)|(0<<DPL_P2)|
          (0<<DPL_P3)|(0<<DPL_P4)|(0<<DPL_P5),1)==false) return false;
63
64      return true;
65  }
66
67  bool nrf24_checkAvailability(){
68      if (nrf24_checkRegister(RF_CH, selectedChannel,1)==true) { return true; }
          else { return false;}
69  }
70
71
72
73  /* Set the RX address */
74  void nrf24_rx_address(uint8_t * adr)
75  {
76      nrf24_ce_digitalWrite(LOW);
77      nrf24_writeRegister(RX_ADDR_P1,adr,nrf24_ADDR_LEN);
78      nrf24_ce_digitalWrite(HIGH);
79  }
80
81  /* Returns the payload length */
82  uint8_t nrf24_payload_length()
83  {
84      return payload_len;
85  }
86
87  /* Set the TX address */
88  void nrf24_tx_address(uint8_t* adr)
89  {
90      /* RX_ADDR_P0 must be set to the sending addr for auto ack to work. */
91      nrf24_writeRegister(RX_ADDR_P0,adr,nrf24_ADDR_LEN);
92      nrf24_writeRegister(TX_ADDR,adr,nrf24_ADDR_LEN);
93  }
94
95  /* Checks if data is available for reading */
96  /* Returns 1 if data is ready ... */
```

```
 97  uint8_t nrf24_dataReady()
 98  {
 99      // See note in getData() function - just checking RX_DR isn't good enough
100      uint8_t status = nrf24_getStatus();
101
102      // We can short circuit on RX_DR, but if it's not set, we still need
103      // to check the FIFO for any pending packets
104      if ( status & (1 << RX_DR) )
105      {
106          return 1;
107      }
108
109      return !nrf24_rxFifoEmpty();;
110  }
111
112  /* Checks if receive FIFO is empty or not */
113  uint8_t nrf24_rxFifoEmpty()
114  {
115      uint8_t fifoStatus;
116
117      nrf24_readRegister(FIFO_STATUS,&fifoStatus,1);
118
119      return (fifoStatus & (1 << RX_EMPTY));
120  }
121
122  /* Returns the length of data waiting in the RX fifo */
123  uint8_t nrf24_payloadLength()
124  {
125      uint8_t status;
126      nrf24_csn_digitalWrite(LOW);
127      spi_transfer(R_RX_PL_WID);
128      status = spi_transfer(0x00);
129      nrf24_csn_digitalWrite(HIGH);
130      return status;
131  }
132
133  /* Reads payload bytes into data array */
134  void nrf24_getData(uint8_t* data)
135  {
136      /* Pull down chip select */
137      nrf24_csn_digitalWrite(LOW);
138
139      /* Send cmd to read rx payload */
140      spi_transfer( R_RX_PAYLOAD );
141
142      /* Read payload */
143      nrf24_transferSync(data,data,payload_len);
144
145      /* Pull up chip select */
146      nrf24_csn_digitalWrite(HIGH);
147
148      /* Reset status register */
```

```
149     nrf24_configRegister(STATUS,(1<<RX_DR));
150 }
151
152 /* Returns the number of retransmissions occured for the last message */
153 uint8_t nrf24_retransmissionCount()
154 {
155     uint8_t rv;
156     nrf24_readRegister(OBSERVE_TX,&rv,1);
157     rv = rv & 0x0F;
158     return rv;
159 }
160
161 // Sends a data package to the default address. Be sure to send the correct
162 // amount of bytes as configured as payload on the receiver.
163 void nrf24_send(uint8_t* value)
164 {
165     /* Go to Standby-I first */
166     nrf24_ce_digitalWrite(LOW);
167
168     /* Set to transmitter mode , Power up if needed */
169     nrf24_powerUpTx();
170
171     /* Do we really need to flush TX fifo each time ? */
172     #if 1
173     /* Pull down chip select */
174     nrf24_csn_digitalWrite(LOW);
175
176     /* Write cmd to flush transmit FIFO */
177     spi_transfer(FLUSH_TX);
178
179     /* Pull up chip select */
180     nrf24_csn_digitalWrite(HIGH);
181     #endif
182
183     /* Pull down chip select */
184     nrf24_csn_digitalWrite(LOW);
185
186     /* Write cmd to write payload */
187     spi_transfer(W_TX_PAYLOAD);
188
189     /* Write payload */
190     nrf24_transmitSync(value,payload_len);
191
192     /* Pull up chip select */
193     nrf24_csn_digitalWrite(HIGH);
194
195     /* Start the transmission */
196     nrf24_ce_digitalWrite(HIGH);
197 }
198
199 uint8_t nrf24_isSending()
200 {
```

```
201     uint8_t status;
202
203     /* read the current status */
204     status = nrf24_getStatus();
205
206     /* if sending successful (TX_DS) or max retries exceded (MAX_RT). */
207     if((status & ((1 << TX_DS)  | (1 << MAX_RT))))
208     {
209         return 0; /* false */
210     }
211
212     return 1; /* true */
213
214 }
215
216 uint8_t nrf24_getStatus()
217 {
218     uint8_t rv;
219     nrf24_csn_digitalWrite(LOW);
220     rv = spi_transfer(NOP);
221     nrf24_csn_digitalWrite(HIGH);
222     return rv;
223 }
224
225 uint8_t nrf24_lastMessageStatus()
226 {
227     uint8_t rv;
228
229     rv = nrf24_getStatus();
230
231     /* Transmission went OK */
232     if((rv & ((1 << TX_DS))))
233     {
234         return NRF24_TRANSMISSON_OK;
235     }
236     /* Maximum retransmission count is reached */
237     /* Last message probably went missing ... */
238     else if((rv & ((1 << MAX_RT))))
239     {
240         return NRF24_MESSAGE_LOST;
241     }
242     /* Probably still sending ... */
243     else
244     {
245         return 0xFF;
246     }
247 }
248
249 void nrf24_powerUpRx()
250 {
251     nrf24_csn_digitalWrite(LOW);
252     spi_transfer(FLUSH_RX);
```

```
253     nrf24_csn_digitalWrite(HIGH);
254
255     nrf24_configRegister(STATUS,(1<<RX_DR)|(1<<TX_DS)|(1<<MAX_RT));
256
257     nrf24_ce_digitalWrite(LOW);
258     nrf24_configRegister(CONFIG,nrf24_CONFIG|((1<<PWR_UP)|(1<<PRIM_RX)));
259     nrf24_ce_digitalWrite(HIGH);
260
261     _delay_ms(5);
262 }
263
264 void nrf24_powerUpTx()
265 {
266     nrf24_configRegister(STATUS,(1<<RX_DR)|(1<<TX_DS)|(1<<MAX_RT));
267
268     nrf24_configRegister(CONFIG,nrf24_CONFIG|((1<<PWR_UP)|(0<<PRIM_RX)));
269
270     _delay_ms(5);
271 }
272
273 void nrf24_powerDown()
274 {
275     nrf24_ce_digitalWrite(LOW);
276     nrf24_configRegister(CONFIG,nrf24_CONFIG);
277
278     _delay_ms(5);
279 }
280
281 uint8_t spi_transfer(uint8_t tx)
282 {
283     uint8_t i = 0;
284     uint8_t rx = 0;
285
286     nrf24_sck_digitalWrite(LOW);
287
288     for(i=0;i<8;i++)
289     {
290
291         if(tx & (1<<(7-i)))
292         {
293             nrf24_mosi_digitalWrite(HIGH);
294         }
295         else
296         {
297             nrf24_mosi_digitalWrite(LOW);
298         }
299
300         nrf24_sck_digitalWrite(HIGH);
301
302         rx = rx << 1;
303         if(nrf24_miso_digitalRead())
304         {
```

```
305             rx |= 0x01;
306         }
307
308         nrf24_sck_digitalWrite(LOW);
309
310     }
311
312     return rx;
313 }
314
315 /* send and receive multiple bytes over SPI */
316 void nrf24_transferSync(uint8_t* dataout,uint8_t* datain,uint8_t len)
317 {
318     uint8_t i;
319
320     for(i=0;i<len;i++)
321     {
322         datain[i] = spi_transfer(dataout[i]);
323     }
324
325 }
326
327 /* send multiple bytes over SPI */
328 void nrf24_transmitSync(uint8_t* dataout,uint8_t len)
329 {
330     uint8_t i;
331
332     for(i=0;i<len;i++)
333     {
334         spi_transfer(dataout[i]);
335     }
336
337 }
338
339 /* Clocks only one byte into the given nrf24 register */
340 void nrf24_configRegister(uint8_t reg, uint8_t value)
341 {
342     nrf24_csn_digitalWrite(LOW);
343     spi_transfer(W_REGISTER | (REGISTER_MASK & reg));
344     spi_transfer(value);
345     nrf24_csn_digitalWrite(HIGH);
346 }
347
348 /* Read single register from nrf24 */
349 void nrf24_readRegister(uint8_t reg, uint8_t* value, uint8_t len)
350 {
351     nrf24_csn_digitalWrite(LOW);
352     spi_transfer(R_REGISTER | (REGISTER_MASK & reg));
353     nrf24_transferSync(value,value,len);
354     nrf24_csn_digitalWrite(HIGH);
355 }
356
```

```
357 /* Write to a single register of nrf24 */
358 void nrf24_writeRegister(uint8_t reg, uint8_t* value, uint8_t len)
359 {
360     nrf24_csn_digitalWrite(LOW);
361     spi_transfer(W_REGISTER | (REGISTER_MASK & reg));
362     nrf24_transmitSync(value,len);
363     nrf24_csn_digitalWrite(HIGH);
364 }
365
366 /* Check single register from nrf24 */
367 bool nrf24_checkRegister(uint8_t reg, uint8_t desiredValue, uint8_t len)
368 {
369     uint8_t registerValue;
370     nrf24_readRegister(reg,&registerValue,len);
371     if (registerValue==desiredValue) { return true; } else { return false; }
372 }
373
374 #define RF_DDR  DDRD
375 #define RF_PORT PORTD
376 #define RF_PIN  PIND
377
378 #define CE_CSN_DDR  DDRC
379 #define CE_CSN_PORT PORTC
380 #define CE_CSN_PIN  PINC
381
382 #define MISO_BIT_POS    0
383 #define MOSI_BIT_POS    1
384 #define SCK_BIT_POS     4
385
386 #define CE_BIT_POS      0
387 #define CSN_BIT_POS     1
388
389 #define set_bit(reg,bit) reg |= (1<<bit)
390 #define clr_bit(reg,bit) reg &= ~(1<<bit)
391 #define check_bit(reg,bit) (reg&(1<<bit))
392
393 /* ---------------------------------------------------------------------------- */
394
395 void nrf24_setupPins()
396 {
397     set_bit(CE_CSN_DDR, CE_BIT_POS); // CE output
398     set_bit(CE_CSN_DDR, CSN_BIT_POS); // CSN output
399
400     clr_bit(RF_DDR, MISO_BIT_POS); // MISO input
401     set_bit(RF_DDR, MOSI_BIT_POS); // MOSI output
402     set_bit(RF_DDR, SCK_BIT_POS); // SCK output
403 }
404 /* ---------------------------------------------------------------------------- */
405 void nrf24_ce_digitalWrite(uint8_t state)
406 {
407     if(state)
408     {
```

```
409             set_bit(CE_CSN_PORT, CE_BIT_POS);
410         }
411         else
412         {
413             clr_bit(CE_CSN_PORT, CE_BIT_POS);
414         }
415     }
416     /* ------------------------------------------------------------------------ */
417     void nrf24_csn_digitalWrite(uint8_t state)
418     {
419         if(state)
420         {
421             set_bit(CE_CSN_PORT, CSN_BIT_POS);
422         }
423         else
424         {
425             clr_bit(CE_CSN_PORT, CSN_BIT_POS);
426         }
427     }
428     /* ------------------------------------------------------------------------ */
429     void nrf24_sck_digitalWrite(uint8_t state)
430     {
431         if(state)
432         {
433             set_bit(RF_PORT, SCK_BIT_POS);
434         }
435         else
436         {
437             clr_bit(RF_PORT, SCK_BIT_POS);
438         }
439     }
440     /* ------------------------------------------------------------------------ */
441     void nrf24_mosi_digitalWrite(uint8_t state)
442     {
443         if(state)
444         {
445             set_bit(RF_PORT, MOSI_BIT_POS);
446         }
447         else
448         {
449             clr_bit(RF_PORT, MOSI_BIT_POS);
450         }
451     }
452     /* ------------------------------------------------------------------------ */
453     uint8_t nrf24_miso_digitalRead()
454     {
455         return check_bit(RF_PIN, MISO_BIT_POS);
456     }
457     /* ------------------------------------------------------------------------ */
458
```