```
1 #ifndef F_CPU
 2 #define F_CPU 16000000UL
 3 #endif
 4 #include <avr/io.h>
 5 #include <util/delay.h>
 6 #include <avr/interrupt.h>
 7 #include <stdlib.h>
 8 #include <string.h>
 9 #include <stdbool.h>
10 #include <stdint.h>
11
12 #include "nrf24.h"
13
14 void initIO();
15
16 int main(void)
17 {
18
        //sei();
                    // Interrupts on
19
        initIO();
        nrf24_initRF_SAFE(MAIN_BOARD, RECEIVE); // CONNECTION TO MAIN BOARD : GENERAL >>
          RF CHANNEL 112
21
22
       while (1)
23
            if(nrf24 dataReady())
24
25
26
                nrf24_getData(command_buffer);
27
                CommandStatus status = DecomposeMessageFromBuffer();
28
                if (status==SUCCESFUL DECOMPOSITION) { HandleAvailableCommand(); }
                  else
29
                {
30
                    bit_flip(PORTD, BIT(7)); _delay_ms(250); bit_flip(PORTD, BIT(7));
31
                }
32
            }
33
34
            if (nrf24_checkAvailability()==false) { nrf24_initRF_SAFE(MAIN_BOARD,
              RECEIVE); }
35
        }
36 }
37
38
39 void initIO(){
40
        /*
            Input/Output pin initialization
41
42
            1 : OUTPUT | 0 : INPUT | 0b76543210 Bit order
            ATTACHMENTS
43
44
                RELAY 0
                            : PD3
                                                     OUTPUT
45
                RELAY 1
                            : PD2
                                                     OUTPUT
46
                RELAY 2
                            : PD6
                                                     OUTPUT
47
                RELAY 3
                            : PD5
                                                     OUTPUT
48
                RED LED
                            : PD7
                                                     OUTPUT
49
                GREEN LED
                          : PB0
                                                     OUTPUT
```

```
...de placa de potencia\Proyecto de placa de potencia\main.c
```

```
50
           nRF24L01
51
               CE : PC0
                                                   OUTPUT
                                                   OUTPUT
               CSN : PC1
52
               MISO : PD0 (MSPIM MISO ATMEGA)
53
                                                   INPUT
               MOSI : PD1 (MSPIM MOSI ATMEGA)
54
                                                   OUTPUT
55
               SCK : PD4 (MSPIM XCK)
                                                   OUTPUT
       */
56
57
       DDRD = 0b11111110;
58
       DDRB = 0b00101001;
       DDRC = 0b11011111;
59
60 }
61
62
63
64
65
66
```

2