Schematic: Seeed SoM - STM32MP157C

SHEET	SHEET NAME
01	Title/Revision History
02	MPU_1
03	MPU_2
04	DDR3
05	eMMC
06	PMU
07	PINOUT/LED

Revision History

DATE	REVISION	DESCRIPTION
2019/05/21	Seeed SoM - STM32MP157C_v1.0_SCH_190521	Initial Release
2019/09/04	Seeed SoM - STM32MP157C_v1.01_SCH_190904	
2019/12/13	Seeed SoM - STM32MP157C_v1.01_SCH_191213	Change R5,R6 from 1k to 2k

U3A — STM32MP157CAC3 — TFBGA361_0D5_12X12X1_2MM

Left side signals:
[6,7] PA0_WKUP — AB3 PA0
[7] ETH_RX_CLK — AA4 PA1
[7] ETH_MDIO — AC3 PA2
[7] LTDC_B5 — U2 PA3
[7] DVP_HSYNC — V4 PA4
[7] LTDC_R4 — V3 PA5
[7] DVP_PCLK — AC8 PA6
[7] ETH_RX_DV — AB8 PA7
[5] MMC2_DAT4 — A13 PA8
[5] MMC2_DAT5 — A8 PA9
[7] HDMI_NRST — Y17 PA10
[7] OTG_FS_DM — AA18 PA11
[7] OTG_FS_DP — AB19 PA12
[7] MOC1 — N2 PA13
[7] MOC2 — T2 PA14
[7] DSI_LCD_BL_CTRL — C19 PA15

[7] ETH_RXD2 — AB6 PB0
[7] ETH_RXD3 — AA7 PB1
[7] QSPI_CLK — Y16 PB2 (UART4_RX)
[5] MMC2_DAT2 — A11 PB3
[5] MMC2_DAT3 — B13 PB4
[7] FDCAN2_RX — Y8 PB5
[7] HDMI_CEC — Y14 PB6
[7] DVP_VSYNC — D11 PB7
[7] LTDC_B6 — AB10 PB8
[7] DVP_D7 — B10 PB9
[7] I2S2_CK — Y3 PB10
[7] ETH_TX_EN — AB1 PB11
[7] I2S2_WS — AC5 PB12
[7] FDCAN2_TX — AA10 PB13
[5] MMC2_DAT0 — C13 PB14
[5] MMC2_DAT1 — B12 PB15

OTG_VBUS — AC19 OTG_VBUS
[7] USB1_N — AB17 USB_DM1
[7] USB1_P — AC17 USB_DP1
[7] USB2_N — AB16 USB_DM2
[7] USB2_P — AC16 USB_DP2
AB18 USB_RREF

R80 3.3K 1% R0402

Right side signals (U3A):
PC0 — AB5 — LTDC_R5 [7]
PC1 — AA6 — ETH_MDC [7]
PC2 — Y2 — ETH_TXD2 [7]
PC3 — AC7 — I2S2_SDO [7]
PC4 — AB7 — ETH_RXD0 [7]
PC5 — B14 — ETH_RXD1 [7]
PC6 — B11 — DVP_D0 [7]
PC7 — D18 — MMC2_DAT7 [5]
PC8 — D17 — SDMMC1_D0 [7]
PC9 — D15 — SDMMC1_D1 [7]
PC10 — D16 — SDMMC1_D2 [7]
PC11 — D13 — SDMMC1_D3 [7]
PC12 — K2 — SDMMC1_CK [7]
PC13 — L2 — PMIC_WAKEUP [6,7]
PC14_OSC32_IN — L1 — LSE_IN [2]
PC15_OSC32_OUT — LES_OUT [2]

PD0 — B8 — FDCAN1_RX [7]
PD1 — B9 — FDCAN1_TX [7]
PD2 — D12 — SDMMC1_CMD [7]
PD3 — D14 — DVP_D5 [7]
PD4 — B6 — GPIO_PD4 [7]
PD5 — A7 — SDMMC3_D2 [7]
PD6 — D2 — USART2_RX [7]
PD7 — D10 — SDMMC3_D3 [7]
PD8 — K3 — LTDC_B7 [7]
PD9 — B5 — LTDC_B0 [7]
PD10 — AC10 — LTDC_B3 [7]
PD11 — AA19 — QSPI_BK1_IO0 [7]
PD12 — L3 — QSPI_BK1_IO1 [7]
PD13 — J2 — DSI_TE [7]
PD14 — TIM4_CH3 [7]
PD15 — TIM4_CH4 [7]

JTMS_SWDIO — C20 — STLINK_SWDIO [7]
JTCK_SWCLK — B20 — STLINK_SWCLK [7]
JTDI — A20 — JTDI [7]
JTDO_TRACESWO — A19 — JTDO_TRACESWO [7]
NJTRST — B19 — JTRST [7]

U3B — STM32MP157CAC3 — TFBGA361_0D5_12X12X1_2MM

[7] SAI2_MCLKA — D6 PE0
[7] DVP_D3 — C8 PE1
[7] ETH_TXD3 — W1 PE2
[5] MMC2_CLK — C9 PE3
[5] DSI_RESET — D19 PE4
[5] MMC2_DAT6 — C11 PE5
[7] LTDC_G1 — C10 PE6
[7] QSPI_BK2_IO0 — AA11 PE7
[7] QSPI_BK2_IO1 — AC13 PE8
[7] QSPI_BK2_IO2 — AA9 PE9
[7] QSPI_BK2_IO3 — Y15 PE10
[7] DVP_D4 — A4 PE11
[7] GPIO_PE12 — B4 PE12
[7] DVP_D6 — A3 PE13
[7] LTDC_G0 — C6 PE14
[7] LTDC_R7 — D3 PE15

[7] SDMMC3_D0 — D8 PF0
[7] SDMMC3_CMD — A5 PF1
[7] DSI_LCD_INT — A14 PF2
[7] GPIO_PF3 — U1 PF3
[7] SDMMC3_D1 — D9 PF4
[7] USART2_TX — D7 PF5
[7] QSPI_BK1_IO3 — AA13 PF6
[7] QSPI_BK1_IO2 — AB12 PF7
[7] GPIO_PF8 — AC11 PF8
[7] SPI5_MOSI — AA14 PF9
[7] LTDC_DE — Y12 PF10
[7] SAI2_SDBm — Y10 PF11
[7] GPIO_PF12 — Y9 PF12
[7] ADC2_INP2 — Y5 PF13
[7] I2C1_SCL — AC4 PF14
[7] I2C1_SDA — Y4 PF15

Right side (U3B):
PG0 — AC2 — ETH_NRST [7]
PG1 — W1 — HDMI_INT [7]
PG2 — V2 — GPIO_PG3 [7]
PG3 — T4 — ETH_GTX_CLK [7]
PG4 — AB2 — ETH_CLK125 [7]
PG5 — Y6 — MMC2_CMD [5]
PG6 — A10 — ETH_CLK [7]
PG7 — AC14 — LTDC_CLK [7]
PG8 — AB9 — AUDIO_RST [7]
PG9 — Y13 — LTDC_B2 [7]
PG10 — AB11 — GPIO_PG11 [7]
PG11 — Y7 — LTDC_B1 [7] (UART4_TX)
PG12 — K4 — ETH_TXD0 [7]
PG13 — AA2 — ETH_TXD1 [7]
PG14 — AA1 — SDMMC3_CLK [7]
PG15 — B7

PH0_OSC_IN — P1 — HSE_IN [2]
PH1_OSC_OUT — P2 — HES_OUT [2]
PH2 — AB4 — LTDC_R0 [7]
PH3 — B3 — LTDC_R1 [7]
PH4 — A2 — I2C2_SCL [6,7]
PH5 — Y11 — I2C2_SDA [6,7]
PH6 — W4 — SPI5_CLK [7]
PH7 — D5 — SPI5_MISO [7]
PH8 — C5 — LTDC_R2 [7]
PH9 — C4 — LTDC_R3 [7]
PH10 — B2 — DVP_D1 [7]
PH11 — D1 — DVP_D2 [7]
PH12 — C3 — LTDC_R6 [7]
PH13 — LTDC_G2 [7]
PH14 — LTDC_G3 [7]
PH15 — B1 — LTDC_G4 [7]

U3C — STM32MP157CAC3 — TFBGA361_0D5_12X12X1_2MM

[7] LTDC_G5 — C1 PI0
[7] LTDC_G6 — E3 PI1
[7] LTDC_G7 — E2 PI2
[7] GPIO_PI3 — E1 PI3
[7] LTDC_B4 — E4 PI4
[7] SAI2_SCKAm — F3 PI5
[7] SAI2_SDAm — F4 PI6
[7] SAI2_FSAm — F2 PI7
[7] LPO_32k — L4 PI8
[7] LTDC_VSYNC — T1 PI9
[7] LTDC_HSYNC — P4 PI10
[7] STUSB1600_IRQOUTn — PI11

[7] SPI1_CLK — G3 PZ0
[7] SPI1_MISO — G1 PZ1
[7] SPI1_MOSI — J4 PZ2
[7] USART1_CTS — G4 PZ3
[7] GPIO_PZ4 — G2 PZ4
[7] USART1_RTS — H2 PZ5
[7] USART1_RX — H1 PZ6
[7] USART1_TX — J3 PZ7

[7] BOOT0 — N1 BOOT0
[7] BOOT1 — N4 BOOT1
[7] BOOT2 — M2 BOOT2

Right side (U3C):
DSI_D0P — C15 — DSI_D0_P [7]
DSI_D0N — B15 — DSI_D0_N [7]
DSI_D1P — B17 — DSI_D1_P [7]
DSI_D1N — A17 — DSI_D1_N [7]
DSI_CKP — B16 — DSI_CK_P [7]
DSI_CKN — A16 — DSI_CK_N [7]

ANA0 — U3 — ADC1_INN1 [7]
ANA1 — U4 — ADC1_INP1 [7]

PWR_ON — R2 — PWR_ON [2,6,7]
NRST — M3 — NRST [5,6,7]

PWR_LP — N3
PDR_ON — R3
PDR_ON_CORE — T3
NRST_CORE — M4 — C105 10nF C0402 50V,X7R

BYPASS_REG1V8 — AB13 — R81 0R R0402 5% DNP — VDD
R82 0R R0402 5%

TP101

VDD
R83 0R R0402 5% — R84 0R R0402 5%
R85 0R R0402 5% DNP — R86 0R R0402 5% DNP

OSC1 — X4-SMD-3_2X2_5X1_0MM
VDD
R87 10R R0402 1%
C106 10nF C0402 50V,X7R
C107 6.8pF DNP C0402 50V,C0G
24MHz 6.8pF
VDD — CLK (3)
EN — GND (2)
R4 0R R0402 5% — HSE_IN [2]
C108 6.8pF DNP 50V,C0G C0402

R89 1K R0402 5%
[2,6,7] PWR_ON — R88 10K R0402 5%
R90 0R R0402 5% DNP — HES_OUT [2]
VDD — R1 10K DNP R0402 5%

X1 — X2_SMD_3_2X1_5MM
[2] LSE_IN — R2 0R R0402 5% — X1 32.768kHz 12.5pF — R79 0R R0402 5% — LES_OUT [2]
C109 6.8pF 50V,C0G C0402
C110 6.8pF 50V,C0G C0402

Left component U3E (STM32MP157CAC3, TFBGA361_0D5_12X12X1_2MM)

Left-side DDR data/strobe pins:

Pin	Signal	Net
E22	DDR_DQ0	[4] DDR_D0
F22	DDR_DQ1	[4] DDR_D1
H21	DDR_DQ2	[4] DDR_D2
E21	DDR_DQ3	[4] DDR_D3
J21	DDR_DQ4	[4] DDR_D4
J22	DDR_DQ5	[4] DDR_D5
H22	DDR_DQ6	[4] DDR_D6
G21	DDR_DQ7	[4] DDR_D7
G22	DDR_DQS0P	[4] DDR_DQS0
G23	DDR_DQS0N	[4] DDR_DQSN0
H23	DDR_DQM0	[4] DDR_DQM0
T21	DDR_DQ8	[4] DDR_D8
U21	DDR_DQ9	[4] DDR_D9
T22	DDR_DQ10	[4] DDR_D10
W21	DDR_DQ11	[4] DDR_D11
W23	DDR_DQ12	[4] DDR_D12
T23	DDR_DQ13	[4] DDR_D13
W22	DDR_DQ14	[4] DDR_D14
Y21	DDR_DQ15	[4] DDR_D15
U22	DDR_DQS1P	[4] DDR_DQS1
U23	DDR_DQS1N	[4] DDR_DQSN1
V22	DDR_DQM1	[4] DDR_DQM1
B22	DDR_DQ16	
D22	DDR_DQ17	
D23	DDR_DQ18	
B21	DDR_DQ19	
A21	DDR_DQ20	
E23	DDR_DQ21	
D21	DDR_DQ22	
A22	DDR_DQ23	
C22	DDR_DQS2P	
B23	DDR_DQS2N	
C23	DDR_DQM2	
Y23	DDR_DQ24	
Y22	DDR_DQ25	
AB21	DDR_DQ26	
AB20	DDR_DQ27	
AC22	DDR_DQ28	
AC21	DDR_DQ29	
AA23	DDR_DQ30	
AA22	DDR_DQ31	
AB22	DDR_DQS3P	
AB23	DDR_DQS3N	
AA20	DDR_DQM3	

Right-side pins of U3E:

Pin	Signal	Net
N22	DDR_CLKP	DDR_CLK [4]
N23	DDR_CLKN	DDR_CLKn [4]
L20	DDR_A0	DDR_A0 [4]
P22	DDR_A1	DDR_A1 [4]
J20	DDR_A2	DDR_A2 [4]
K22	DDR_A3	DDR_A3 [4]
V20	DDR_A4	DDR_A4 [4]
H20	DDR_A5	DDR_A5 [4]
W20	DDR_A6	DDR_A6 [4]
E20	DDR_A7	DDR_A7 [4]
Y20	DDR_A8	DDR_A8 [4]
G20	DDR_A9	DDR_A9 [4]
R22	DDR_A10	DDR_A10 [4]
R20	DDR_A11	DDR_A11 [4]
P23	DDR_A12	DDR_A12 [4]
F20	DDR_A13	DDR_A13 [4]
R21	DDR_A14	DDR_A14 [4]
P20	DDR_A15	DDR_A15 [4]
L23	DDR_BA0	DDR_BA0 [4]
U20	DDR_BA1	DDR_BA1 [4]
M21	DDR_BA2	DDR_BA2 [4]
N21	DDR_RASN	DDR_RASn [4]
N20	DDR_CASN	DDR_CASn [4]
M22	DDR_CSN	DDR_CSn [4]
T20	DDR_CKE	DDR_CKE [4]
M20	DDR_WEN	DDR_WEn [4]
L22	DDR_ODT	DDR_ODT [4]
D20	DDR_RESETN	DDR_RESETn [4]
AC20	DDR_VREF	VREF_DDR
K23	DDR_ZQ	
Y19	DDR_ATO	TP102
K20	DDR_DTO0	TP103
L21	DDR_DTO1	TP104

C27 100nF C0402 16V,X7R
R10 240R R0402 1%

Right component U3D (STM32MP157CAC3, TFBGA361_0D5_12X12X1_2MM)

VDD_CORE — VDDCORE1..VDDCORE20
VDD1..VDD6
VDDQ_DDR1..VDDQ_DDR10
VSS1..VSS54
VBAT, VDD_OTP, VDDA, VREF+, VSSA, VDD_ANA, VDD_DSI
VDDA1V1_REG, VDDA1V8_REG, VDDA1V8_DSI
VDD1V2_DSI_PHY, VDD1V2_DSI_REG
VDD3V3_USBHS, VDD3V3_USBFS
VSS_ANA, VSS_DSI, VSS_USBHS
VREF-, R4

Decoupling capacitors

VDD_CORE:
C28 C29 C30 C31 C32 C33 C34 C35 C120 C121 — 1uF 10V,X5R C0402

VDD:
C36 C37 C38 C39 C40 C41 — 1uF 10V,X5R C0402

VDDQ_DDR:
C42 C43 C44 C45 C132 — 1uF 10V,X5R C0402

R3 0R R0402 5% DNP
C133 100nF C0402 16V,X7R
R12 0R R0402 5% L5 4.7uH L0603 80mA LQM18FN4R7M00D
C134 100nF C0402 16V,X7R
R93 0R R0402 5% DNP
R94 0R R0402 5% DNP
C46 1uF 10V,X5R C0402   C47 1uF 10V,X5R C0402
C48 1uF C0402 10V,X5R
R95 0R R0402 5% DNP
C137 100nF 16V,X7R C0402   C138 1uF 10V,X5R C0402
C50 100nF 16V,X7R C0402   C49 1uF 10V,X5R C0402
C142 100nF 16V,X7R C0402   C51 1uF 10V,X5R C0402
C52 100nF 16V,X7R C0402

Power rails: VDD_CORE, VDD, VDDQ_DDR, VBAT, VDDA, VREF+, VDD_USB

DDR3L SDRAM

4Gb DDR3

MT41K256M16TW-107:P
BGA96_T9_P8_9X14

eMMC
4GB

Layout Note:

Place R134 C179 Close To MPU.

[2] MMC2_DAT0
[2] MMC2_DAT1
[2] MMC2_DAT2
[2] MMC2_DAT3
[2] MMC2_DAT4
[2] MMC2_DAT5
[2] MMC2_DAT6
[2] MMC2_DAT7
[2] MMC2_CMD
[2] MMC2_CLK
[2,6,7] NRST

U8
EMMC04G-M627
BGA153_P14_P5_11P5X13

Title:
Seeed SoM - STM32MP157C

Size: A3
Document Number: 05 eMMC
Rev: v1.01

Draw By: weifeng
Date: Thursday, September 12, 2019
Sheet: 5 of 7

5V_VIN

Layout Note: 5V_VIN 3A

U2

Pin	Signal		Signal	Pin
8	BUCK1IN	VOUT1	5	
6	PGND1	VLX1	7	
12	BUCK2IN	VOUT2	9	
10	PGND2	VLX2	11	
28	BUCK3IN	VOUT3	31	
30	PGND3	VLX3	29	
24	BUCK4IN	VOUT4	27	
26	PGND4	VLX4	25	
33	VLXBST	BSTOUT	34	
32	PGND5	VBUSOTG	35	
37	SWIN	SWOUT	38	
15	GNDLDO	VREF	16	
13	LDO3IN	LDO3OUT	14	
22	LDO16IN	LDO1OUT	23	
19	LDO25IN	LDO6OUT	21	
36	VIN	LDO2OUT	18	
42	VIO	LDO5OUT	20	
3	SDA	AGND	41	
4	SCL	INTLDO	40	
44	PWRCTRL			
1	RSTN	LDO4OUT	39	
2	WAKEUP	INTN	43	
17	PONKEYN	EPGND	45	

STPMIC1APQR
WFQFN44_0D4_5X6X0_8MM

C186 10uF C0603 10V,X5R
C187 10uF C0603 10V,X5R
C188 10uF C0603 10V,X5R
C189 10uF C0603 10V,X5R

R149 0R R0402 5%
L8 1uH L2016 2.05A WPN201610H1R0MT
C190 10uF C0603 10V,X5R

R150 0R R0402 5%

BST_OUT

Layout Note: BST_OUT 1A

VDD   5V_VIN   3V3   VDDQ_DDR

C191 10uF C0603 10V,X5R
C192 1uF   C0402 10V,X5R
C193 1uF   C0402 10V,X5R
C194 4.7uF C0402 6.3V,X5R
C195 4.7uF DNP C0402 6.3V,X5R

VDD

R152 4.7K 5% R0402
R151 4.7K 5% R0402

[2,7] I2C2_SDA
[2,7] I2C2_SCL
[2,7] PWR_ON
[2,5,7] NRST

R153 0R R0402 5%

[2,7] PMIC_WAKEUP
[7] PONKEYN

[2,7] PA0_WKUP

VDD_CORE
L9 1uH L2016 2.05A WPN201610H1R0MT
R154 0R 1% R0603
C196 22uF C0805 6.3V,X5R
Defaut Output:1.2V

VDDQ_DDR
L10 1uH L2016 2.05A WPN201610H1R0MT
C197 22uF C0805 6.3V,X5R
Defaut Output:1.1V

VDD
L11 1uH L2016 2.05A WPN201610H1R0MT
C198 22uF C0805 6.3V,X5R
Defaut Output:3.3V

3V3
L12 1uH L2016 2.05A WPN201610H1R0MT
C199 22uF C0805 6.3V,X5R
Defaut Output:3.3V

C200 22uF C0805 6.3V,X5R
BST_OUT Defaut Output:5.2V

R155 0R R0402 5%
VBUS_OTG

R156 0R R0402 5%
VBUS_SW

Defaut Output:VOUT2/2

Defaut Output:0.675V
Defaut Output:1.8V
Defaut Output:1.2V
Defaut Output:3.3V
Defaut Output:2.9V

Defaut Output:3.3V

VREF_DDR   VTT_DDR   1V8_AUDIO   1V2_HDMI   3V3_HDMI   VDDA   VDD_USB

Layout Note:
VDD_CORE	1~1.5A
VDDQ_DDR	1A
VDD	500mA
3V3	2A
BST_OUT	1A
VBUS_OTG	500mA
VBUS_SW	1A
VREF_DDR	100mA
VTT_DDR	200mA
1V8_AUDIO	350mA
1V2_HDMI	200mA
3V3_HDMI	350mA
VDDA	350mA
VDD_USB	100mA

C201 1uF 10V,X5R C0402
C202 10uF 10V,X5R C0603
C203 4.7uF 6.3V,X5R C0402
C204 4.7uF 6.3V,X5R C0402
C205 4.7uF 6.3V,X5R C0402
C206 4.7uF 6.3V,X5R C0402
C207 4.7uF 6.3V,X5R C0402
C208 4.7uF 6.3V,X5R C0402

J1 — DF40C-70DP-0.4V(51) BTB2X35_0D4_15_52x1_85x1_14mm

Half-Duplex Master

Left net	Pin	Pin	Right net
[2] I2S2_CK			
[2] I2S2_WS			
[2] I2S2_SDO			
QSPI_BK1_NCS			
[2] HDMI_CEC			
[2] HDMI_INT	OTG_FS_ID		
[2] HDMI_NRST			
[2] LTDC_B7	I2C4_SCL		
[2] LTDC_B6			
[2] LTDC_B5			
[2] LTDC_B4	SAI2_SDBm		
[2] LTDC_B3			
[2] LTDC_B2			
[2] LTDC_B1			
[2] LTDC_B0	I2S2_SDI		
[2] LTDC_G7	DVP_D8		
[2] LTDC_G6			
[2] LTDC_G5			
[2] LTDC_G4	DVP_D11		
[2] LTDC_G3	FDCAN1_RX		
[2] LTDC_G2	FDCAN1_TX		
[2] LTDC_G1			
[2] LTDC_G0			
[2] LTDC_R7	I2C4_SDA		
[2] LTDC_R6	QSPI_BK2_NCS		
[2] LTDC_R5	DAC1_OUT2		
[2] LTDC_R4			
[2] LTDC_R3			
[2] LTDC_R2			
[2] LTDC_R1			
[2] LTDC_R0	DVP_D13		
[2] LTDC_CLK	QSPI_CLK		
[2] LTDC_DE			
[2] LTDC_HSYNC			
[2] LTDC_VSYNC			

Layout Note: The LTCD signals must be length-matched

Right side (J1):
ETH_RXD0 [2], ETH_RXD1 [2], ETH_RXD2 [2], ETH_RXD3 [2], ETH_RX_DV [2], ETH_CLK125 [2], ETH_RX_CLK [2]
ETH_GTX_CLK [2], ETH_TXD0 [2], ETH_TXD1 [2], ETH_TXD2 [2], ETH_TXD3 [2], ETH_TX_EN [2]
ETH_MDC [2], ETH_MDIO [2]
ETH_NRST [2], ETH_MDINT [2], ETH_CLK [2]
DVP_D0 [2], DVP_D1 [2], DVP_D2 [2], DVP_D3 [2], DVP_D4 [2], DVP_D5 [2], DVP_D6 [2], DVP_D7 [2]
DVP_HSYNC [2], DVP_VSYNC [2], DVP_PCLK [2], MOC1 [2], GPIO_PE12 [2]

Layout Note:
The RGMII signals must be length-matched by RX,TX and MDC groups

Layout Note:
The DCMI signals must be length-matched

J2 — DF40C-70DP-0.4V(51) BTB2X35_0D4_15_52x1_85x1_14mm

Left side (J2):
[2] USART2_RX, [2] USART2_TX
[2] BOOT0, [2] BOOT1, [2] BOOT2
[2] SAI2_SCKAm, [2] SAI2_FSAm, [2] SAI2_SDAm, [2] SAI2_MCLKA, [2] SAI2_SDBm, [2] AUDIO_RST
[2] SDMMC1_D0, [2] SDMMC1_D1, [2] SDMMC1_D2, [2] SDMMC1_D3, [2] SDMMC1_CMD, [2] SDMMC1_CK, [2] GPIO_PI3
[2] DSI_D1_N, [2] DSI_D1_P
[2] DSI_CK_N, [2] DSI_CK_P
[2] DSI_D0_N, [2] DSI_D0_P
[2] DSI_LCD_INT, [2] DSI_TE, [2] DSI_LCD_BL_CTRL, [2] DSI_RESET

DVP_D12, DVP_D10, DVP_D9, SPI1_NSS

Right side (J2):
OTG_FS_DP [2], OTG_FS_DM [2]
STUSB1600_IRQOUTn [2], OTG_VBUS
QSPI_BK1_IO0 [2], QSPI_BK1_IO1 [2], QSPI_BK1_IO2 [2], QSPI_BK1_IO3 [2]
QSPI_BK2_IO0 [2], QSPI_BK2_IO1 [2], QSPI_BK2_IO2 [2], QSPI_BK2_IO3 [2], QSPI_CLK [2]
SPI5_NSS, UART4_RX
I2C2_SCL [2,6], I2C2_SDA [2,6]
SPI1_MOSI [2], SPI1_MISO [2], SPI1_CLK [2]
SPI5_MOSI [2], SPI5_MISO [2], SPI5_CLK [2]
LPO_32k [2], USART1_TX [2], USART1_RX [2], USART1_CTS [2], USART1_RTS [2]
SDMMC3_D0 [2], SDMMC3_D1 [2], SDMMC3_D2 [2], SDMMC3_D3 [2], SDMMC3_CMD [2], SDMMC3_CK [2]

WiFi/BLE Interface

Layout Note:
Differential impedance:90 Ohm

Layout Note: The SDMMC1 signals must be length-matched

Layout Note:Differential impedance:100 Ohm

Layout Note:
The SDMMC3 signals must be length-matched

LED section

3V3

VDD — R7 R0402 1K DNP — LED1 Red led0402 — 1 2
R6 R0402 2K 5%

Power LED

LED2 Blue led0402
[2] GPIO_PG3 — R5 R0402 2K 5% — 1 2

State LED

J4 — DF40C-70DP-0.4V(51) BTB2X35_0D4_15_52x1_85x1_14mm

3V3_HDMI 1V2_HDMI 1V8_AUDIO BST_OUT 5V_VIN   3V3 VDD VBUS_OTG VBUS_SW VBAT

Left side (J4):
VREF+
[2] ADC2_INP2
[2] ADC1_INN1
[2] ADC1_INP1
[2] MOC2
[2] GPIO_PZ4
[2] GPIO_PD4
[2] GPIO_PF12
[2] GPIO_PF8
[2] GPIO_PF3
[2] GPIO_PG11
[2] USB1_N, [2] USB1_P
[2] USB2_N, [2] USB2_P

SPI5_MISO, UART4_TX, GPIO_PG3

Right side (J4):
I2C1_SCL [2], I2C1_SDA [2]
TIM4_CH3 [2], TIM4_CH4 [2]
PWR_ON [2,6]
PMIC_WAKEUP [2,6]
PA0_WKUP [2,6]
PONKEYN [6]
NRST [2,5,6]
STLINK_SWDIO [2], STLINK_SWCLK [2]
JTDI [2], JTDO_TRACESWO [2], JTRST [2]
FDCAN2_RX [2], FDCAN2_TX [2]
I2C6_SDA, I2C6_SCL
FDCAN1_RX [2], FDCAN1_TX [2]

Layout Note:Wire according to the differential signal

Layout Note:
Differential impedance:90 Ohm

Headers

J5 — Header 1P — PTH_2mm_3D4
J6 — Header 1P — PTH_2mm_3D4
J7 — Header 1P — PTH_2mm_3D4