Multi -threading

Part 1

Three basic techniques of computer systems design

- Locality of access
- Parallelism
- Speculation/prediction

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- Good for software: Users got “free” performance just by buying a new chip
  - No change needed to the program (same ISA)
  - Higher frequency (smaller, faster transistors)
  - Higher IPC (different micro-arch)
  - But this was not sustainable…

Implicit parallelism not enough

- OoO superscalars extract ILP from sequential programs
  - Hardly more than 1-2 IPC on real workloads
- In practice, IPC is limited by:
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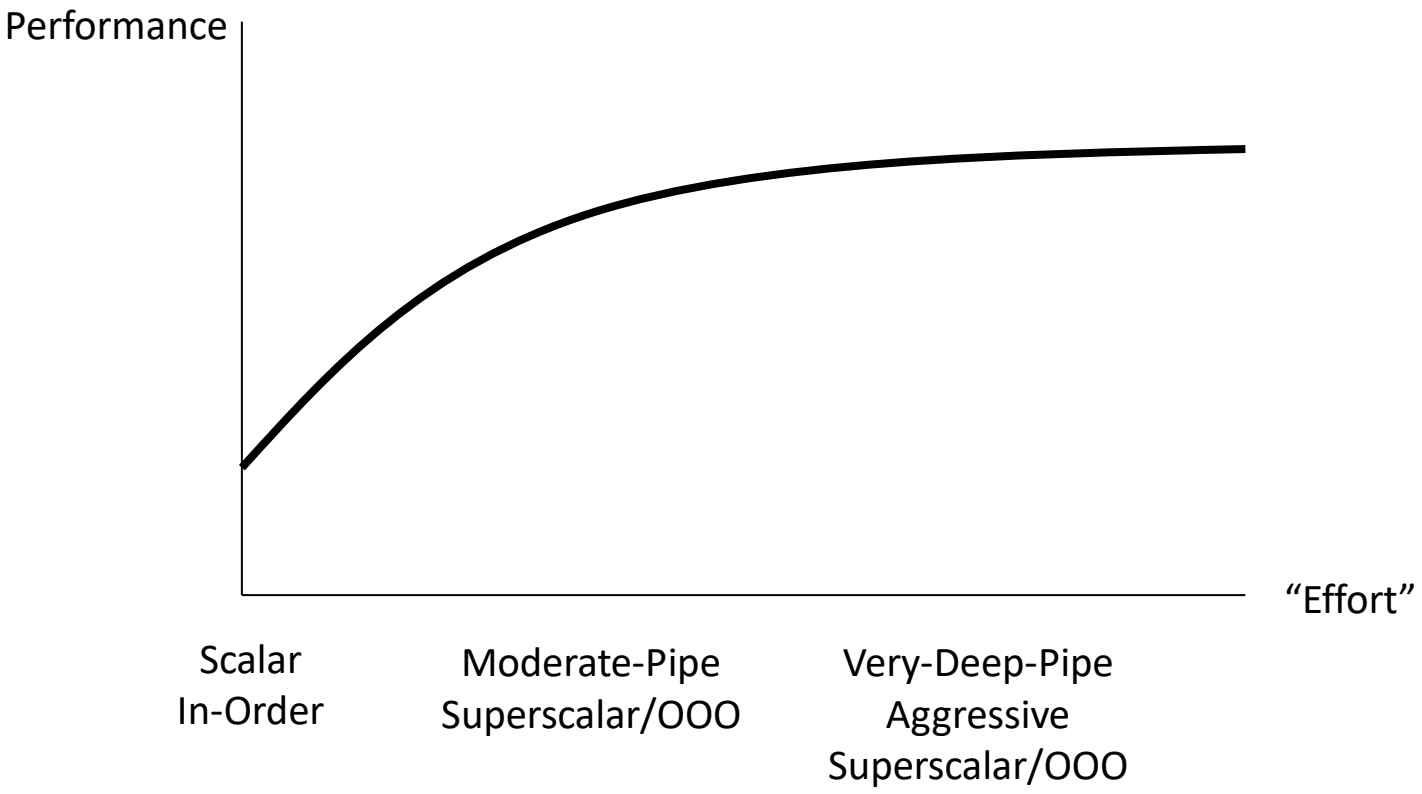
    - # ROB, RS and LSQ entries, functional units
  - Branch prediction accuracy
  - Imperfect memory disambiguation

Implicit parallelism not enough

- To get more performance, we can keep pushing IPC and/or frequency
  - Design complexity (time to market)
  - Cooling (cost)
  - Power delivery (cost)
  - …
- But it is too costly for the marginal improvements gained

Diminishing return on more complexity



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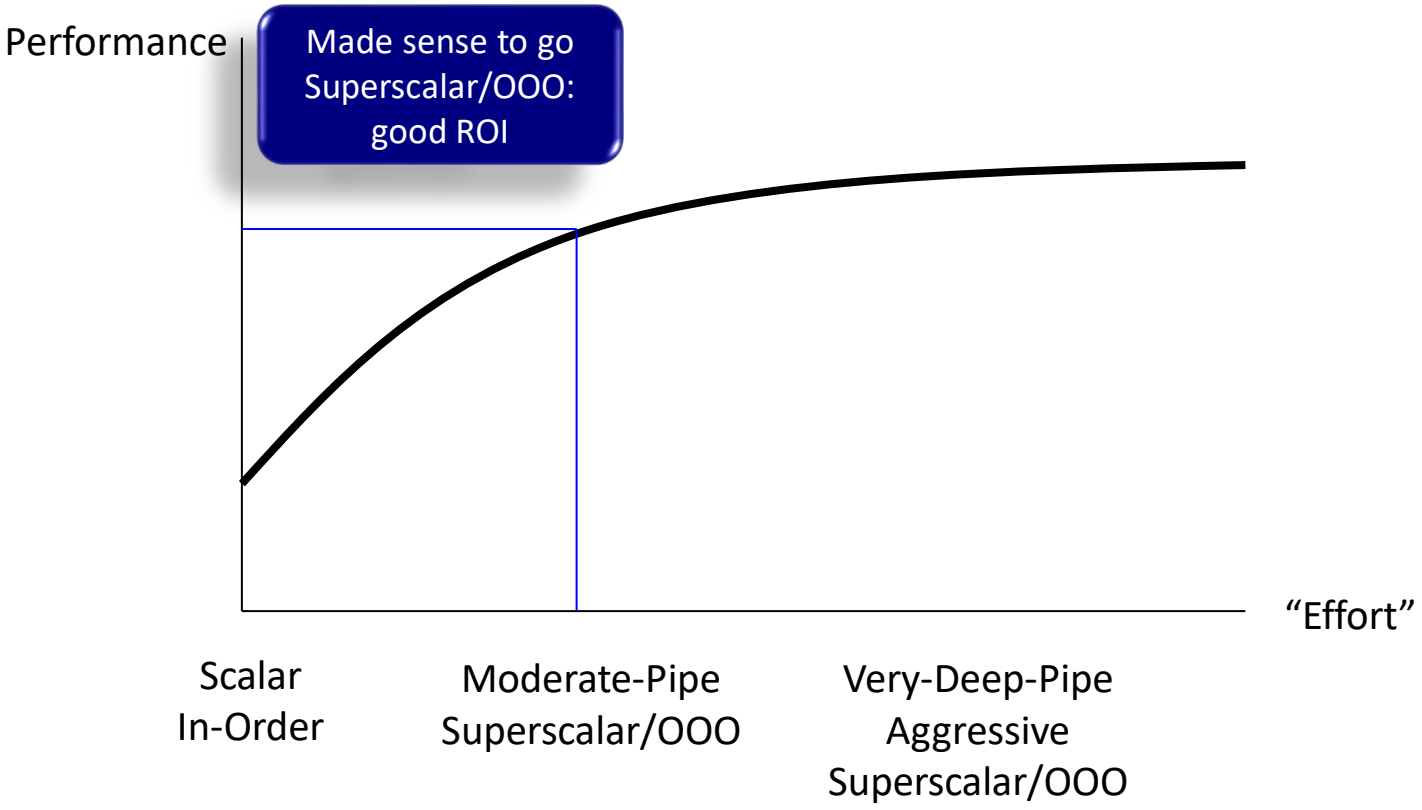

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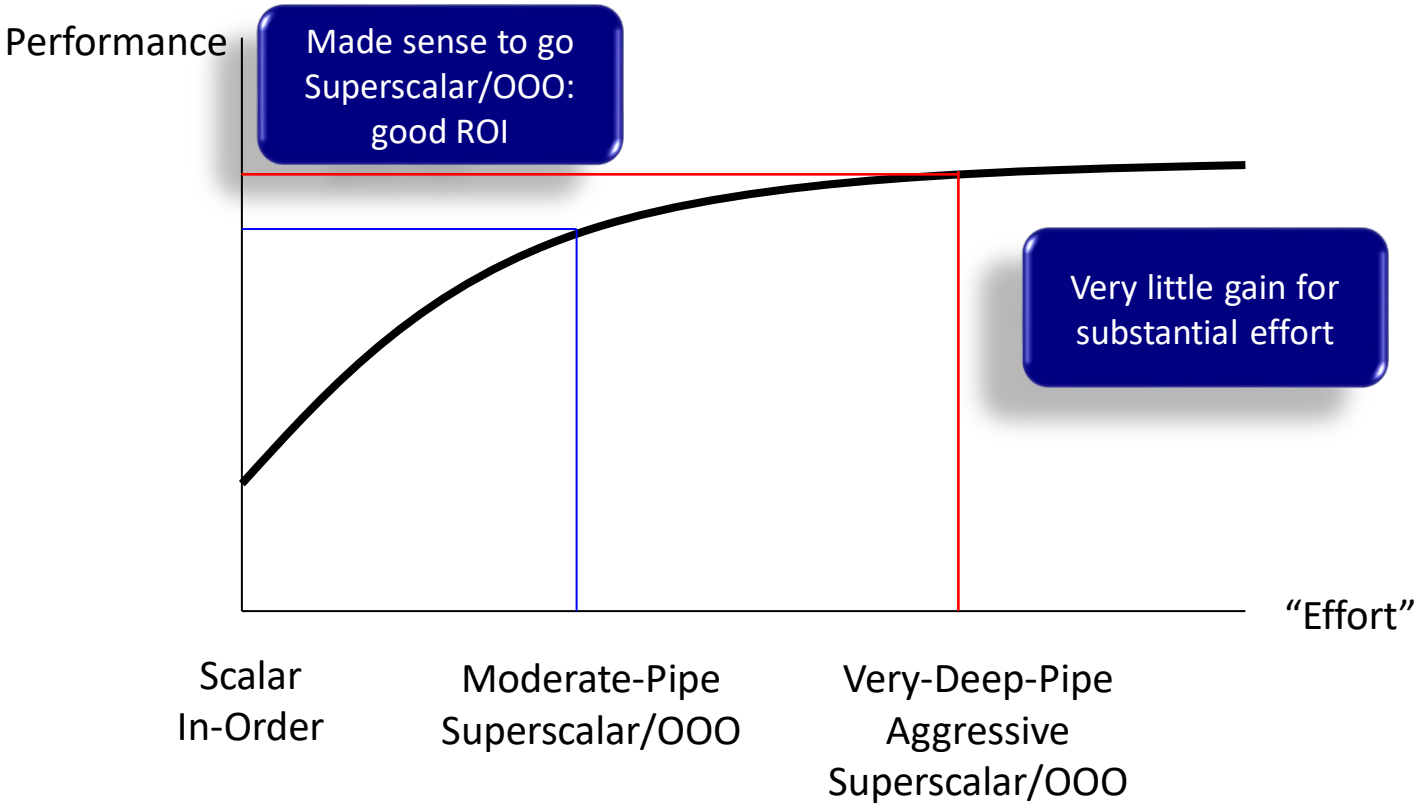

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- Adding more functional units (e.g., ALU) is relatively easy
  - Floating point units are more costly but transistors have been becoming smaller and cheaper

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- Adding more functional units (e.g., ALU) is relatively easy
  - Floating point units are more costly but transistors have been becoming smaller and cheaper
- The challenge is in finding enough parallelism in keeping all of them busy at a time
  - Almost impossible beyond a point, if there is a single sequential stream of instructions.

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- Common forms
  - ***Thread-Level Parallelism (TLP)***: Hardware Multithreading, Multiprocessors
  - ***Data-Level Parallelism (DLP)***: Vector processors, SIMD extensions, GPUs
  - ***Request-Level Parallelism (RLP)***: Data centers

Sources of TLP

- Different applications
  - MP3 player in background while you work in Office
  - Other background tasks: OS/kernel, virus check, etc…
  - Piped applications
    - gunzip -c foo.gz | grep bar | perl some-script.pl

Multiprogramming

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  - MP3 player in background while you work in Office
  - Other background tasks: OS/kernel, virus check, etc…
  - Piped applications
    - gunzip -c foo.gz | grep bar | perl some-script.pl
- Threads within the same application
  - Explicitly coded multi-threading
    - pthreads
  - Parallel languages and libraries
    - OpenMP, Cilk, TBB, etc…

Multiprogramming

Multi-threading

Architectures to Exploit TLP

- ***Hardware Multithreading (MT)***: Multiple threads **share the same processor** pipeline
  - Coarse-grained MT (CGMT)
  - Fine-grained MT (FMT)
  - Simultaneous MT (SMT)

Architectures to Exploit TLP

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- ***Multiprocessors (MP):*** Different threads run on **different processors**
  - Multiple processor chips
  - Chip Multiprocessors (CMP), a.k.a. Multicore processors
  - A combination of the above

Latency vs Throughput

- **MT trades (single-thread) latency for throughput**
  - – Sharing processor degrades latency of individual threads
  - + But improves aggregate throughput
  - + Improves utilization
- Example
  - Thread A: individual latency=10s, latency with thread B=15s
  - Thread B: individual latency=20s, latency with thread A=25s
  - Sequential latency (first A then B or vice versa): 30s
  - Parallel latency (A and B simultaneously): 25s
  - – MT slows each thread by 5s
  - + But finishes both work 5s earlier
- **Different workloads have different parallelism**
  - SpecFP has lots of ILP (can even use an 8-wide machine)
  - Server workloads have TLP (can use multiple threads)

MT Implementations: Sharing

- How do multiple threads share a single processor?
  - Different sharing mechanisms for different kinds of structures
  - Depend on what kind of state structure stores

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- **No state**: ALUs
  - Dynamically shared
- **Persistent hard state (aka "context")**: PC, registers
  - Anything exposed to the s/w
  - Replicated
- **Persistent soft state**: caches, branch predictor
  - Dynamically partitioned (like on a multi-programmed uni-processor)
    - TLBs need ASIDs, caches/bpred tables don't
  - Exception: **ordered "soft" state** (BHR, RAS) is replicated
- **Transient state**: ROB, RS
  - Partitioned … somehow (will see later)

MT Implementations: New design issues

- Main question: **thread scheduling policy**
  - When to switch from one thread to another?
- Related question: **pipeline partitioning**
  - How exactly do threads share the pipeline itself?

- Choice depends on
  - What kind of latencies you want to tolerate
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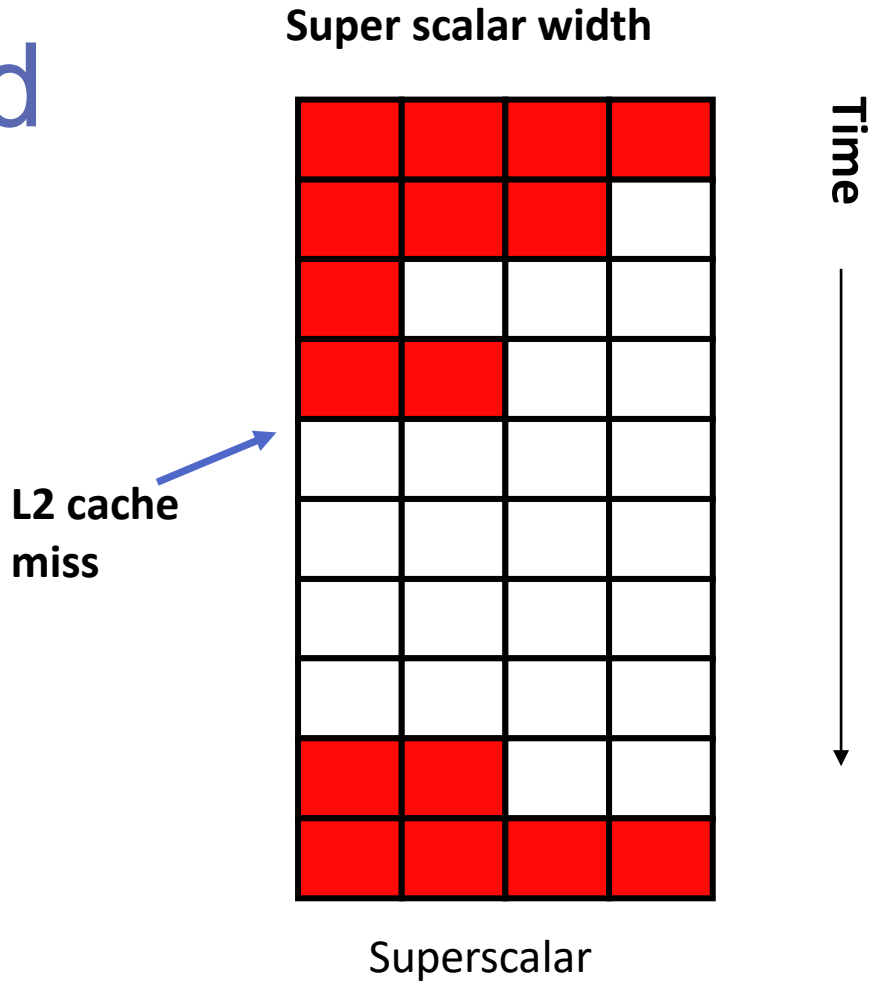
- Three designs
  - Coarse-grain multithreading (CGMT)
  - Fine-grain multithreading (FGMT)
  - Simultaneous multithreading (SMT)

Thread 1 Thread 2

Coarse -Grained Multithreading

- The OS should have already scheduled both threads on the CPU
  - **But only one thread in the pipeline at any time**
- Hardware switches to another thread when current thread stalls on a long latency event
  - E.g., L2 miss
- Example: IBM Northstar/Pulsar



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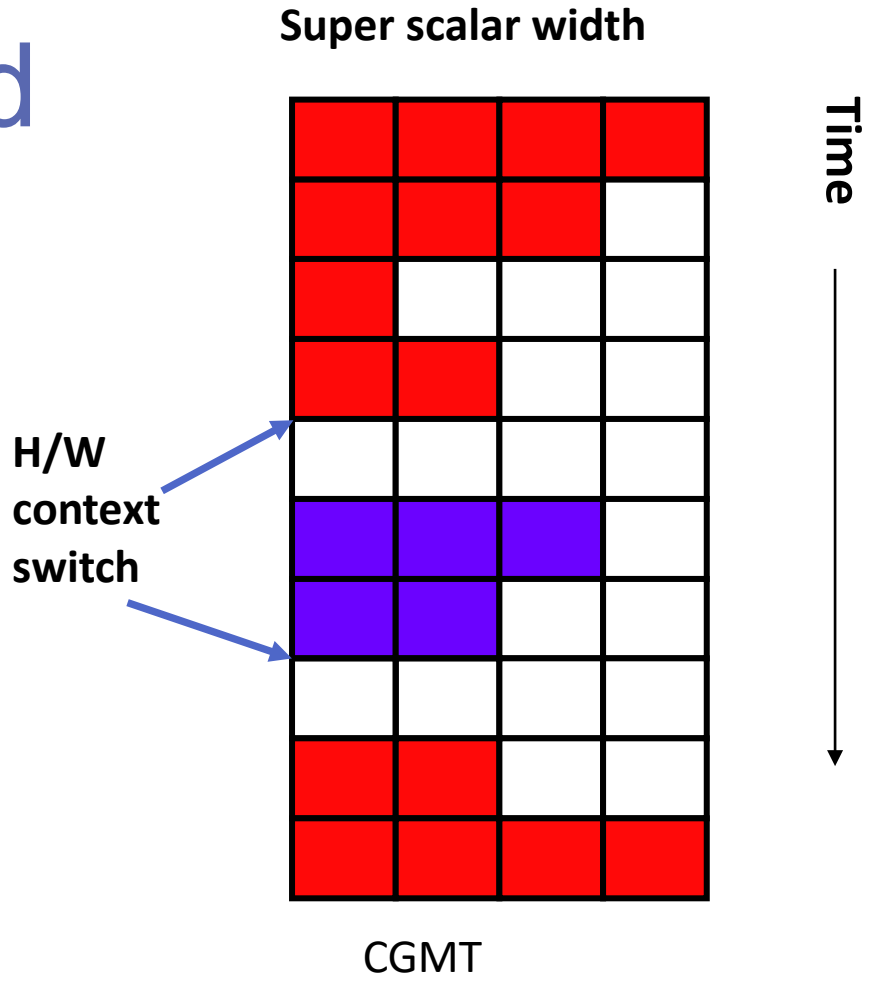
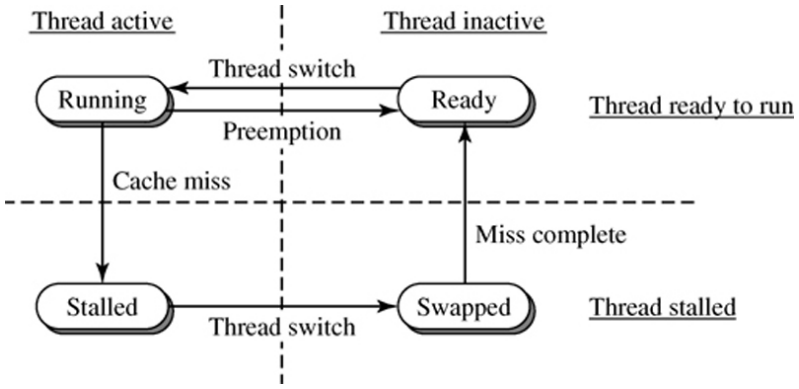


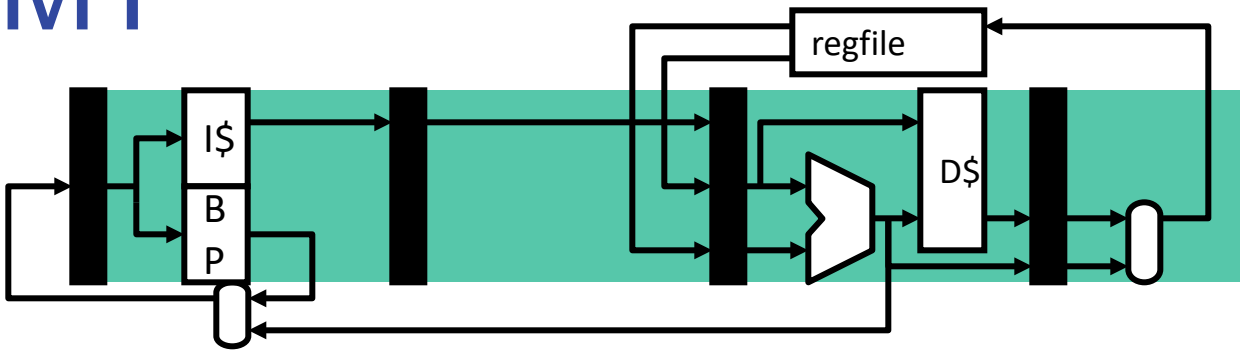
Coarse -Grained Multithreading

- Needs HW “preemption” and “priority” mechanisms to ensure fairness and high utilization
  - Different from OS preemption and priority
  - e.g., HW “preempts” long running threads with no L2 miss
  - High “priority” means thread should not be preempted
    - e.g., when in a critical section
    - Priority changes communicated using special instructions

Thread State Transition Diagram in a CGMT Processor

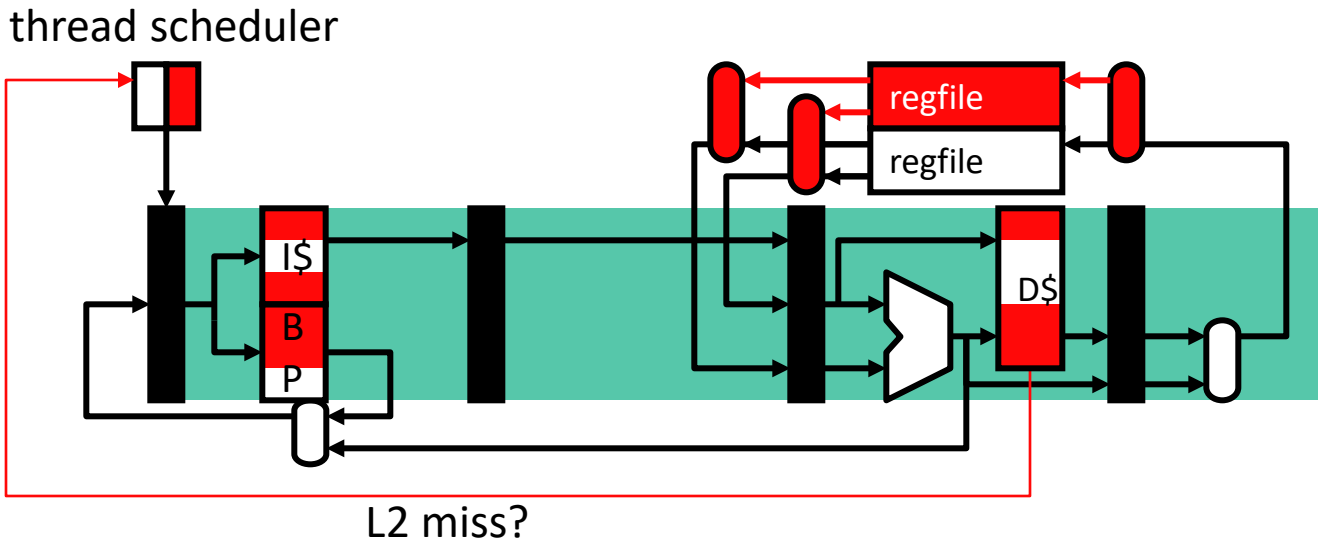


CGMT



Normal pipeline

- CGMT



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- ✗ Tolerates only long latencies (e.g., L2 misses)
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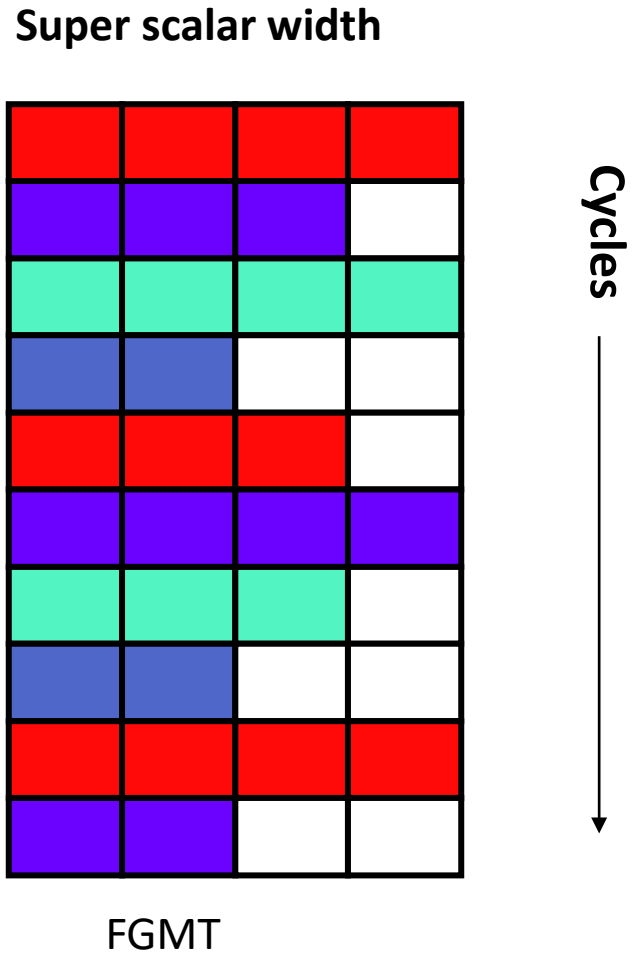
What is the advantage over OS context switch?

Fine -Grained Multithreading

- Every cycle, a different thread fetches and issues instructions
  - Irrespective of whether there is any stall
- (Many) more threads
- **Multiple threads in pipeline at once**



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