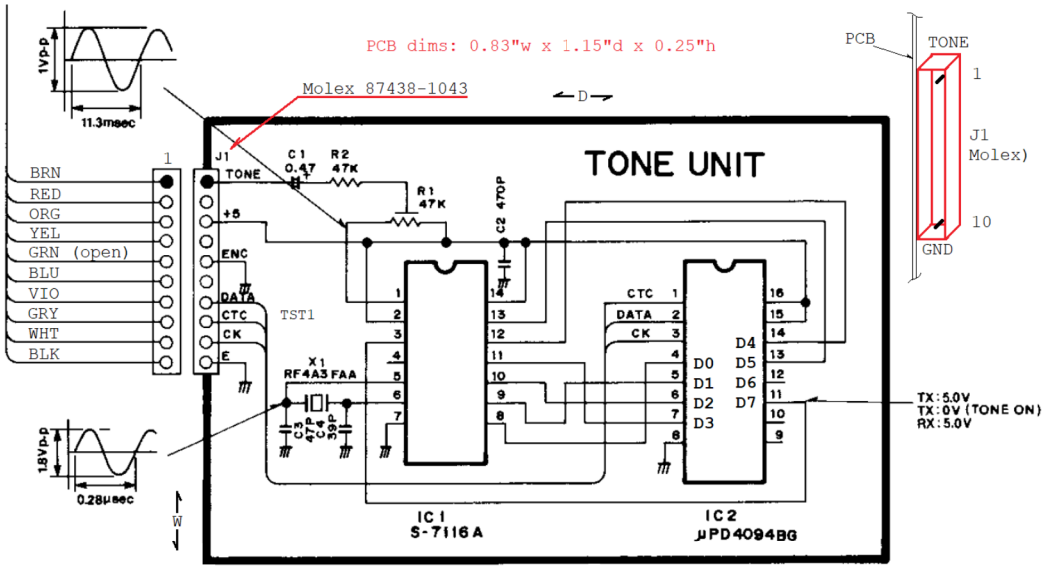
Existing Tone Board Schem:



SR Data Code Table:

SUBAUDIBLE TONE ENCODER FREQUENCY TABLE

OUTPUT FREQUENCY [Hz]	IC1 INPUT PIN NUMBER D0	D1	D2	D3	D4	D5	OUTPUT FREQUENCY [Hz]	IC1 INPUT PIN NUMBER						OUTPUT FREQUENCY [Hz]	IC1 INPUT PIN NUMBER 8	9	10	11	12	13
01: 67.0	H	L	L	L	L	L	0e: 107.2	L	H	H	H	L	L	1b: 167.9	H	H	L	H	H	L
02: 71.9	L	H	L	L	L	L	0f: 110.9	H	H	H	H	L	L	1c: 173.8	L	L	H	H	H	L
03: 74.4	H	H	L	L	L	L	10: 114.8	L	L	L	L	H	L	1d: 179.9	H	L	H	H	H	L
04: 77.0	L	L	H	L	L	L	11: 118.8	H	L	L	L	H	L	1e: 186.2	L	H	H	H	H	L
05: 79.7	H	L	H	L	L	L	12: 123.0	L	H	L	L	H	L	1f: 192.8	H	H	H	H	H	L
06: 82.5	L	H	H	L	L	L	13: 127.3	H	H	L	L	H	L	20: 203.5	L	L	L	L	L	H
07: 85.4	H	H	H	L	L	L	14: 131.8	L	L	H	L	H	L	21: 210.7	H	L	L	L	L	H
08: 88.5	L	L	L	H	L	L	15: 136.5	H	L	H	L	H	L	22: 218.1	L	H	L	L	L	H
09: 91.5	H	L	L	H	L	L	16: 141.3	L	H	H	L	H	L	23: 225.7	H	H	L	L	L	H
0a: 94.8	L	H	L	H	L	L	17: 146.2	H	H	H	L	H	L	24: 233.6	L	L	H	L	L	H
0b: 97.4	H	H	L	H	L	L	18: 151.4	L	L	L	H	H	L	25: 241.8	H	L	H	L	L	H
0c: 100.0	L	L	H	H	L	L	19: 156.7	H	L	L	H	H	L	26: 250.3	L	H	H	L	L	H
0d: 103.5	H	L	H	H	L	L	1a: 162.2	L	H	L	H	H	L							

H: HIGH L: LOW

Bit D7 = /TONE ENABLE (0 = tone on)

CTC (TST1) is assumed to pulse high at the end of the data XFR (this needs to be confirmed).

The F530 PWM creates approximately 5Vpp audio output which is fed into a voltage divider and 2-pole RC filter to get approximately 1Vpp at the input to the level adjust circuit (R1) used in the IC-901 version.

ATtiny3217 can't do precision timing easily. Will use C8051F531A with initial code copied from HM-133. SYSCLK is from ext 3.579545 MHz XTAL and is /2. Use PCA (CEX0) to capture clock edges. ISR shifts in data to an internal mem register. CEX2 captures strobe edges and sets DDS tone and tmute values.

DDS output uses PCA (CEX1) 8-bit PWM to generate tones from above table with a 6991 Hz Fsamp and a 256 byte sine table. Timer 1 drives DDS engine as in the HM-133 application.

CD4094 uses rising edge clock. Data shifts msb first. Data latches when strobe is high.

IPL with no tone (delF1 = 0 and tmute = 1) until enabled via SPI message.

C8051F531 I/O map:

P0.0: Vref (n/c)
P0.1: CK (SPI CLK), input (CEX0)
P0.2: PWM, output (CEX1)
P0.3: CTC (STB), input (CEX2)
P0.4: UART TX (n/c)
P0.5: UART RX (n/c)
P0.7: X1 (xtal)
P1.0: X2 (xtal)
P1.1: DATA (MOSI), input (GPIO)
P1.6: Fsamp out (n/c) (GPIO) {edges toggle at sample rate}

All others = not used, set to push-pull output.