Artemis-I Operation Manual (HW revision -, SW V0.3+)

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The Artemis-I is a PLL synthesizer based on the TI LMX2594 PLL chip. It utilizes a Microchip ATTINY-3217 microcontroller to configure the synthesizer registers via a serial interface. The following lists the major specifications of this synthesizer:

Frequency range: 4000 MHz to 15000 MHz *(operation as low as 2250 Mhz with reduced output)*
Output level: +12 ±2 dBm at 8000 MHz
Typical Phase Noise @ Fc = 4000 MHz: <TBD>
Typical Phase Noise @ Fc = 15000 MHz: <TBD>
Reference: 25.0000 MHz on-board
External reference selected by de-soldering and moving a chip capacitor and may range from 5 MHz to 1400 Mhz, 0.2 to 2 Vpp (-1 dBm to +19 dBm), Zin = 50Ω
Power supply: +5Vdc, 450 mA (heatsink required)
Communications: TTL UART com, 9600 baud, N81
/MUTE input: GND true, 3.3V compatible, on-board pull-up, GND to mute output
Frequency select inputs: 5 bit, binary, GND true, 3.3V logic
Primary connection: 16 pin ribbon header. Connector and cable not supplied. Connector P/N: TE/AMP 1658622-3, Ribbon cable, 16 conductor, 0.05” spacing, any vendor, length as needed (less than 12” recommended).
MCU PGM connection: Atmel UPDI programming via 16 pin connector or optional 6-pin programming connector

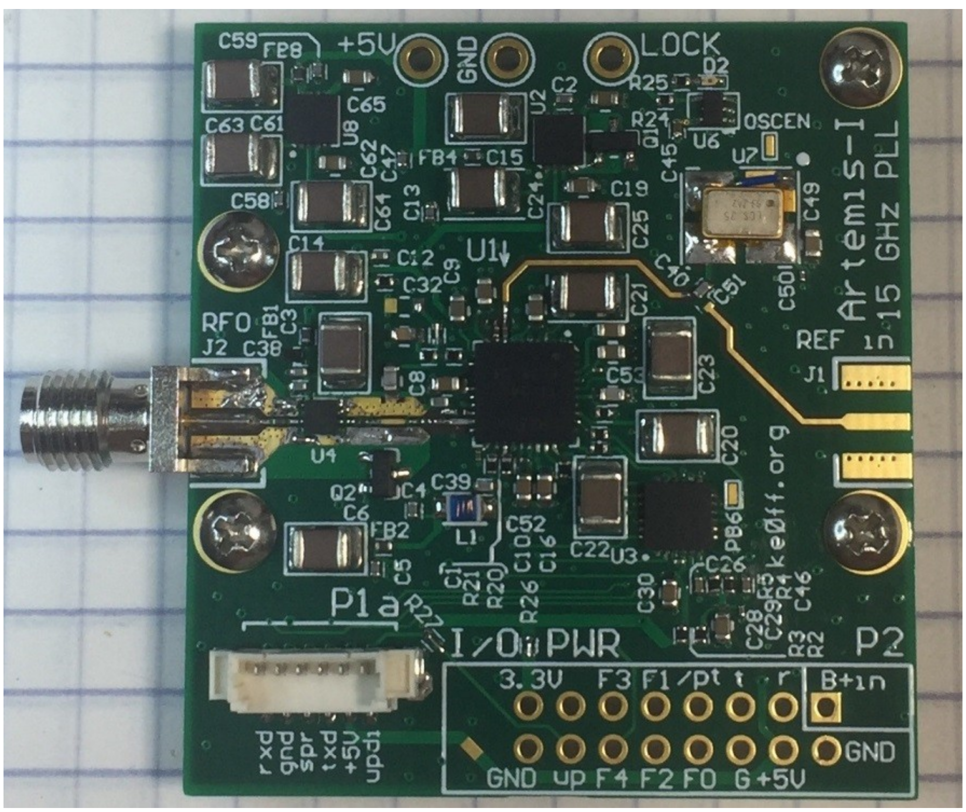


Figure 1. Artemis-I PLL Synthesizer

Operation

The Artemis operates from a +5Vdc supply. A heat-spreader/heat-sink is required for reliable operation (see Appendix for details). All power and control signals for normal operation are available at the main connector, P2.

P1 Pinout

UPDI	1
+5V	2
DBUG_TXD	3
SPARE	4
GND	5
DBUG_RXD	6

Note: See the "SiLabs/Tiva/ATtiny Programming Guide" (see the bibliography section of this document for a link) for more information about this connector.

P2 Pinout

+Vin (n/c)	1	2	GND
DBUG_RXD (TTL)	3	4	+5.0V
DBUG-232 TXD (TTL)	5	6	GND
/MUTE	7	8	FSEL0 (LSD b0)
(LSD b1) FSEL1	9	10	FSEL2 (LSD b2)
(LSD b3) FSEL3	11	12	FSEL4 (MSD b0)
n/c	13	14	UPDI
+3.3V (out)	15	16	GND

Note: All logic signals are 3.3V logic and will NOT tolerate higher voltage logic

Note: Optionally, a pre-regulator may be provided to allow a >+10V power source to operate the Artemis. See the appendix for an example.

Frequency Selection (Channels)

The Artemis supports 7 channels (SW V0.3+) providing a user-programmable frequency source. When /MUTE is open (>3.3V), the channel data represented by the binary code presented at the 5 FSEL inputs (only FSEL[2:0] are active at this time) is transferred to the PLL. Each channel consists of 80, 16-bit registers that are transferred to the LMX2594 when the channel is selected. These registers comprise the entire register set of the LMX2594 and allow for complete control of the PLL functionality. Refer to the LMX2594 datasheet for additional information regarding these registers.

It is recommended that users utilize the TICS Pro evaluation software provided by Texas Instruments when defining a register set for a particular channel definition. From this software, the contents of the can be exported transfer into the Artemis MCU firmware. Programming the channels currently requires reprogramming of the MCU application and covered in a later section of this document.

The 5-bit logic inputs use the pull-up feature of the ATTINY MCU to allow the PLL channel to be selected by applying GND (0V) or open (>+2.5V) levels to the FSEL inputs. To switch channels, simply apply the desired bit pattern (using GND true logic) to the FSEL[4:0] inputs. *Note: the MCU will change channels immediately upon detecting a change in the channel setting. Thus, if individual bits are changed over even just a few ms, it may be possible for the Artemis to step through one or more unintended channels as the inputs settle.*

"GND-True" means that a grounded bit = logic "1" and an open bit = logic "0". Thus, channel 3 would be set by leaving FSEL2 open, grounding FSEL1 and FSEL0 (A DIP switch or GND common binary selector switch works well for this purpose), with all other FSEL inputs open or GND .

/MUTE Function

If desired, the /MUTE input can be used to gate the PLL tone. This is useful for keying the output (for a beacon) or to mute the synthesizer for TX/RX transitions. Simply ground the /MUTE input to turn off the PLL, leave the input open to enable the output.

Serial Port

The Artemis MCU features a 3.3V TTL serial connection that can be used to program the MCU channel sets (future) or to provide real-time frequency control of the PLL. An elapsed time indicator and two temperature sensors are periodically reported to allow simple data-logging operations. The serial parameters are 9600 baud, 8 data bits, no parity, one stop bit. At power-on, an initialization banner message is sent by Artemis:

```
Artemis Help (cmds are case sensitive):
0-7: force-set PLL CH
n: tone on
f: tone off
cn: set hex U32 EE cal 'HGFEDCBA'
Cn: Read EE cal
on: set hex EE offs 'DCBA'
On: Read U16 EE offs
  n = sens#, 1/0
R: Download data to temp channel reg
   Rn..n<tab>0xiirrrr
        n..n = reg index (dec)
        <tab> = ASCII 0x09
        0xii = hex qualifier & hex index
        rrrr = hex reg data
Pc: PGM temp channel to ch# 'c'
t: send download data to PLL
<ENTER>: display ETI(sec)/temp(K) stats
    T0=regulator, T1=PLL
V: SW Version

a/A: read raw ADC, ch0/1
z: debug sram hex dump
z f: debug FLASH hex dump
```

The reset banner provides the software version and a brief list of version features. Primarily, this message is important for identifying the current software version, and verifying that the UART TX connection to the user terminal is working. *Note: The banner message might change with newer software versions.*

The serial commands available are as follows:

All commands are terminated with <CR> (ASCII 0x0d, <ENTER> or <RETURN> on most keyboards). *Note: The ATTINY serial port does <u>not</u> echo characters entered from the host terminal.*

Commands are case sensitive:

?: List Command Help
Displays an abbreviated list of the available commands.

0 – 7: Select Channel
Performs a channel selection just as if the logic inputs were set. The FSEL logic inputs will be superseded until they change state.

n: Tone on
Enables the PLL output. Same as opening the /MUTE input. The /MUTE input is superseded until it changes state.

f: Tone off
Disables the PLL output. Same as grounding the /MUTE input. The /MUTE input is superseded until it changes state.

<Enter>: with no or an invalid command, displays the PLL status message
An example message:

```
T0:323.4 K; T1:321.6 K; ETI: 3
```

T0 is the regulator temperature, T1 is the PLL temperature, the ETI is the number of seconds since power on. Temperatures are in Kelvins – subtract 273 to get the temperature in C. *Note: The sensors are located "near" their respective heat sources, but not extremely close, from a thermal perspective. For example, the PLL sensor reads about 10C lower than the PLL case temperature.*

a	**Read raw A/D value for sensor0**
A	**Read raw A/D value for sensor1**

The raw ADC values are used to create the sensor cal settings for the temperature sensors. See below.

Temperature Calibration Support Commands:

c0 hhhhhhhh	**Set sensor0 slope calibration**
o0 hhhh	**Set sensor0 offset calibration**
c1 hhhhhhhh	**Set sensor1 slope calibration**
o1 hhhh	**Set sensor1 offset calibration**
C0	**Read sensor0 slope calibration**
O0	**Read sensor0 offset calibration**
C1	**Read sensor1 slope calibration**
O1	**Read sensor1 offset calibration**

"h" is a hex digit (0 – 9, A – F, case insensitive).

These values are stored to the MCU EEPROM and are not erased when the MCU firmware is reprogrammed.

Calculation of the "h..h" parameters requires an accurate temperature measurement device to measure the air temperature in the vicinity of the Artemis unit. The procedure is to start with the Artemis at room temperature (it should rest with no power applied for at least 2 hours). Once the Artemis temperature is stabilized, ground the /MUTE signal, start the terminal emulator with an appropriate serial interface configured and then apply power to the Artemis.

Next, wait 60 seconds and then read the raw ADC values for each sensor ("a" and "A" commands) Also, read the ambient temperature near the Artemis. Record the ADC and temperature values. Use the Windows Calculator in Programmer mode to convert hex values to decimal. After the calculation of the cal value, use the calculator to convert decimal to hex.

The cal value, "K" is calculated as follows:

K = T * 10 * RawADC

Round the result and convert K to hex, and add leading zeros so that it is 8 digits total. Enter this value using the "cn hhhhhhhh" command where "n" is the sensor# and "h..h" is the hex value. The space between "n" and the first "h" is required, and spaces between "h" digits are not allowed. Each sensor should have its own value for K calculated.

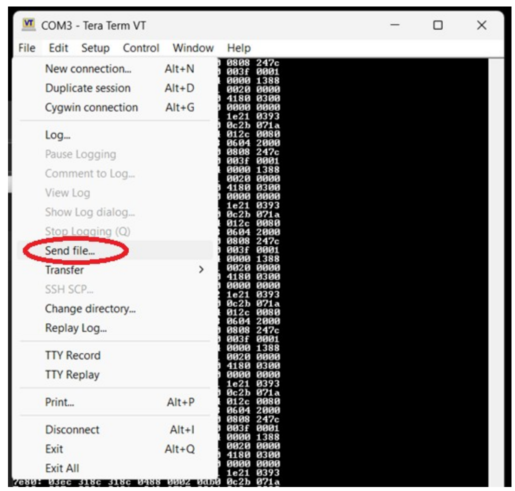
Set the offset values to "0000". The offset is for advanced calibration schemes and is not required for this procedure. The raw ADC data is buffered and can require several seconds (up to a couple of minutes) for the buffer to fill and provide valid, filtered data. This is true when the Artemis is first powered as well.

Rd..d<tab>0xiihhhh   Set register "d..d" (decimal) to "hhhh" (hex)

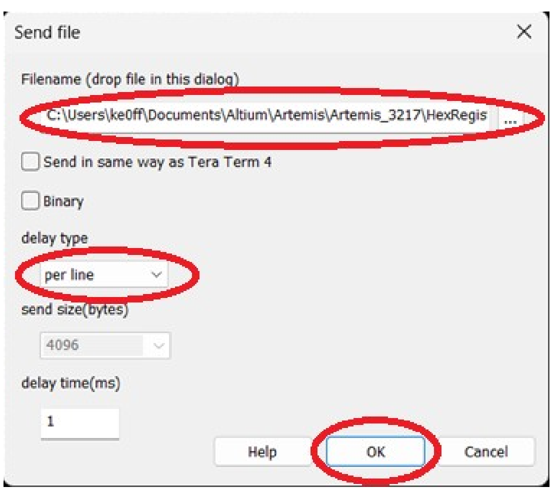
This command accepts a line from the TICSpro export file and stores it into the temporary PLL channel (stored in SRAM). Using a simple ASCII transfer, with 1 ms of line delay, the Artemis can accept the raw output file (via a terminal emulator) to transfer the register contents into temporary memory. Register numbers greater than 79 are ignored. The registers must be processed in decreasing order once "R79" is received. Further, the "d..d" decimal index value must match the "ii" hex index value, or an error results.

To send a file, consult your terminal emulator documentation (TeraTerm instructions are presented below for reference). Currently, only simple ASCII transfers are supported. No handshaking is utilized, but a minimum 1ms delay must be applied by the terminal emulator for each line of ASCII sent. This allows the Artemis time to process the data and be ready for the next register line.

In TeraTerm, select "File->Send File":



The following dialog box appears:



Select the file, set the delay type, and click "OK". It takes about 5 seconds for the file to transfer after which an "OK" or "Error" message is displayed. If "OK", the "t" or "P" commands may be used to test the channel or program it to FLASH.

t **Send temporary channel data to PLL**

This command sends the contents of the temporary channel (held in SRAM) to the PLL chip. The PLL will configure just as if the data were programmed in FLASH until a new FSEL setting is presented or a new channel command is entered into the CLI. At power-up, the temporary channel is set to all "0"s so sending this command without having received a valid channel will produce unforeseen results.

Pn **Program temporary channel to FLASH CH# "n"**

Stores the temporary channel to permanent storage in FLASH. *Note: The "P" command automatically erases the previous channel data, so there is no need for an "Erase" command.*

V: Display software version

z **Hex dump for temporary channel**
z f **Hex dump for all FLASH channel**

These are debug commands and should not normally be needed.

; **Null commands**

This allows optional comments to be embedded in channel files. Any text after the ";" is ignored.

TICS Software

The TICS software is the easiest way to define a register set for the LMX2594 and experiment with different LMX2594 register settings. This software can be downloaded at no charge from the TI web site (see the Bibliography/Links section at the end of this document. *Note, a log-in account is required, but is free to establish*).

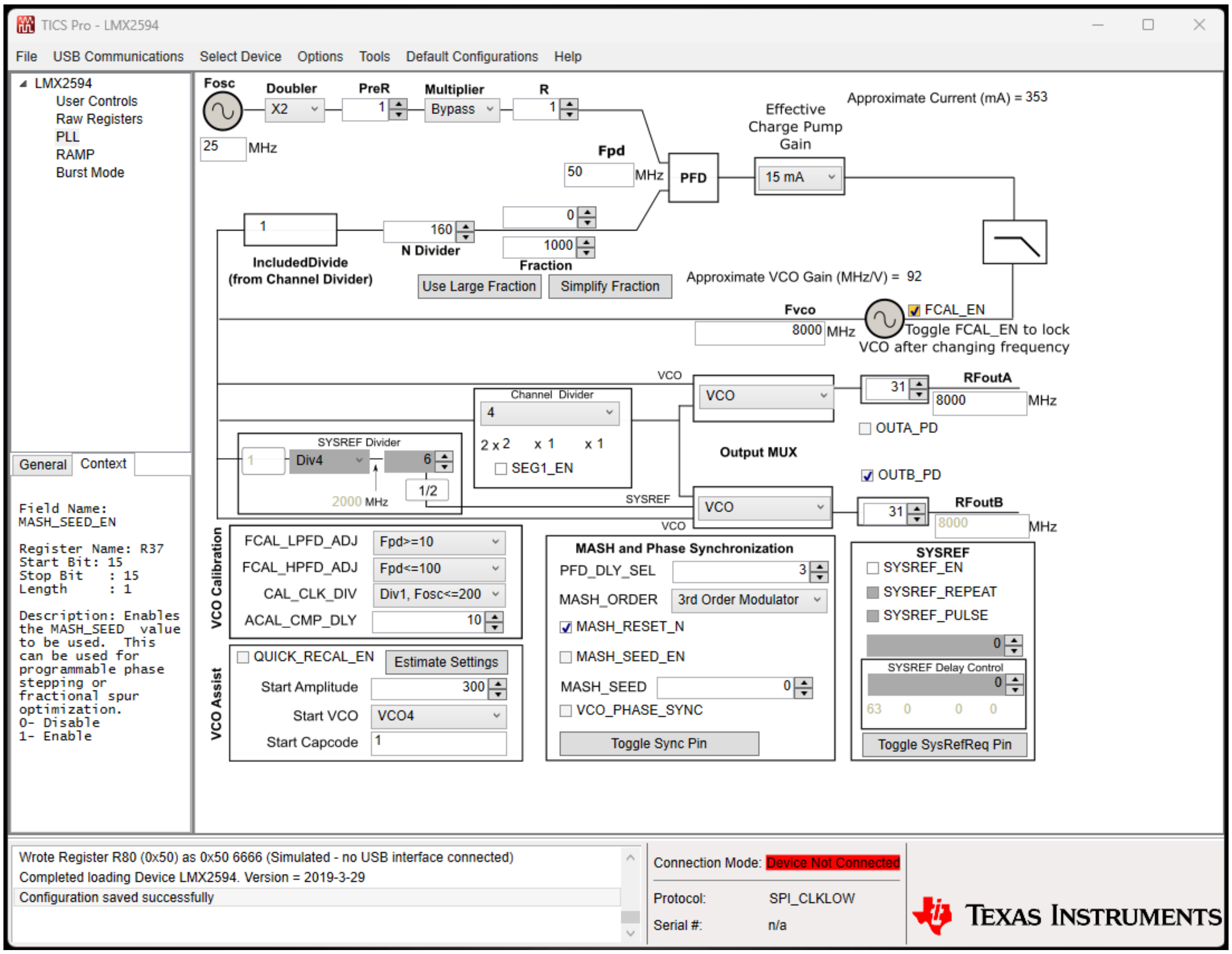


Figure 2. TICS Main Controls screen (selected by clicking “PLL” in the upper left pane).

Figure 2 illustrates the Main Controls screen of the software. *Note: this software has the ability to communicate directly with the TI Evaluation board for the LMX2594. However, this functionality is not available with the Artemis board.* Once the software is installed, the first step is to select the LMX2594 device as shown in Figure 3.

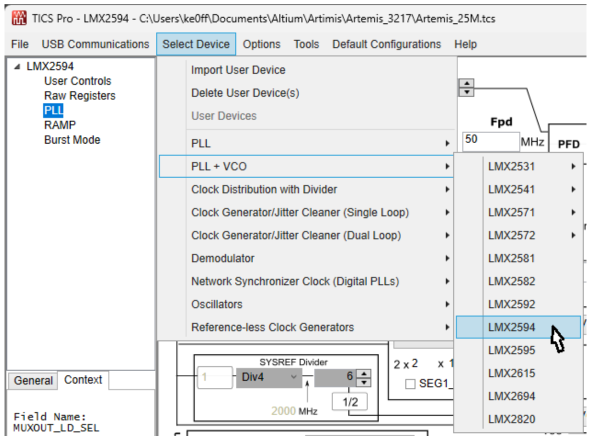
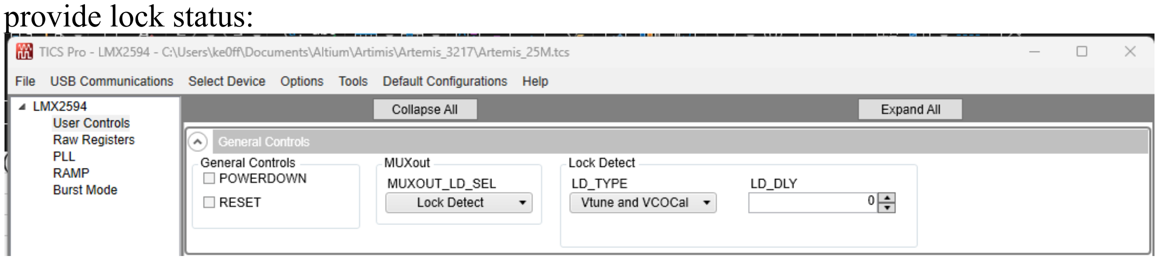


Figure 3. Device selection in the TICS application

Next, set the reference frequency. It is a good idea to save the configuration to allow later retrieval and to guard against the TICS software closing unexpectedly (it is known to do this on some machines). Under "File" choose "Save" and provide a meaningful filename (include the reference frequency, for example).

Also, be sure to confirm that the lock detect output is configured. This allows the LED to provide lock status:



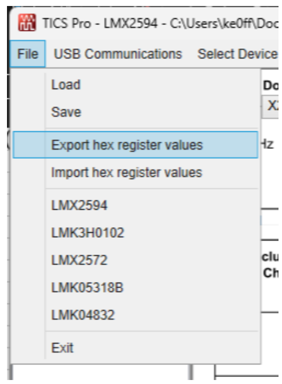
It is best to start with the default settings to the extent possible. The main items that must be filled in for a given frequency are as follows:

Reference Frequency: 25 MHz for the standard Artemis configuration (if a different reference is used, then that value is entered)
RFoutB: Enter the desired output frequency in MHz
OUTB_PD: Un-checked
RFoutA: do not adjust
OUTA_PD: Checked
RF Output Level: This is the unit-less numeric field next to the "RFoutB" text. 31 is the maximum effective setting. Values from 0 – 31 are considered usable.

The reference settings might require additional adjustment to allow fine-resolution frequencies to be selected. Refer to the LMX2594 datasheet and TICS help files for explanations of the other fields on this screen.

The TICS software updates the register settings in real time as the fields are updated. Settings that result in an illegal configuration or other known conflict will be indicated by “shading” of the respective setting field. The user may hover their mouse pointer over the field for a detailed message as to the nature of the problem and what should be done to correct it. The advice offered is generally acceptable.

Once a configuration is complete and there are no warnings displayed (the “FCAL_EN” check-box warning is for the TI Evaluation board connection and can be ignored), the register settings can be exported to allow them to be copied into the ATTINY source code. Under “File”, select “Export hex register values”:



And provide a meaningful filename. This file is a plain-text file (so use a “.txt” extension) that has a list of the register addresses and values. Note that this list is not immediately usable by the ATTINY compiler but may be downloaded as-is to the Artemis CLI serial port using suitable terminal emulator software.

If the data is to be placed in the “channels.c” source file, the desired data must be extracted first which is most easily accomplished by using Excel (2013 or later) or LibreOffice Calc (version 7.6 or later). An example file is included in the github repo, titled “register_extract.xlsx”. Follow the instructions in the spreadsheet for producing the output needed for the ATTINY compiler. The resulting data is copied and pasted into the “channels.c” source file, found in the ATTINY project “src” folder. Once all of the channels are copied into the source folder, the code may be compiled (F7) and loaded into the Artemis controller (green right-arrow).

Artemis Frequency Response

The LMX2594 can produce frequencies from 10 MHz to 15 GHz. That is over 3 decades of frequency range. However, the frequency response of the device varies over that range. In addition, the choice of buffer amplifier introduces its own influence on the frequency response of the Artemis output. In addition, cables and connectors introduce frequency dependent losses. The PMA2-183LN+ amplifier is specified to operate in the 4 to 15 GHz range, which covers the target range desired for the Artemis project (other synthesizers are available for the <4GHz range). However, the PMA2-183LN+ has some usable gain below 4 GHz, so it might be possible to use to as low as 2.25 GHz (no guarantees, however).

Figure 4 illustrates the Artemis response with the PMA2-183LN+. This plot represents a single sample, so it is for reference only. Performance at any given frequency must be verified by the user.

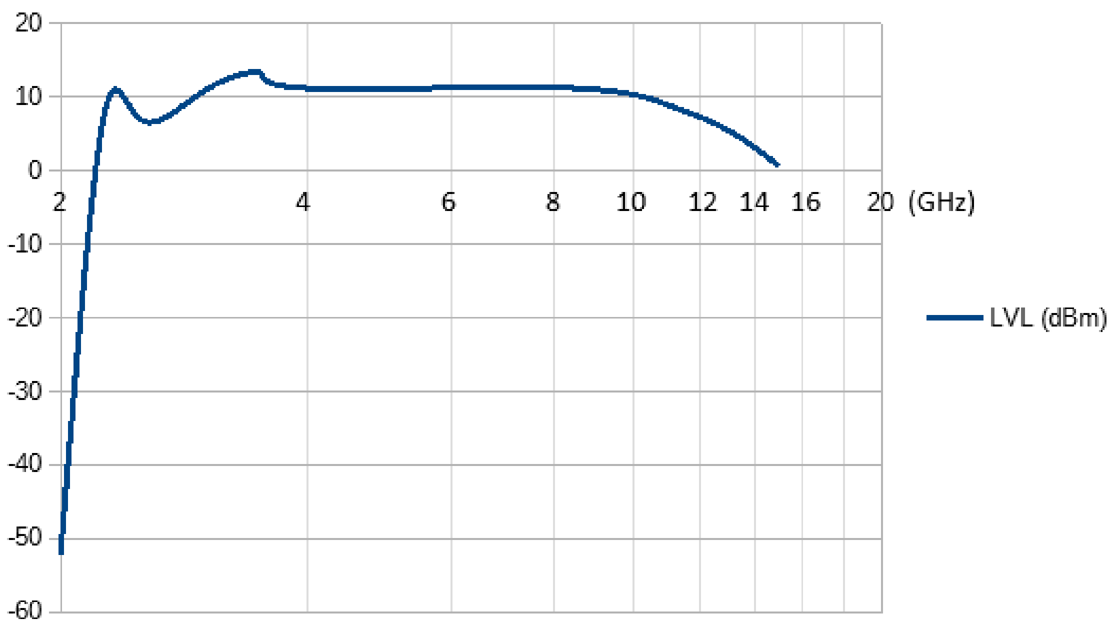


Figure 4. Representative frequency response of the Artemis synthesizer

MCU Programming Cable Connections

In order to program the MCU software or channel data using the MCU programming tools, the Microchip IDE compiler/debugger must be used with a suitable programming adapter. The programming adapter can be constructed with components available from DigiKey or Mouser. Instructions are found in the "SiLabs/Tiva/ATtiny Programming Guide" (see the Bibliography for a web link).

The debug adapter connects to P1 (see Figure 5). Follow the programmer instructions to compile and upload a new FLASH program to the MCU. *Note: The 1-wire UPDI programming signal is also exposed on P2-14 making it possible to route the programming signal outside the PLL enclosure for ease of access. UPDI and GND are the only signals needed to connect to an external programming interface.*

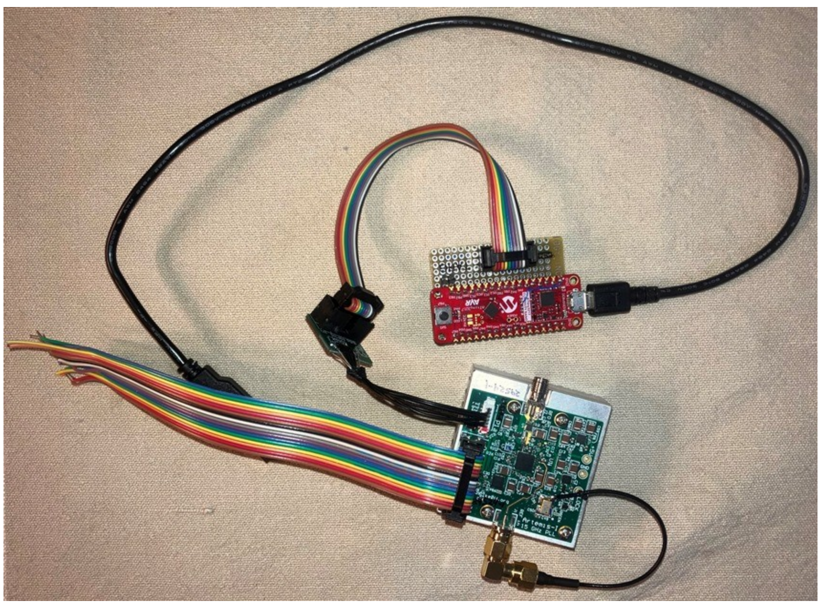


Figure 5. ATTINY programmer connection to the Artemis board

UART Connections

The Debug RXD and TXD connections (3.3V TTL) are available at P2-3 and P2-5, respectively. To exercise this option, a 3.3V TTL USB com port adapter must be used (Available on [Amazon.com: DTech USB to TTL Serial 3.3V Adapter Cable TX RX Signal 4 Pin 0.1 inch Pitch Female Socket PL2303 Prolific Chip Windows 10 8 7 XP Vista (6ft, Black) : Electronics] or other models that provide a UART COM port with 3.3V CMOS (sometimes referred as TTL) logic interface).

Alternatively, the ATTINY CuriosityNano Programmer, described in the "SiLabs/Tiva/ATtiny Programming Guide" (see the Bibliography for a link) can be used as a USB COM port for the Artemis board.

Bibliography/References

- TICS Software: https://dr-download.ti.com/secure/software-development/support-software/MD-xsZ2KP7U5k/1.7.7.5/TICSPro_1.7.7.5_23-Jul-2024.exe
- LMX2594 datasheet: https://www.ti.com/product/LMX2594?keyMatch=LMX2594&tisearch=universal_search&usecase=GPN-ALT
- Artemis github repo: https://github.com/ke0ff/artemis_pll
- Mini Circuits product page for the PMA2-183LN+: https://www.minicircuits.com/WebStore/dashboard.html?model=PMA2-183LN%2B
- SiLabs/Tiva/ATtiny Programming Guide: https://ke0ff.github.io/Orion/silabspgm.pdf
- Channel formatting spreadsheet: https://github.com/ke0ff/artemis_pll/blob/main/register_extract.xlsx

Appendix A
Installation and Application Notes

The Artemis mounting holes are sized for 2-56 screws (0.11" diameter clearance hole). Figure 6 illustrates the outline drawing of the Artemis including mounting hole locations. 8 screws and 4 standoffs are included with the Artemis kit. Replacement screws and standoffs may be obtained from McMaster-Carr (www.mcmaster.com) or other hardware supplier:

Screws, 2-56 x 0.250" (McMaster PN: 91772A077), QTY 4
Spacer, #2 x 0.0625" (McMaster PN: 92510A378), QTY 4

A heatsink is required for proper operation of the Artemis board. Figure 7 illustrates the drill/mill template for the mating surface of the heatsink (the source and P/N are in the BOM, shown later in this document). This template is available as a 3D printable model on the Artemis github.com repo. There are provisions to accommodate an external 5V regulator on the heatsink (user provided). A good, ultra-low-noise design is recommended.

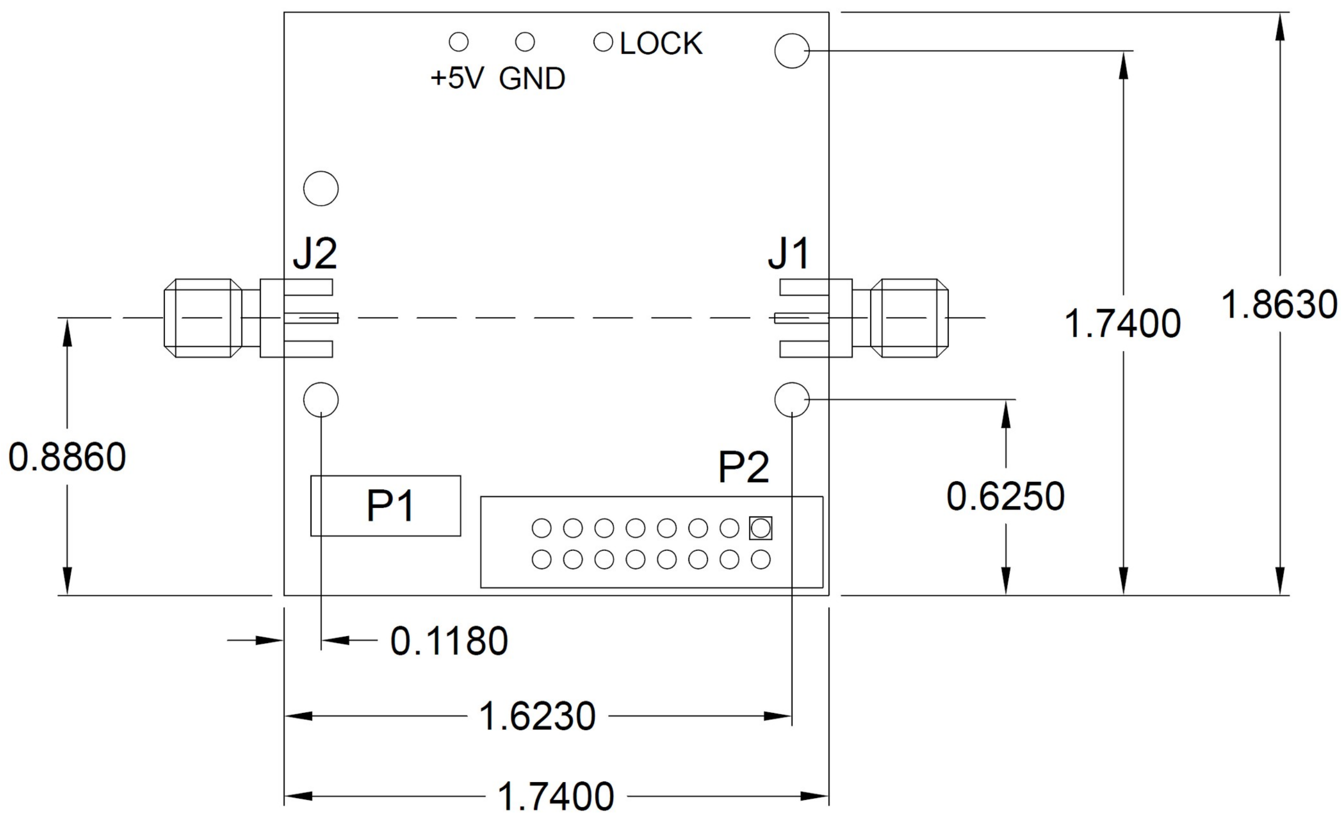


Figure 6. Artemis mechanical dimensions

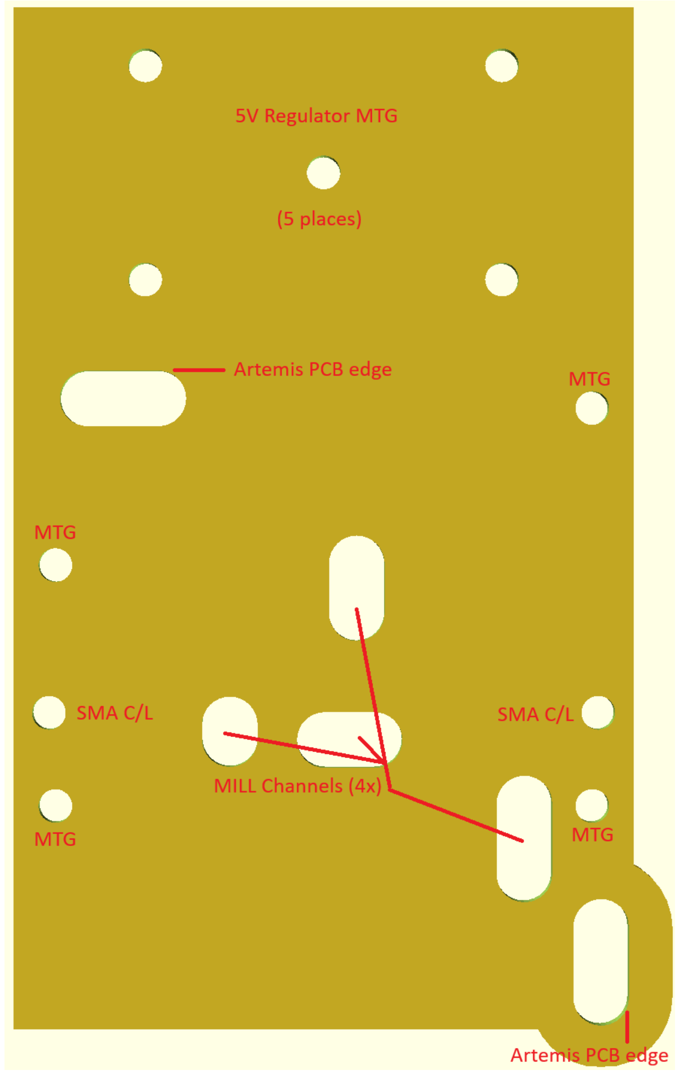


Figure 7. Artemis Heat-sink drill/mill template (dims in mils)
MTG holes are 2-56 drill and tap, 300 deep (8 places)
Center 5V regulator hole is 4-40 drill and tap, 300 deep
Mill channel (ϕ187.5) depths: (A) 95, (B) 102 (C) 60
SMA C/L troughs milled with ϕ500 end mil, offset 105 from top

RF Filtering

The Artemis PLL is an excellent signal source with a very wide tuning range. The Artemis is suitable for a transverter or transceiver LO source, or a lab instrumentation source. It is also a popular debug tool for field testing receivers when roving.

For all of its flexibility, there is one thing that must be considered when using the Artemis: filtering is required to reduce the harmonic output of the PLL. For some output settings, the harmonic output can be as high as -16 dBc or more. For instrumentation applications, this may not be a serious issue. However, for communications transceiver applications, these spurs must be reduced to preserve signal purity and system performance. Generally, a suitable low-pass filter will have an Fc somewhat above the desired output frequency (to reduce pass-band attenuation) and a stop band that extends to at least 5Fc. At least 30 dB at 2Fc and 35 dB of stop-band attenuation at or above 3Fc is a good general purpose target for most applications. This will generally provide -45 dBc or better harmonic perfomance.

Small SMA filters, such as available from MiniCircuits, are easy to implement, and are not terribly costly – they simply attach to the Artemis output via an appropriate adapter. For LO and other mixer applications, reflectionless filters are recommended as these present a consistent input/output impedance even in the stop-band. However, these can be more difficult to find and implement, so they are not often an easy option. A buffer with high-isolation can be used after the filter if it is a good match to 50 ohms in the stop-band. This may also require an attenuator if the buffer produces too much signal for the mixer. The attenuator should follow the buffer if possible and should offer a good output match across the entire bandwidth of the mixer.

Filtering for wide bandwidth applications (about an octave of bandwidth or greater) is difficult to manage. This is because the output frequency varies over the harmonic range of the lowest desired output. This means that a filter that is good for the lower frequencies will attenuate the higher frequencies and a filter optimized for the higher frequency will not provide sufficient attenuation to the 2^{nd} harmonic. In these cases, either a switched filter arrangement or a tunable filter, such as a YIG Tuned Filter (YTF), must be used. Both options represent a complicated compromise that will require considerable care and effort to produce.

Fortunately, most wide-band applications are geared towards instrumentation where other instruments that are part of the measurement suite might be expected to provide some semblance of filtering or other immunity to harmonics emitted by the Artemis reference source.

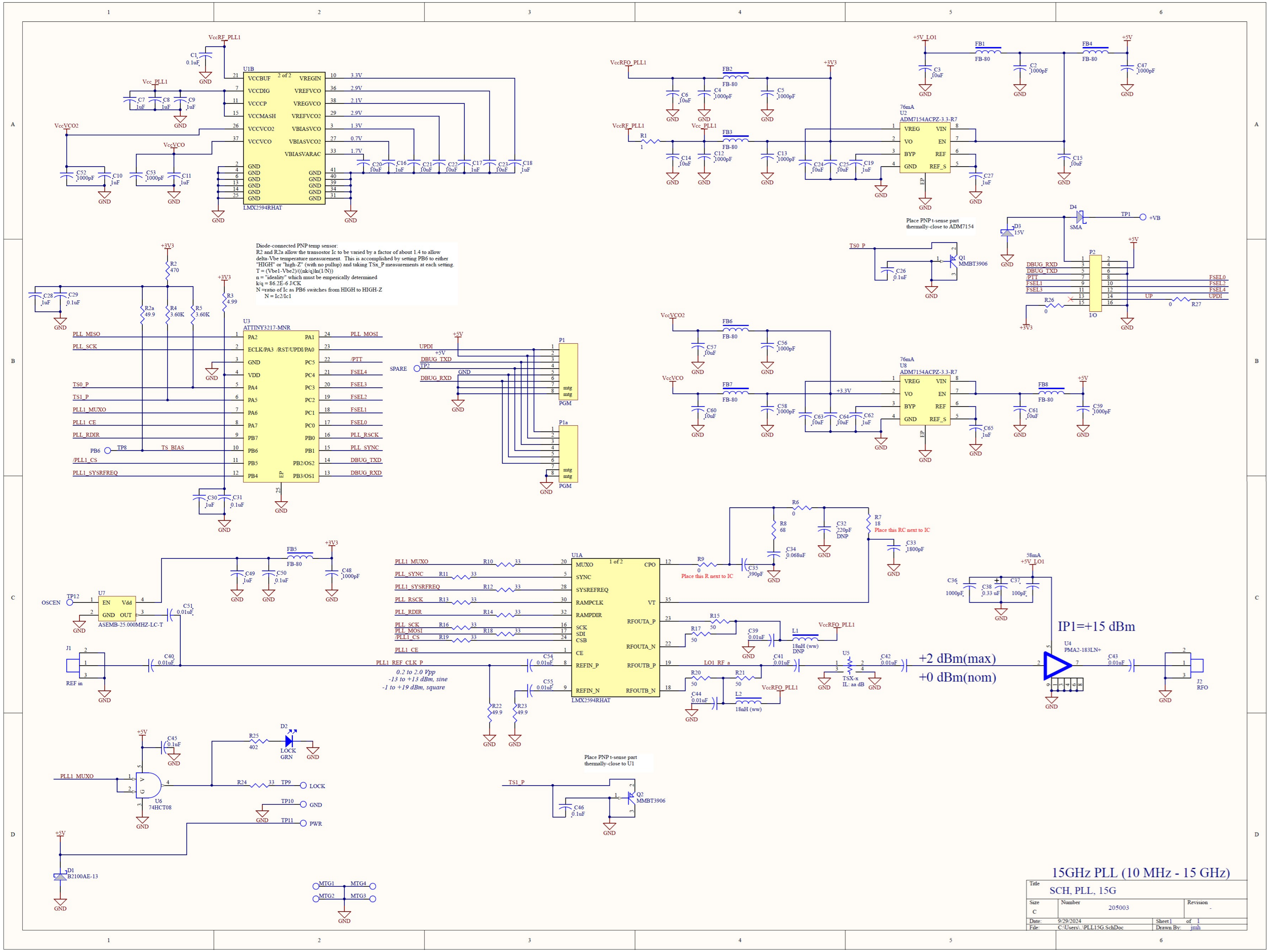
Appendix B
Schematic and BOM

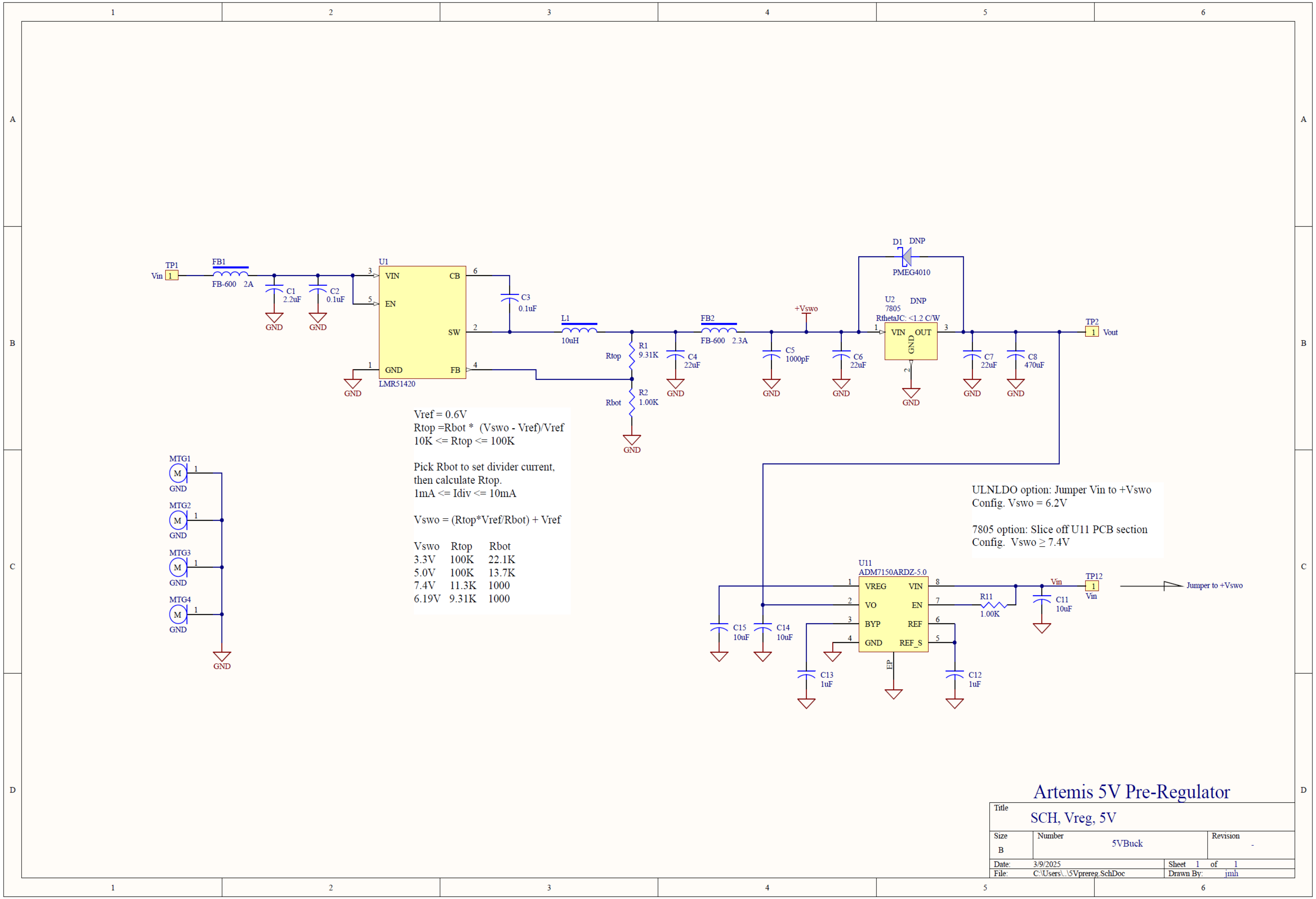
Bill **O**f **M**aterials

Qty	Designator	Description	MFR	MPN
4	C1, C29, C31, C50	CAP, MLCC, X5R, 0201, 25V, 10%, 0.1uF	Taiyo Yuden	GMK063BJ104KP-F
10	C2, C4, C5, C12, C13, C47, C48, C56, C58, C59	CAP, MLCC, C0G, 0402, 100V, 10%, 1000pF	Kemet	C0402C102J1GEC7411
3	C26, C45, C46	CAP, MLCC, X5R, 0402, 25V, 10%, 0.1uF	Murata	GRM155R71H104KE14D
2	C27, C65	CAP, MLCC, X7R, 0603, 50V, 10%, 1uF	Taiyo Yuden	UMK107AB7105MA-T
15	C3, C6, C14, C15, C20, C21, C22, C23, C24, C25, C57, C60, C61, C63, C64	CAP, MLCC, X7R, 1210, 50V, 10%, 10uF	Kemet	C1210C106K5RACTU
1	C33	CAP, MLCC, C0G, 0603, 100V, 10%, 1800pF	Murata	GRM1885C2A182JA01D
1	C34	CAP, MLCC, C0G, 0603, 50V, 10%, 0.068uF	TDK	VJ0603Y683KXACW1BC
1	C35	CAP, MLCC, C0G, 0603, 50V, 10%, 390pF	TDK	C1608C0G2A391K080AA
1	C36	CAP, MLCC, C0G, 0402, 50V, 5%, 1000pF	Murata	GRM1555C1H102FA01D
1	C37	CAP, MLCC, C0G, 0402, 50V, 5%, 100pF	Murata	GRM1555C1H101JA01J
1	C38	CAP, TANT, SMD, 0402, 0.33uF, 20V	ROHM Semi	TCTU1D334M8R
3	C39, C44, C51	CAP, MLCC, C0G, 0402, 16V, 10%, 10000pF	Murata	GRM1555CYA103GE01D
3	C41, C42, C43	CAP, MLCC, C0G, 0201, 16V, 10%, 0.1uF	Passives Plus	0201BB104KW160
2	C52, C53	CAP, MLCC, C0G, 0201, 100V, 10%, 1000pF	Murata	GRM0335C1H102GE01D
2	C54, C55	CAP, MLCC, C0G, 0201, 16V, 10%, 10000pF	Taiyo Yuden	MSASU063SB5103KFNA01
13	C7, C8, C9, C10, C11, C16, C17, C18, C19, C28, C30, C49, C62	CAP, MLCC, X7R, 0603, 50V, 10%, 1uF	Taiyo Yuden	MSASU168AB7105KTNA01
2	D1, D4	DIO, 50V, SHTKY, SMA	MCC	SS2150-LTP
1	D2	LED, 0402, GRN	Kingbright	APG1005CGC-T
1	D3	DIO, TVS, 15V, 500W	MCC	SMAJ16A-TP
8	FB1, FB2, FB3, FB4, FB5, FB6, FB7, FB8	Bead, Ferrite, SMD, 80 ohm	Laird	MI0402K121R-10
2	J1, J2	CONN, SMA, EDGE	TE Connectivity	CONSMA003.062
2	L1, L2	IND, CHP, WW, 2.7nH, 0805	Murata	LQW2BAS2N7J00L
0	P1 or P1a	CON, PICBLD, 1.25MM, 6POS (optional)	Molex	53398-0671
1	P2	CON, DIP, 16 POS	3M	D2516-6002-AR
1	P2-mate	CON, IDC, 16 POS	3M	D89116-0031HK
6	P2-cable (per inch)	CBL, RBN, 16 POS	3M	3801/16
2	Q1, Q2	TRAN, PNP, 40V, 100mA, 4.7K bias	OnSemi	MMUN2132LT1G
1	R1	RES, CHP, 0402, 1%, 100ppm/C, 1	Vishay/Dale	RCC04021R00FKED
9	R10, R11, R12, R13, R14, R16, R18, R19, R24	RES, CHP, 0402, 1%, 33	Yageo	RC0402FR-0733RL
2	R15, R17	RES, CHP, RF, 0402, 0.1%, 50	Vishay/Dale	FC0402E50R0BST1
1	R2	RES, CHP, 0402, 1%, 470	Yageo	RC0402FR-07470RL
4	R20, R21, R22, R23	RES, CHP, 0201, 1%, 49.9	Yageo	RC0201FR-0749R9L
1	R25	RES, CHP, 0402, 1%, 402	Yageo	RC0402FR-07402RL
1	R2a	RES, CHP, 0402, 1%, 49.9	Yageo	RC0402FR-0749R9L
1	R3	RES, CHP, 0402, 1%, 4.99	Yageo	RC0402FR-074R99L
2	R4, R5	RES, CHP, 0402, 1%, 3.60K	Yageo	RC0402FR-073K6L
4	R6, R9, R26, R27	RES, CHP, 0402, 1%, 0	Yageo	RC0402FR-070RL
1	R7	RES, CHP, 0402, 1%, 18	Yageo	RC0402FR-0718RL
1	R8	RES, CHP, 0402, 1%, 68	Yageo	RC0402FR-0768RL
1	U1	IC, PLL, w/VCO, 7.3-15000 MHz, 300MHz REF	TI	LMX2594RHAT
2	U2, U8	IC, VREG, ULN, 3.3V	Analog Devices	ADM7154ACPZ-3.3-R7
1	U3	IC, MCU, SFF, 8b, 32Kb, 20MHz	MicroChip	ATTINY3217-MNR
1	U4	MMIC, AMP, E-PHEMT	Mini Circuits	PMA2-183LN+
1	U6	IC,GATE,2IN,AND,SNGL,	TI	SN74AHC1G08DCKR
1	U7	IC, OSC, SMD, W_EN	ECS	ECS-TXO53-S3-33-250-BN-TR
ALT	U7	IC, OSC, SMD, W_EN	Abracon	ASEMB-25.000MHZ-LC-T
1	PCB	PCB, Artemis-I, Rev -	ANY	Artemis-I
1	THP1	Pad, Thermal, 1”x1”	Laird	A15959-07
1	HS1	Heat Sink, 2”x3”, 5W – heatsinkonline.com	heatsinkonline.com	253AS

5V Pre-Regulator CCA **B**ill **O**f **M**aterials

QTY	Designator	Description	MFR	MPN
1	C1	CAP, MLCC, X7R, 1210, 100V, 10%, 2.2uF	AVX	12061C225K4T2A
2	C2, C3	CAP, MLCC, X5R, 0402, 50V, 10%, 0.1uF	Murata	GRT155R71H104KE01D
3	C4, C6, C7	CAP, MLCC, X7R, 1210, 25V, 10%, 22uF	Samsung	CL32B226KAJNNNE
1	C5	CAP, MLCC, C0G, 0805, 100V, 10%, 1000pF	Walsin	0603N102G101CT
1	C8	CAP, TANT, 2917, 6.3V, 10%, 470uF	Vishay	TR3E477K6R3C0050
3	C11, C14, C15	CAP, MLCC, X7R, 1206, 50V, 10uF	Samsung EM	CL31B106KBHNNNE
2	C12, C13	CAP, MLCC, X7R, 0805, 50V, 1uF	Samsung EM	CL21B105KBFNNNE
1	FB1	FB, 0805, 600 ohm, 2A	Fair-Rite	2508056017Y2
1	FB2	FB, 0805, 600 ohm, 2.3A	Murata	BLM21SP601SN1D
1	L1	IND, 1819, 10uH, 5.4A	Coiltronics	EXL1V0505-100-R
1	R1	RES, CHP, 0603, 1%, 100ppm/C, 9.31K	Yageo	RC0603FR-079K31L
2	R2, R11	RES, CHP, 0603, 1%, 100ppm/C, 1.0K	Yageo	RC0603FR-071KL
1	U1	IC, REG, SW, BUCK, SOT-23-6	TI	LMR51420XDDCR
1	U11	IC, REG, ULN, 5.0V, SO8-EP	Analog Devices	ADM7150ARDZ-5.0
1	N/A	PCB, Artemis_PreReg	Any	Artemis-PreReg


Diode-connected PNP temp sensor:
R2 and R2a allow the transistor Ic to be varied by a factor of about 1.4 to allow
delta-Vbe temperature measurement. This is accomplished by setting PB6 to either
"HIGH" or "high-Z" (with no pullup) and taking TSx_P measurements at each setting.
T = (Vbe1-Vbe2)/((nk/q)ln(1/N))
n = "ideality" which must be emperically determined
k/q = 86.2E-6 J/CK
N =ratio of Ic as PB6 switches from HIGH to HIGH-Z
N = Ic2/Ic1
Place PNP t-sense part thermally-close to ADM7154
Place PNP t-sense part thermally-close to U1
Place this R next to IC
Place this RC next to IC
0.2 to 2.0 Vpp
-13 to +13 dBm, sine
-1 to +19 dBm, square
IP1=+15 dBm
+2 dBm(max)
+0 dBm(nom)
U1B LMX2594RHAT
U1A LMX2594RHAT
U2 ADM7154ACPZ-3.3-R7
U8 ADM7154ACPZ-3.3-R7
U3 ATTINY3217-MNR
U4 PMA2-183LN+
U5 TSX-x
U6 74HCT08
U7 ASEMB-25.000MHZ-LC-T
Q1 MMBT3906
Q2 MMBT3906
D1 B2100AE-13
REF in
RFO
15GHz PLL (10 MHz - 15 GHz)
Title
SCH, PLL, 15G
Size C
Number 205003
Revision -
Date: 9/29/2024
Sheet 1 of 1
File: C:\Users\..\PLL15G.SchDoc
Drawn By: jmh


Vref = 0.6V
Rtop =Rbot * (Vswo - Vref)/Vref
10K <= Rtop <= 100K
Pick Rbot to set divider current, then calculate Rtop.
1mA <= Idiv <= 10mA
Vswo = (Rtop*Vref/Rbot) + Vref
Vswo Rtop Rbot
3.3V 100K 22.1K
5.0V 100K 13.7K
7.4V 11.3K 1000
6.19V 9.31K 1000
ULNLDO option: Jumper Vin to +Vswo
Config. Vswo = 6.2V
7805 option: Slice off U11 PCB section
Config. Vswo ≥ 7.4V
Jumper to +Vswo
Artemis 5V Pre-Regulator
Title SCH, Vreg, 5V
Size B
Number 5VBuck
Revision -
Date: 3/9/2025
Sheet 1 of 1
File: C:\Users\..\5Vprereg.SchDoc
Drawn By: jmh