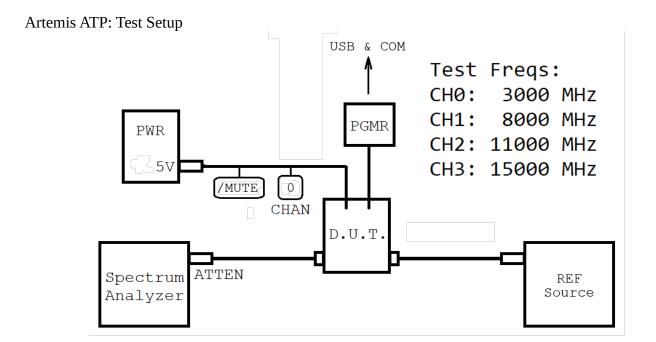
Date: / 20 S/N	I:	SW Ve	ersion:
Test Operator: Pov	wer +5Vin:	Vdc (mea	sure at PCB TP)
1) UART TX serial test: Observe Powergarbled characters.	-on banner message. P	asses if message i	is displayed with no P/F:
2) UART RX serial test: Issue "?" help of displayed with no garbled characters.	command from PC term	ninal. Passes if he	elp message is P/F:
3) FSEL Test: Cycle through binary inpudigits are recognized and displayed (after			terminal. Passes if all P/F:
4) /MUTE Test: cycle /MUTE, and obse toggles (muted output less or equal to -4	± •	serial terminal. P	asses if channel output P/F:
5) +3.3V out Test: Measure P2-15 with a $V_{\rm (3.3V)}$:	n DMM. Passes if volta	age = 3.3V ±10%	P/F:
6) Sideband Test: Set CH2 and observe to Verify that any sidebands are ≤-40 dBc. <i>measurable if they are greater than 3 dB</i> (Fc level: dBm) – (SB level: Span: MHz SB Freque	Record strongest sides above the noise floor. dBm) =	oand. <i>Note: sideb</i> dBc	ands are considered
7) Output level test #1: Set CH1 and obs signal level. Passes if output is ≥ +10 dl Level: dBm	<u> </u>	=	analyzer. Record the P/F:
8) Output level test #2: Set CH3 and obssignal level. Passes if output is ≥ 0 dBm Set CH0, passes if 3 GHz level is $\geq +10$. Level:	dBm	P/F:
9) Noise Test: Set CH2 and observe the set a 100 Khz span and measure the abs. offset. Fc level: dBm Noise NL (dBc) = {Noise Level} - {Fc	noise level. Passes if ise level:	NL is better than · dBm/Hz	-78 dBc/Hz at 10KHz
10) Load custom channel config and test			
REFERENCE Freq:	Level:		
FSEL 0:	FSEL 1:		
FSEL 2:	FSEL 3:		
Test Operator Signature:			

Artemis Acceptance Test Procedure



POWER SUPPLY:				
DMM Model/SN:				
S/A:			-	
EXT. ATTEN: dB	ATTEN MODEL/SN:			
D.U.T. RF OUT CABLE:			-	
LOSS AT 2 GHz:	dB	LOSS AT 12 GHz:	dE	3
LOSS AT 8 GHz:	dB	LOSS AT 15 GHz:	dE	}
ATP REF SOURCE:			_	
LEVEL AT D.U.T.	. CONNECTOR:	dBm		
Date: / / 20) TEST OPERATO	OR:		_