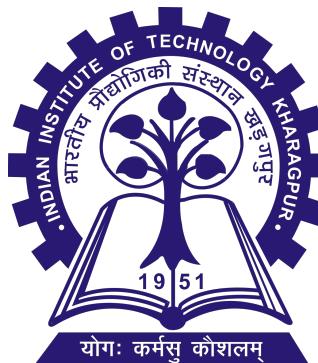


CHARGER DESIGN FOR LIGHT ELECTRIC VEHICLES

*Report submitted to
Indian Institute of Technology, Kharagpur
for the award of the degree
of*

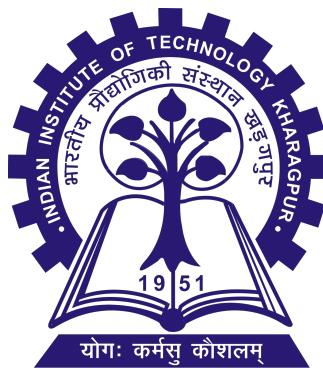
Bachelor of Technology
in Electrical Engineering

by
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Department of Electrical Engineering
Indian Institute of Technology, Kharagpur
May 2020

**DEPARTMENT OF ELECTRICAL ENGINEERING
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CERTIFICATE

This is to certify that the dissertation report entitled "Charger Design for Light Electric Vehicles" submitted by **Mr. Shuvam Keshari** to Indian Institute of Technology Kharagpur, India, is a record of bonafide research work carried out by him under my supervision and guidance and is worthy of consideration for the award of the degree of Bachelor of Technology in Electrical Engineering of the institute.

(Dr. Dipankar Debnath)

DECLARATION

I certify that:

1. The work contained in this report has been done by me under the guidance of my supervisor(s).
2. The work has not been submitted to any other Institute for any degree or diploma.
3. I have followed the guidelines provided by the Institute in preparing the report.
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(SHUVAM KESHARI)

(16EE10046)

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Abstract

The aim of this project is to design an efficient charger for light(3kW) electric vehicles. We are in a new era of transportation, where cleaner cars (that are also affordable) are not a thing of imagination. Electric vehicles are being treated essential for the sustainability and development of human society. The charger, being an essential component of the vehicle, demands a good design.

The charger has two stages; the first stage is a PFC (Power factor correction) rectifier followed by an isolated buck converter (PSFB : Phase-shifted full bridge). The rectifier ensures power factor close to 1 at the input side, which helps us ensure lower losses and also smaller current rating outlet at the input side. The PSFB converter ensures controlled current output to the battery while also providing isolation for protection of either side due to any fault.

All simulations have been done using PSIM.

All programming has been done on NXP microcontrollers.

Keywords: electric vehicles, charger, flyback, power factor correction, phase shifted full bridge

List of Symbols and Abbreviations

<i>EV</i>	: Electric Vehicle
<i>PFC</i>	: Power Factor Correction
<i>PSFB</i>	: Phase Shifted Full Bridge
<i>ICE</i>	: Internal Combustion Engine
<i>DCFC</i>	: Direct Current Fast Charger
<i>EVSE</i>	: Electric Vehicle Supply Equipment
<i>BMS</i>	: Battery Management System
<i>ZVS</i>	: Zero Voltage Switching
<i>CC/CV</i>	: Constant Current/Constant Voltage charging
<i>IC</i>	: Integrated Circuit
μC	: Micro-controller
<i>LDO</i>	: Low Drop Out
<i>CCM</i>	: Continuous Conduction Mode
<i>DCM</i>	: Discontinuous Conduction Mode
<i>ESR</i>	: Equivalent Series Resistance
<i>SWG</i>	: British Standard Wire Gauge
<i>SMD</i>	: Surface Mount Device
V_{OR}	: Output Reflected Voltage

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Introduction

1.1 A Short History of EVs

The first *practical* electric vehicle was built by Thomas Davenport in 1835 (motor patented: February 25, 1837). Although diesel and gasoline vehicles were introduced by 1900, the internal combustion engines they used were not perfect yet and steam engines had their own limitations. Hence, Ferdinand Porshe (first 1898 model: Lohner Porshe) and Thomas Edison set out to build and popularize electric vehicles, which were being seen as the future of mobility.

By 1914, Henry Ford had introduced an efficient assembly line for mass production of gasoline vehicles that brought down the price to \$260 as compared to an Electric Roadster costing \$1750. Additionally, the invention of the automatic starter combined with the superior range of petrol cars impacted the viability of electric vehicles. The battery technology just wasn't there.

By 2000, with the development of light-weight and high energy density lithium-ion batteries, soaring oil prices and environmental pollution, EVs began gaining popularity again. Tesla Motors and other car manufacturers have pledged to shift towards electric for a greener future.

1.2 Why is EV the New Buzzword?

More often than not, whenever change happens, it is just history repeating itself. The EV segment of the automobile industry has shown a similar trend: from about 40% in 1900, to almost nil by 1935, and sharply increasing again as we approach 2020. Predicted to be the next disruptive market force for transportation, EVs have the potential to revolutionize how energy is used, created and redirected.

Benefits of Going Electric

Fights Global Warming: One of the primary reasons for the introduction of electric cars into the market is the concern over greenhouse gas emissions and their contribution to global warming. Elimination of the exhaust pipe in electric cars promotes sustainable mobility.

Better Energy Efficiency: EVs are 75% efficient at turning input energy into kinetic energy, while gas-powered vehicles with internal combustion engines (ICE) are only 25%.

Low Maintenance Costs: An average driver could save approximately \$860 a year on gas costs when they switch to an electric car. A 50kWh battery has a range of 220 miles and charging it fully costs about \$5.5, whereas fuel costs about \$21 for the same range.

In the future, it is likely that all cars will be electric. In fact, there are already pledges in place by many car manufacturers to have a full electric fleet in only a couple decades. It's time to embrace the change and look towards our future. [5]

1.3 Why is the Charger Design so Important?

The charging infrastructure plays a vital role in the EV market. One of the prime reasons why EVs are not able to penetrate certain market segments is the “charging anxiety”. Simply put, it takes a lot of time to charge an EV, making it a problem for emergencies. For a typical EV, the time taken to add 100 miles of range varies from 26 hours for the slowest AC charger, to 6 minutes for the fastest DCFC (Direct Current Fast Charger) — still far slower than the 300 miles/minute enjoyed by a 30 mile/gallon ICE.

Faster charging implies a more powerful charger, which in turn implies higher operating current levels and hence demands an efficient power electronic design. Several protection and communication features are also vital while charging, thus arising the need of the commonly known EVSE, a protocol to help keep the user and the electric vehicle safe while charging.

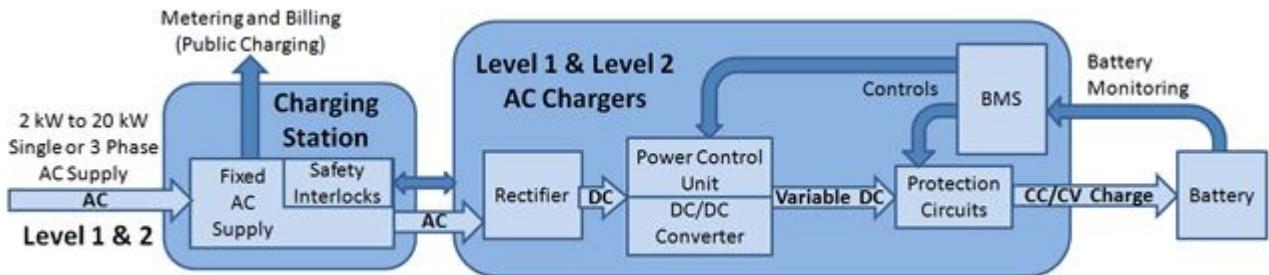


Figure 1.1: Schematic of a typical EVSE. [3]

1.4 Target Architecture

In this project, we have a target of building the hardware of a 3kW charger for an electric vehicle powered by a 72V Li-ion battery (LiFePO₄ type). This specification was chosen based on the fact that in India, electrification of Light Public transport vehicle mostly used for last mile connectivity could work with such a charger rating. Our vision is to enable India to develop its own products in the field of EV rather than being dependent on China, which has been the case for many other fields.

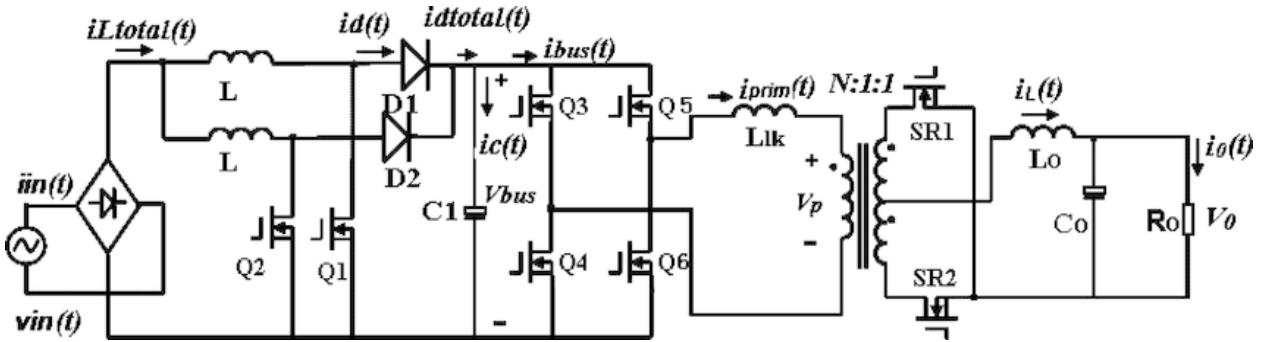


Figure 1.2: Target Architecture of the Charger. [14]

As can be seen from the figure above, there are two stages of the charger:

- **PFC :** The first non-isolated PFC stage for rectification (AC-DC). It is essentially a boost converter that ensures unity power factor at the input side using certain techniques of current programmed control. The output of this stage is a fairly stable DC voltage that must be higher than the peak of the input sinusoidal voltage. This stage can be interleaved for a higher current rating.
- **PSFB :** The second stage is an isolated DC-DC stage for conversion to a lower voltage value. PSFB topology is suitable for the 3kW design target since ZVS can be achieved easily. Here too, the output switches (SR1 and SR2 in the figure) may be paralleled to increase the current handling capacity.

Design Sequence

As discussed in the previous chapter, the charger consists of 2 stages. The figure below shows that each stage has its own controller which in turn, should have its own power supply.

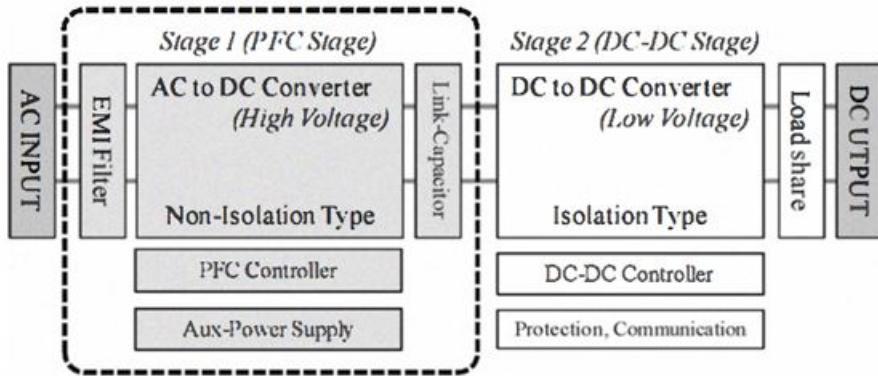


Figure 2.1: Block Diagram of the Charger Components

An isolated power supply is also needed for the controller and gate drivers of the final DC-DC stage. Finally, an input EMI filter and output current monitoring protocols for CC/CV charging are also essential. With so many aspects to consider, a proper design sequence is essential to approach the project. Each aspect needs to be designed, fabricated and tested in a modular way before the final integration of everything involved:

- Auxillary Power Supply Design
- PFC Design and Testing with resistive load
- PSFB Design and Testing with PFC
- Integration of CC/CV modes

Design of the Auxiliary Power Supply

3.1 Necessity

The only source of energy in an EV is the battery, which has a terminal voltage of about 72V. Various components inside the vehicle need power at different voltage levels to run properly. A small gate driver IC for instance, needs about 12V and a few mA of current to function. Hence arises the need of voltage conversion from the main 72V battery to various other voltage levels. Since most of the components need less than 15V to operate, one of the output voltages can be maintained at 16V (1V drop-out allowance).

Another important aspect for EV charging is the *ground reference* or simply *ground*. We already have the battery ground (negative terminal). Whenever an external source is plugged into the EV (the AC supply while charging), a new ground reference also comes into picture (the AC ground). Now, for example, we have to power a gate driver circuit on the AC side that needs 12V DC supply (with respect to AC ground). It is obviously impractical to make an AC-DC converter just for maintaining the ground reference. A better idea would be to use the battery itself for that purpose since low power isolated DC-DC conversion is much simpler. Hence the need of isolated voltage conversion also comes into picture. Here too, a 16V isolated output can be designed.

A third ground reference is also essential because we generally want the micro-controllers (μ C) to operate at their own reference altogether because of noise issues. These μ Cs operate at low voltages and currents, so an 8V isolated output would be enough.

Thus we need an auxiliary power supply that takes power from the battery at 72V, maintains isolation among three different ground references and also changes the voltage level as follows:

- **Battery ground (with 16V output)**
- **AC ground (with 16V output)**
- **μ C ground (with 8V output)**

We shall now decide the kind of converters to use for this purpose.

(Note that lower voltage levels can be achieved by using an LDO regulator [e.g 8V to 3.3V]. The power loss will be negligible since current levels are quite low).

3.2 Topology Selection

The non-isolated conversion from 72V to 16V w.r.t battery ground can be achieved using the simplest DC-DC converter i.e. the Buck converter. The output is controlled at 16V.

The other two grounds are different from the battery ground; hence we need an isolated DC-DC converter for this low power conversion. The best topology for this is the Flyback converter, since it can provide isolation with minimum component count. Of course, it should have 2 secondary windings, one 16V winding w.r.t AC ground and one 8V winding w.r.t μC ground.

3.3 Modes of Operation of the Converters

The Flyback converter is essentially an isolated buck-boost converter and hence it has the problem of right half plane zero when operating in CCM. To illustrate this aspect, let us take a standard buck-boost converter operating with a steady state duty ratio of d and input voltage V_{in} . We know that in the small signal model (with perturbations), the control gain is given by:

$$\frac{\hat{v}_0(s)}{\hat{d}(s)} = G_{vd} \cdot \frac{1 - \frac{s}{\omega_z}}{1 + \frac{s}{Q\omega_0} + \left(\frac{s}{\omega_0}\right)^2} \quad (3.1)$$

where :

$$G_{vd} = \frac{V_{in}}{(1-d)^2} \quad \omega_z = \frac{R}{L} \cdot \frac{(1-d)^2}{d} \quad Q = (1-d)R\sqrt{\frac{C}{L}} \quad \omega_0 = \frac{1-d}{\sqrt{LC}}$$

We can clearly see that there is a zero in the right half plane at ω_z . Due to this, when we increase the control input d , there is initially a drop in the output voltage. This problem goes away if we shift to DCM operation. The state space averaged dynamic model of the DCM Flyback converter (equivalent buck-boost) is given by (d, d_2 are steady state variables) :

$$\dot{\hat{x}} = \begin{bmatrix} 0 & 0 \\ \frac{d_2}{C} & -\frac{2}{RC} \end{bmatrix} \hat{x} + \begin{bmatrix} 0 \\ \frac{d}{d_2 RC} \end{bmatrix} \hat{v}_{dc} + \begin{bmatrix} 0 \\ \frac{V_{dc}}{d_2 RC} \end{bmatrix} \hat{d} \quad (3.2)$$

If the steady state output voltage is V_0 , then the control gain is given by:

$$\frac{\hat{v}_0(s)}{\hat{d}(s)} = K \cdot \frac{1}{1 + \frac{s}{\tau}} \quad (3.3)$$

which is a 1st order system where : $K = \frac{V_0}{2d}$ & $\tau = \frac{2}{RC}$

Hence, the Flyback converter should be designed to run in DCM at all operating conditions. The buck converter however, does not have the issue of right half plane zero. For a steady state duty ratio d and input voltage V_{in} , the small signal control gain is given by:

$$\frac{\hat{v}_0(s)}{\hat{d}(s)} = \frac{V_{in}}{1 + \frac{s}{Q\omega_0} + (\frac{s}{\omega_0})^2} \quad (3.4)$$

where : $Q = R\sqrt{\frac{C}{L}}$ & $\omega_0 = \frac{1}{\sqrt{LC}}$

Hence the buck converter should be designed to operate in CCM, which can be easily implemented by making it synchronous.

(Note that since equations 3.1, 3.3 and 3.4 are based on small signal models, the steady state quantities (d, V_{in}, V_0) themselves are dynamic variables).

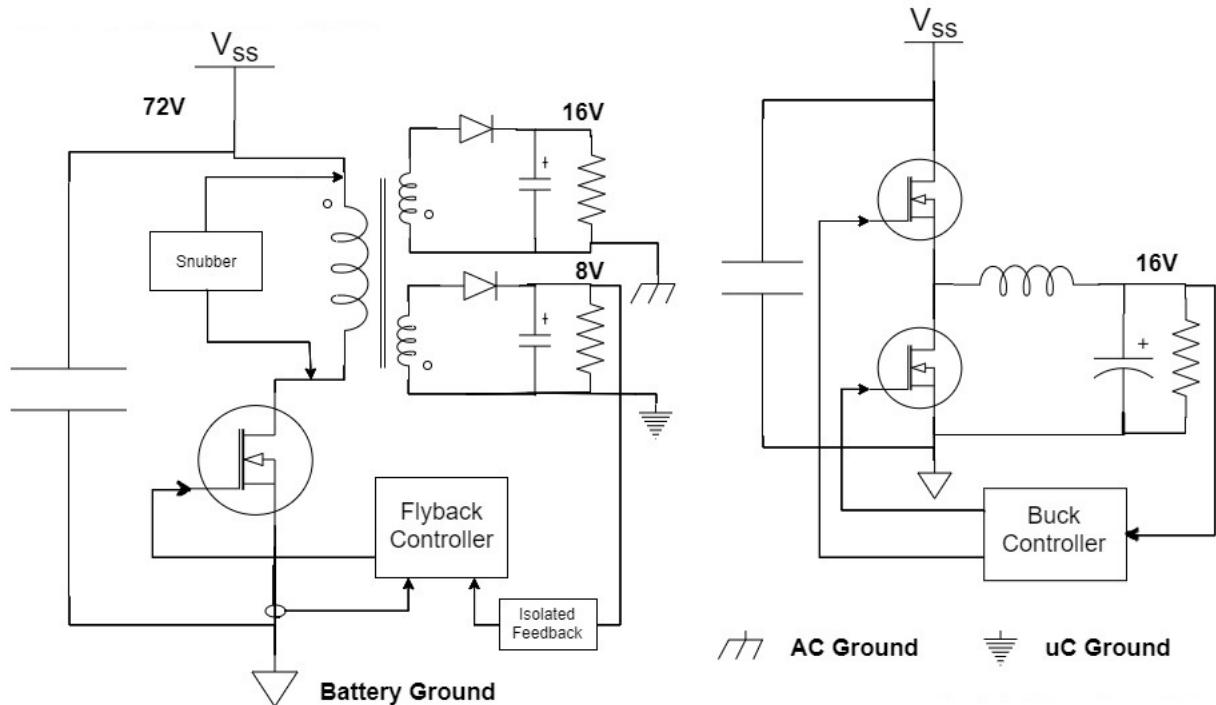


Figure 3.1: Basic Schematic of the Auxillary Power Supply [2]

Control strategy

The figure above shows the preliminary design of the auxillary power supply. The duty control of the Flyback converter can be realized using an inner current programmed control loop and an outer voltage feedback loop. For the buck converter, controlling the output voltage is enough. Suitable controller ICs need to be selected for this purpose.

3.4 Design of the DCM Flyback Converter (24W)

3.4.1 Specifications

The two outputs of the flyback converter (16V on AC ground and 8V on μC ground) will be supplying power mainly to ICs, that need current in the range of a few mA. Considering other aspects of the vehicle, 0.5A is selected for the 16V winding and 2A for the 8V winding, including a safety margin. The maximum power rating is thus 24W, although in nominal conditions, it would be much less. The other specifications are as follows:

- **Input Voltage** V_{dc} : 40V - 60V (since 48V battery was available for prototyping)
- **1st Output Voltage** V_1 : 16V (0.1 - 0.5A) with $\delta V < 5\%$
- **2nd Output Voltage** V_2 : 8V (0.2 - 2A) with $\delta V < 5\%$
- **3rd Output Auxillary Voltage** V_{aux} : 16V (50mA) with $\delta V < 5\%$
- **Output Power** P_o : 24W (max)
- **Switching frequency** f_s : 100kHz
- **Minimum efficiency** η : 75%
- **Controller IC used** : NCP (ON Semiconductor)

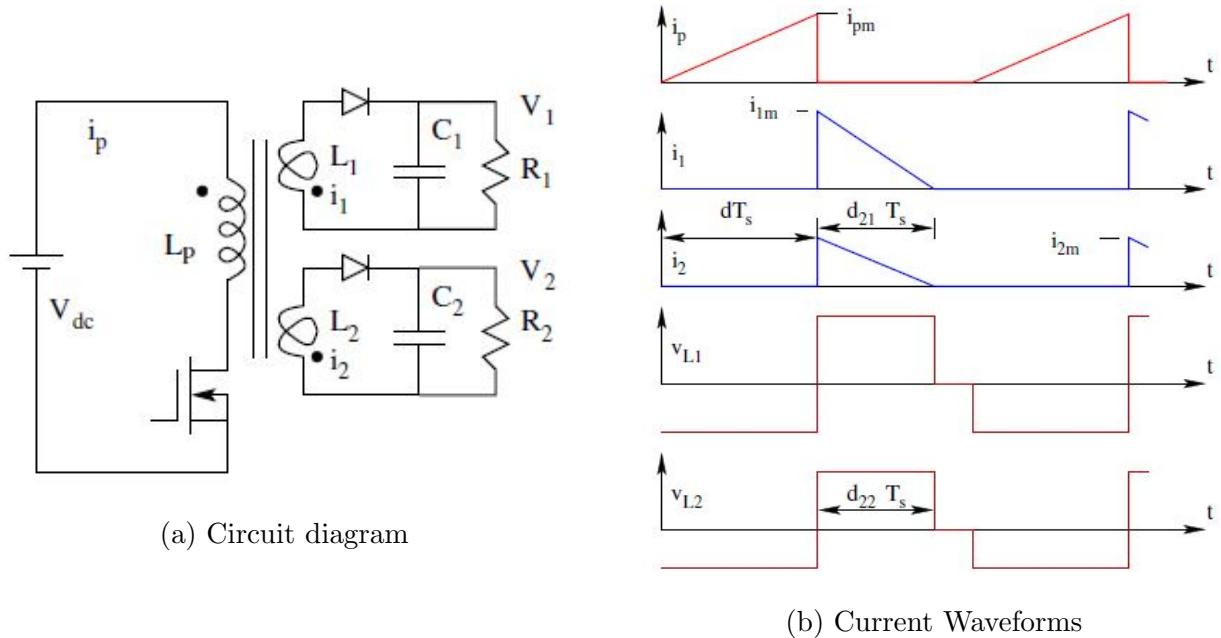


Figure 3.2: Two output DCM Flyback Converter [11, p352]

3.4.2 Preliminary Calculations

$$V_{dc}(\min) = 40V \quad V_{dc}(\max) = 60V$$

Input Capacitor Calculation

$$C_{in} = \frac{I_{inmax}T_s}{2\delta V_{dc}} = \frac{P_o}{\eta V_{dcmin}} \frac{T_s}{2\delta V_{dc}} \quad (3.5)$$

Taking the ripple in the input DC bus (δV_{dc}) to be about 4V, we get $C_{in} = 1\mu F$

Conduction Parameters and Conduction times

From figure 3.2, i_{1m} (and similarly i_{2m}) through diodes D1 and D2 are related to the intervals $d_{21}T_s$ ($d_{22}T_s$) and the load currents by :

$$i_{xm} = \frac{V_x d_{2x} T_s}{L_x} = \frac{V_x}{R_x} \frac{2}{d_{2x}} \quad (3.6)$$

Hence we get $d_{2x} = \sqrt{K_x}$ where $K_x = \frac{2L_x}{R_x T_s}; \quad x = 1, 2$

(If $d_{21} \approx d_{22}$ then the results of the single output flyback can be applied directly).

Evidently, $K_x \propto I_x$, so we have:

$$\frac{K_{1min}}{K_{1max}} = \frac{I_{1min}}{I_{1max}} = \frac{0.1}{0.5} = 0.2 \quad \frac{K_{2min}}{K_{2max}} = \frac{I_{2min}}{I_{2max}} = \frac{0.2}{2} = 0.1$$

Selection of duty ratio d

The preferred operating duty ratio for a flyback converter is below 0.5. The maximum duty ratio chosen for this design is $d_{max} = 0.45$

Range of duty ratio

Voltage transfer ratio: Applying volt-second balance on L_x we get : $V_x = \frac{d}{\sqrt{K_x}} \frac{N_x}{N_p} V_{dc}$

From this we get the range of variation of duty ratio as follows:

$$\frac{d_{max}}{d_{min}} = \frac{V_{dcmax}}{V_{dcmin}} \sqrt{\frac{K_{xmax}}{K_{xmin}}} \quad (3.7)$$

For secondary windings 1 and 2, we get this ratio as 3.35 and 4.74 respectively. Hence the range of duty ratio variation can be assumed to be $(d_{min}, d_{max}) \approx (0.1, 0.45)$ with the nominal duty being 0.27

Selection of Primary Inductance

$$P_{in} = \frac{P_o}{\eta} = V_{dc} \langle I_{in} \rangle = V_{dc} I_{pm} \frac{d}{2}$$

$$I_{pmax} = \frac{2P_{omax}}{\eta V_{dcmin} d_{max}} = 3.5A \quad I_{pmin} = \frac{2P_{omin}}{\eta V_{dcmax} d_{min}} = 1.4A$$

$$L_{pmax} = \frac{V_{dcmin} d_{max} T_s}{I_{pmax}} = 51.4 \mu H \quad L_{pmin} = \frac{V_{dcmax} d_{min} T_s}{I_{pmin}} = 42.8 \mu H$$

Hence an L_p value of $45 \mu H$ was chosen. Note that the nominal output power will not always be $24W$, resulting in lower I_{pmax} and hence a greater value of L_p may also work (useful for selecting “shelf” L_p as explained later). This has to be verified by simulation for the required output loads (as has been done later in section 3.4.4 using a larger L_p).

Condition for DCM

$$K_{crit} = (1 - d_{max})^2 > K_{xmax} = \frac{2L_x}{R_{xmin} T_s} = \frac{2L_x I_{xmax}}{V_x T_s} \quad (3.8)$$

Considering allowance for transients, say d_{max} is 0.5 so, from the inequality above, we get the following for near maximum loads: $L_1 < 40 \mu H$ and $L_2 < 5.55 \mu H$

Turns Ratio selection

Using L_1 and L_2 , we get the turns Ratio: $\frac{N_1}{N_p} = \sqrt{\frac{L_1}{L_p}} < 0.94$ $\frac{N_2}{N_p} = \sqrt{\frac{L_2}{L_p}} < 0.35$

By selecting L_1 and L_2 , we can fix the turns ratio. If a “shelf” transformer with nearly same turns ratio is available, it might be better to consider that first and make slight modifications.

Calculation of Output Capacitors

We know that the output voltage ripple for a capacitor is $\Delta V = \frac{1}{C} \int i_c dt$. Now for output $x = 1, 2$ the load is supplied by the capacitor C_x during approximately $(1 - d_{2x})T_s$ period with a current $I_x = \frac{V_x}{R_x}$. Hence: $\Delta V_x = \frac{1}{C_x} \frac{V_x}{R_x} (1 - d_{2x})T_s$. Also, since $\Delta V_x < 0.05V_x$, and $d_{2x} = \sqrt{K_x}$:

$$C_x > \frac{I_{xmax}}{0.05f_s V_x} \left(1 - \sqrt{\frac{2L_x I_{xmin} f_s}{V_x}} \right) \quad (3.9)$$

Substituting the relevant values, we get: $C_1 > 5 \mu F$ and $C_2 > 42 \mu F$. In general the ESR of the capacitor is more stringent in flyback converter [11, sF.4.16]. Hence, normally much higher capacitor values are selected than what is calculated. Thus, standard values are chosen accordingly.

3.4.3 Flyback Transformer Design (Core Selection)

The flyback transformer is essentially a coupled inductor that stores energy in the air gap of the core. Since the currents are switching at 100kHz, so the core material has to be such that its B-H hysteresis curve has very less area enclosed, otherwise there will be excessive core loss as heat. Ferrite material is hence chosen for the core.[11]

Table 3.1: Physical entities involved in transformer design

Symbol	Description	Typical Value
J	The safe current density for the conducting material	3 A/mm^2
B_m	The maximum allowable flux density for the ferrite material	0.2 T
I_p	The maximum peak input current	3.5 A
I_{in}	The maximum average input current (at V_{dcmin}, P_{omax})	0.6 A
L_p	Primary inductance	$45 \mu\text{H}$
a_w	Cross sectional area of wire	I_{in}/J
A_C	Cross sectional area of the core	to be estimated
A_W	Window area of the core	to be estimated
N	Number of turns to fit in the window area	to be estimated
l_g	Air gap in the core to store magnetic energy	to be estimated
k_w	Fraction of the window area used for windings ($0.3 < k_w < 0.5$)	$Na_w/A_W = 0.4$

The peak flux density in the core due to the peak current in the inductor is related by:

$$LI_p = N\Phi_p = NA_C B_m$$

Replacing the previous relations, we finally obtain:

$$A_C A_W = \frac{LI_p I_{in}}{k_w B_m J} \quad (3.10)$$

This value comes out to be about 390 mm^4 . The smallest core that just exceeds this must be selected. From [10, D.2] or [4], we see that required core could be EE19 or EE16. This can also be verified by the K_g method of core selection as mentioned in [10, s14.4.2]

Note that making a good transformer with low leakage and exact number of turns is a difficult task, since it involves manual manufacturing skills. Hence if a factory made transformer is already available with nearly same standard features, it is better to use that in the design, even though it demands slight modifications. A suitable such standard transformer was found online (Q4344-BL): [1] with nearly the same features. It was perfect for the application. Even though its primary inductance was a little higher than calculated, simulation results (section 3.4.4) showed that the converter would still operate at DCM at nominal loads. The maximum load estimated would rarely be reached and unfortunately if that happens, it will make the converter operate in CCM.

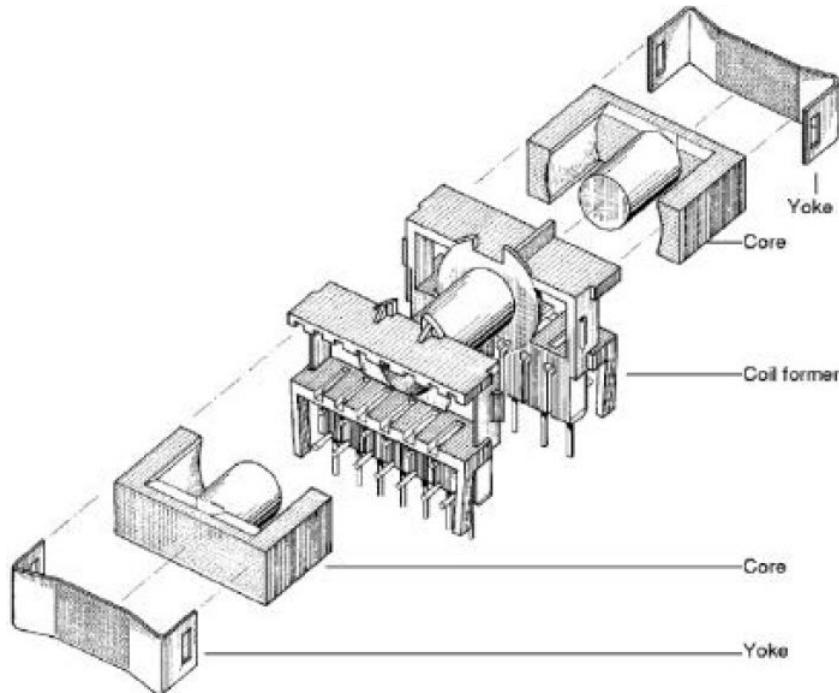


Figure 3.3: Exploded view of the Flyback Transformer with ETD29 core

To test this aspect, a different transformer was also made and tested (with a slightly larger, but readily available ETD29 core). The exploded view of this transformer is shown in the figure above. For this ETD29 core (N87), the core area $A_C = 70mm^2$ (from ETD 29 datasheet). Suitable yoke, bobbins, formers, wires etc. are chosen to make the transformer.

Number of turns

We know that the number of turns $N_p > \frac{LI_p}{B_m A_C} > 11.25$.

As calculated previously, $\frac{N_1}{N_p} < 0.94$ and $\frac{N_2}{N_p} < 0.35$. To make a whole number of turns in each winding, let us select $N_p = 18, N_1 = 15, N_2 = 6, N_{aux} = N_1 = 15$. Winding the turns manually always leads to errors, so increasing N_2 ensures that the relative error is reduced.

Air Gap

The air gap $l_g > \frac{\mu_0 N_p I_p}{B_m} > 0.4mm$. Hence an air gap of 0.5mm is chosen for the core. Note that the two assumptions must hold true after selecting the values:

- **Reluctance :** $R_c \ll R_g$ Air gap reluctance is very high
- **No fringing :** $l_g \ll \sqrt{A_C}$

Wire Size

For DCM operation, rms value of input current: $I_{rms} = I_p \sqrt{\frac{D}{3}}$. For duty 0.5, we get maximum possible rms as $\approx 1.5A$. Hence $a_w = I_{rms}/J = 0.5mm^2 \equiv 21$ SWG

Images of the two selected cores

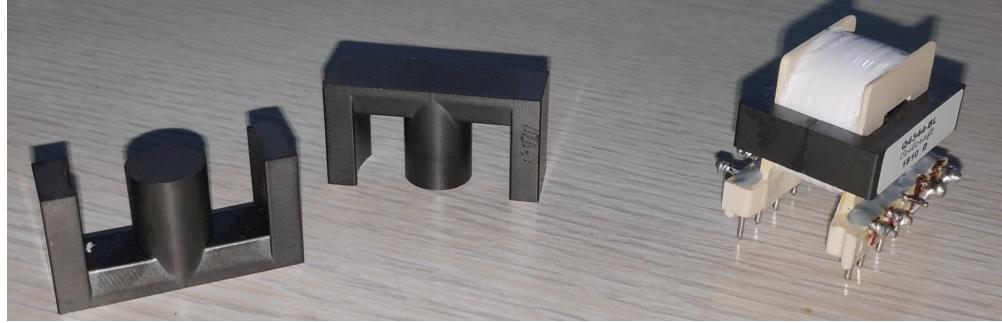


Figure 3.4: Visual comparison between the two cores

3.4.4 Simulation

The following simulation results were obtained for the open loop operation of the flyback using the Q4344-BL transformer (with $L_p = 85\mu H$) at nominal duty and nominal loads. As can be seen clearly, the converter still operates at DCM.

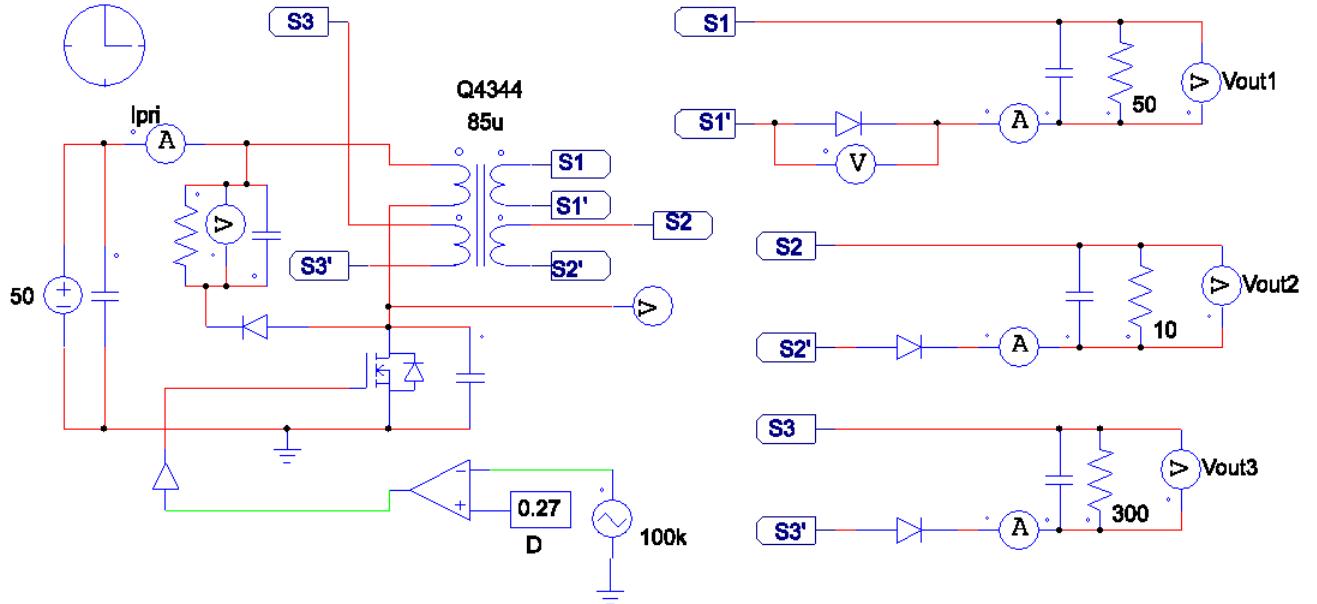


Figure 3.5: Flyback simulation with Q4344 transformer

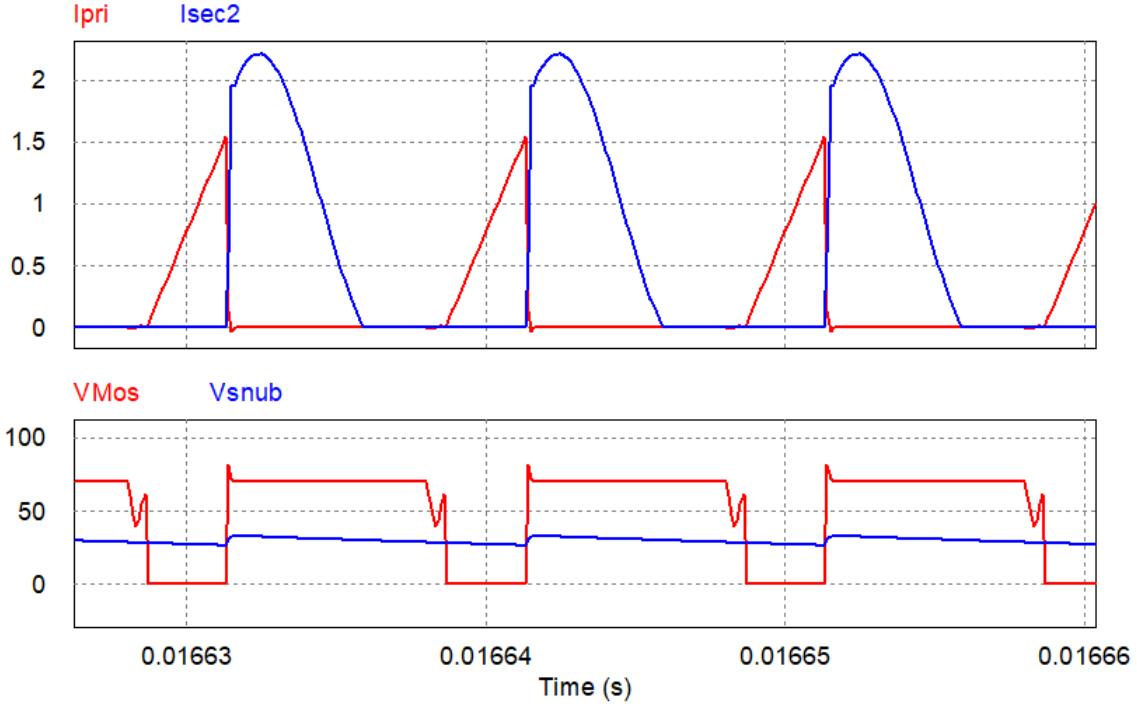


Figure 3.6: Current and output voltage waveforms

3.4.5 MOSFET Selection

$$V_{ds} = V_{dc} + \left(V_1 \frac{N_p}{N_1} + V_2 \frac{N_p}{N_2} + V_3 \frac{N_p}{N_3} \right) + I_{pri} \sqrt{\frac{L_{leak}}{C_{oss}}} \quad (3.11)$$

The last term represents the voltage spike. V_{ds} comes out to be about 160V after calculation. Hence, keeping a safety margin, a 250V mosfet is selected, with $C_{oss} = 180\text{pF}$. The peak primary current is 3.5A, so a mosfet with $I_{ds} = 10\text{A}$ is selected.

3.4.6 Snubber design

A snubber circuit has to be placed across the primary winding to provide a path for the leakage current in order to save the mosfet from burn out due to voltage spike.

$$R_{snub} < 2V_{clamp} \frac{(V_{clamp} - V_{OR})}{L_{leak} I_p^2 f_s} \quad (3.12)$$

$$C_{snub} > \frac{V_{clamp}}{V_{ripple} f_s R_{snub}} \quad (3.13)$$

The RCD Snubber selection was done iteratively as seen in Figure 3.14.

3.4.7 Control using NCP1203 IC

This IC was selected because it has several features:

- Current mode control (inner control loop)
- Voltage feedback (outer control loop)
- Startup circuit (500V HV pin)
- Skip cycle mode (for example at no load)
- Several protection circuits (excess current or Under Voltage Lock-Out)

Since the 8V output is more sensitive, so voltage feedback is taken from it and the other winding is left for being cross regulated. The figure below shows the basic scheme.

Typical Application Example with one secondary winding

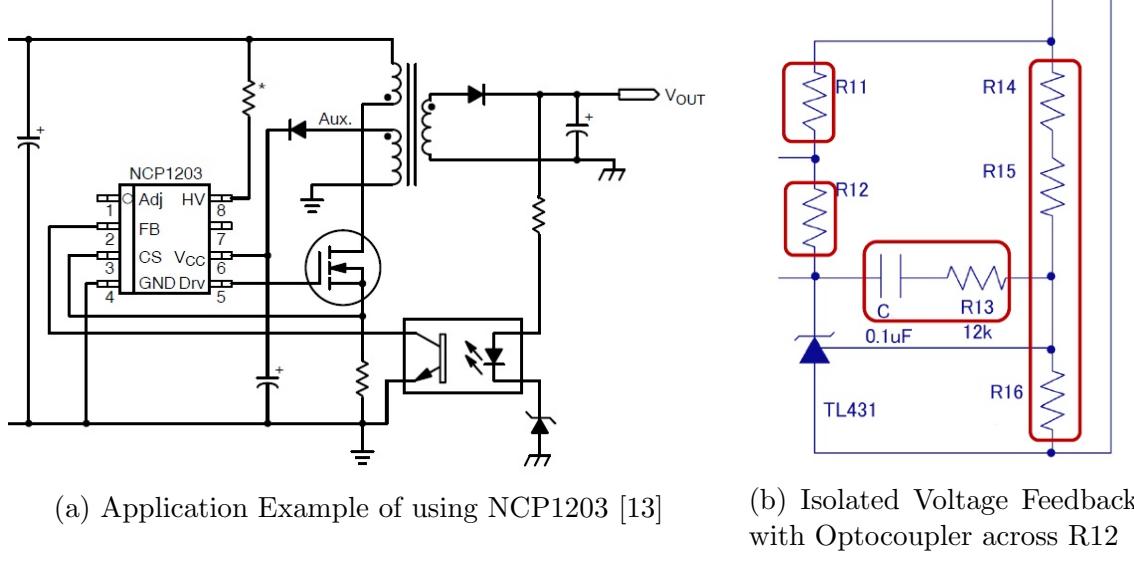


Figure 3.7: Control of the Flyback

The feedback is modified according to the following [12]. TL431 is a shunt regulator that maintains 2.5V across R16. Accordingly, R14, R15 can be selected to regulate 8V output. R12, R11 depends on the current limit of TL431. C and R13 make up the “phase compensating circuit”.

The sense resistor is chosen according to the limiting values at the FB pin as given in [13]. The drive pin is connected to the Mosfet gate through a gate resistance R_g that is typically a few 10s of ohms. A discharge resistor is also placed across the gate-source of the mosfet typically of $10\text{k}\Omega$.

The final schematic is shown in the following section.

3.4.8 Final Schematics and Fabrication

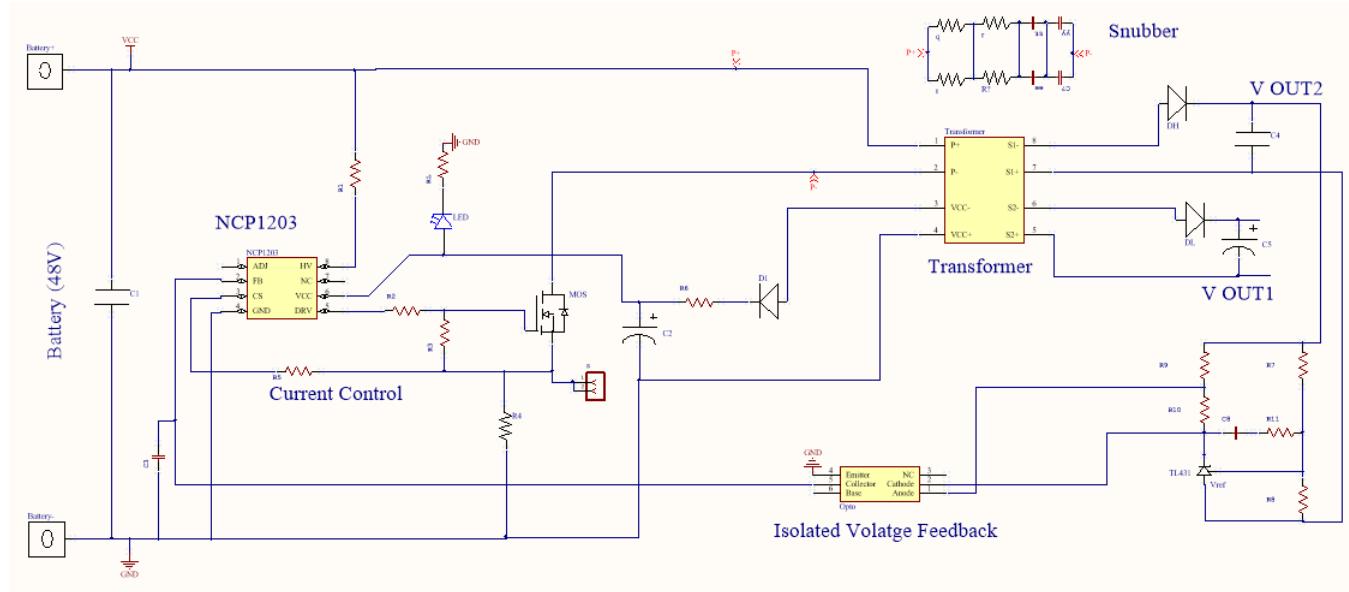


Figure 3.8: Flyback Schematic Drawn in Altium Designer

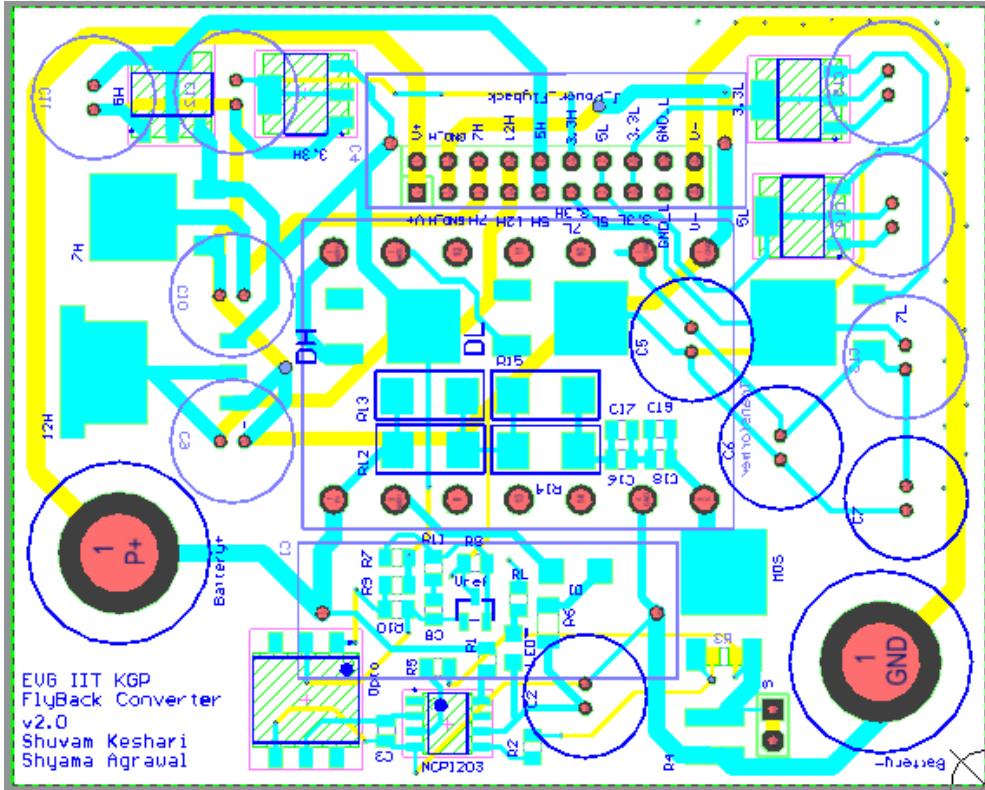
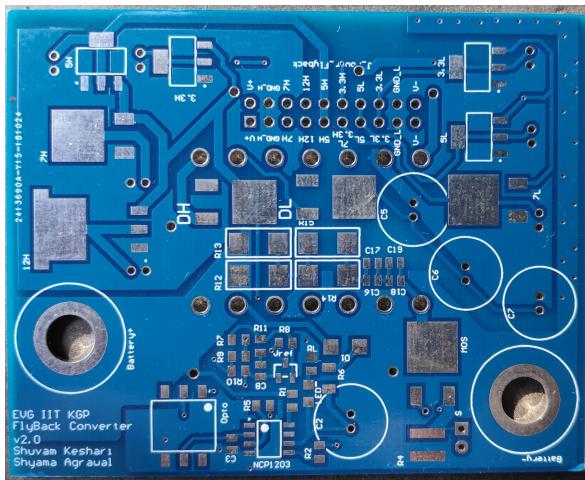
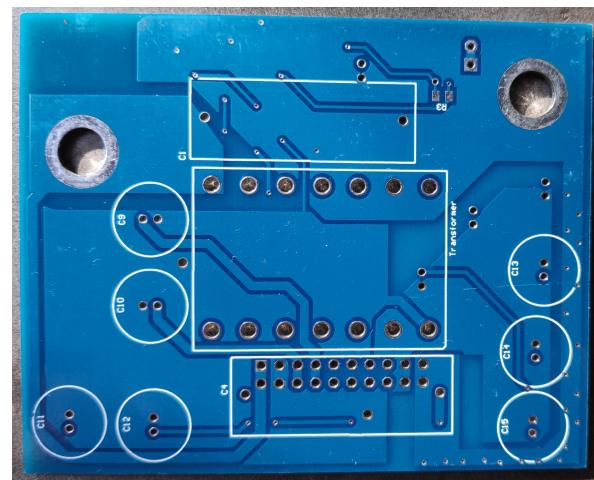


Figure 3.9: Flyback PCB Layout Drawn in Altium Designer



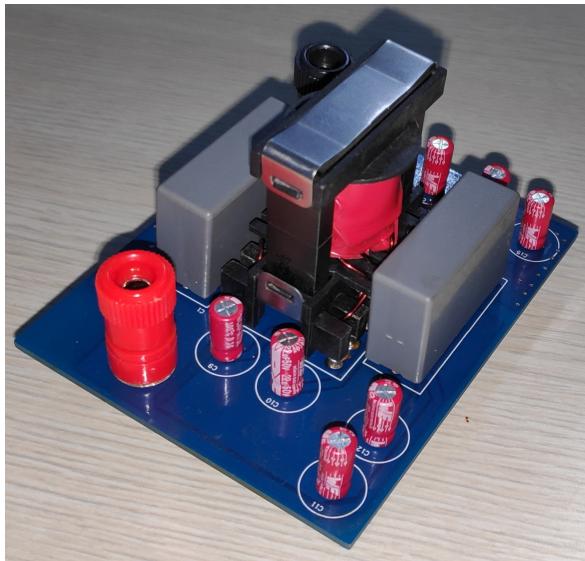
(a) Top Layer



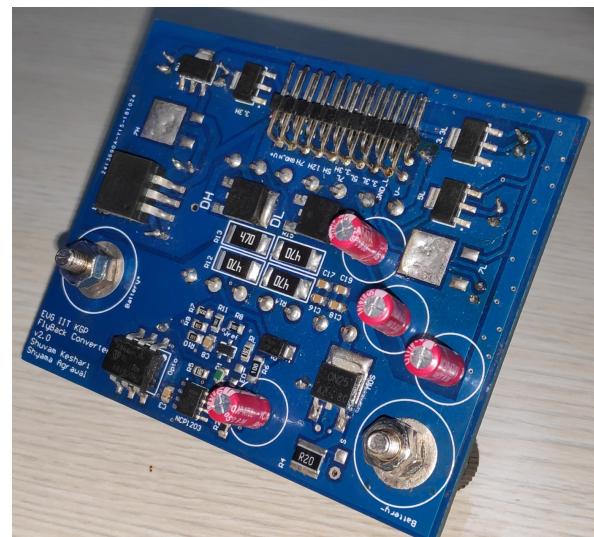
(b) Bottom Layer

Figure 3.10: Flyback Fabrication (80mm by 64mm)

The SMD components were soldered using a heat gun to melt the paste-like solder flux. The through hole components were soldered using a solder wire and a soldering iron.



(a) Through hole & magnetic components



(b) SMD Components

Figure 3.11: Flyback Hardware

3.4.9 Hardware Results

The following hardware results were obtained on testing the flyback converter in closed loop with the NCP IC. The output voltages were just as expected, and the regulation under varying loads was very fast. Different snubbers (combinations of R-C values) had to be used to ensure a proper V_{ds} across the mosfet. An efficiency of about 83% was obtained.

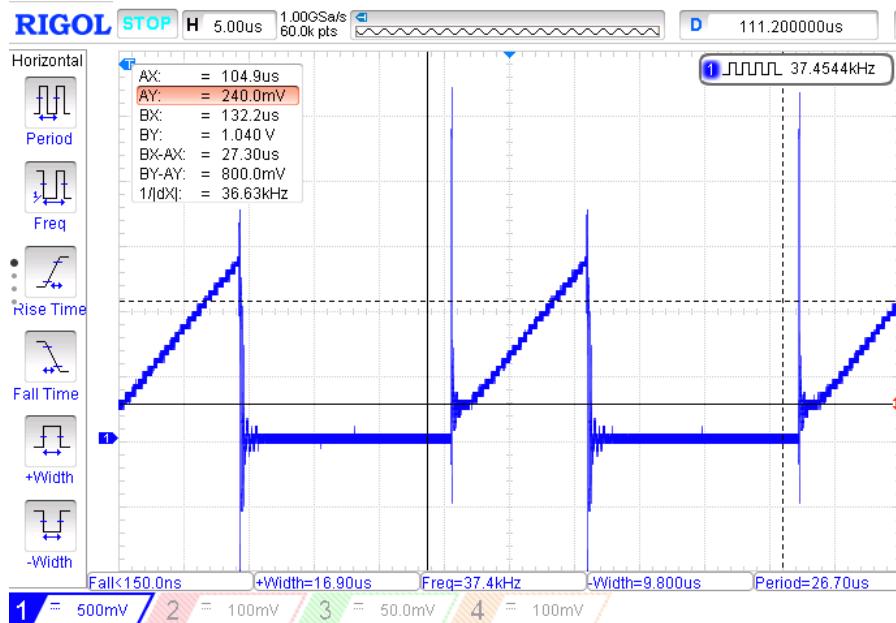


Figure 3.12: Primary current (DCM)

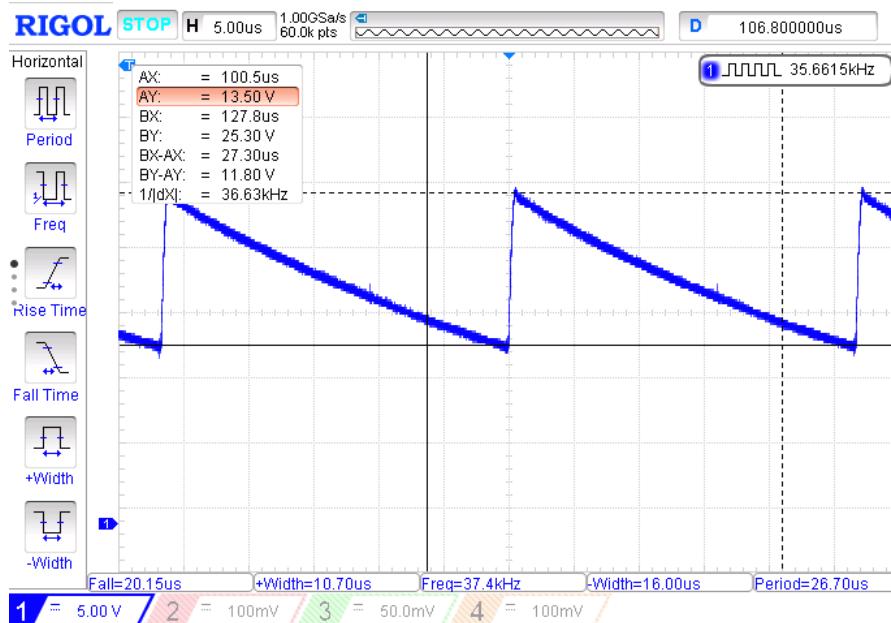


Figure 3.13: Snubber Voltage

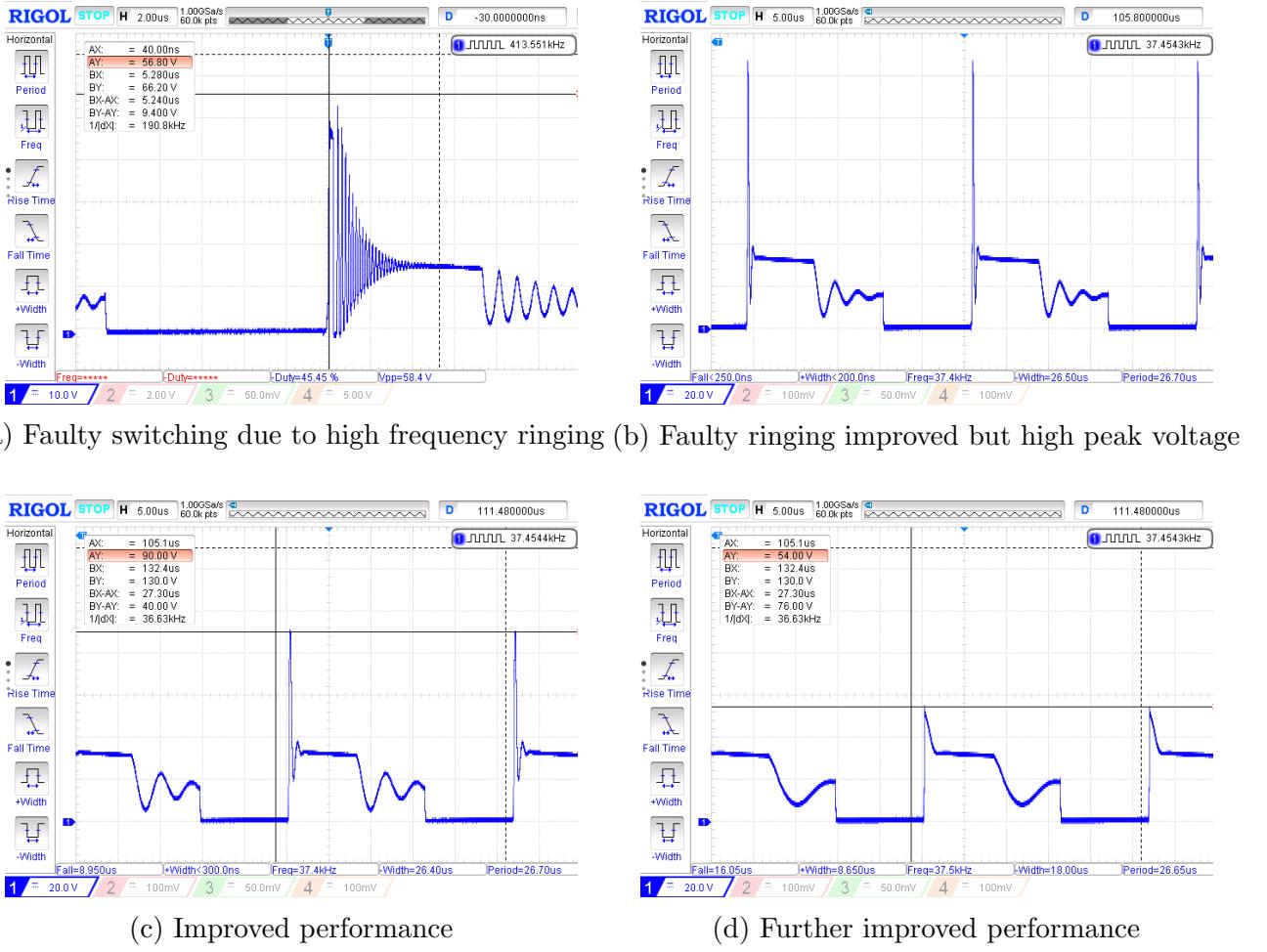


Figure 3.14: Voltage across drain-source of mosfet due to various snubbers

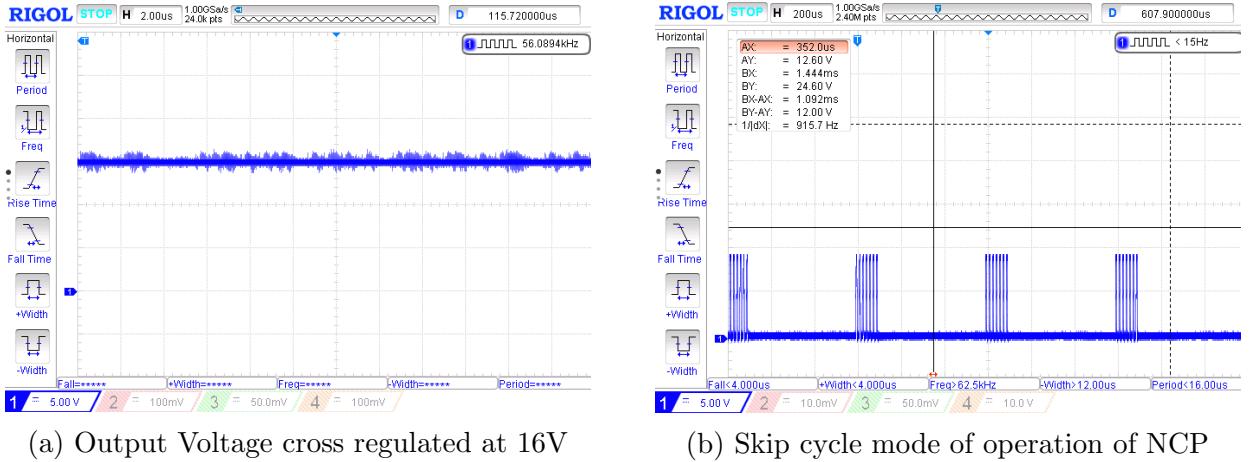


Figure 3.15: Output Voltage and Skip cycle operation

3.5 Design of the Buck Converter (80W)

The buck converter was also designed and tested along with the flyback. However, there were a few issues in the hardware that required a fresh design. For instance, the enable signals were not properly configured and a manual switching resulted in the burnout of the mosfet. Hence the detailed steps for it have not been included in this report. However, the auxillary power supply that was fabricated has been shown in the next section (3.6).

3.5.1 Specifications

The buck converter would be used to supply power to the peripherals, so a current supplying capacity of about 5A is set. The specifications are as follows:

- **Input Voltage** V_{dc} : 40V - 60V (since 48V battery was available for prototyping)
- **Output Voltage** V_0 : 16V (5A) with $\delta V < 5\%$
- **Output Power** P_o : 80W (max)
- **Current ripple** ΔI_L : 0.5A
- **Switching frequency** f_s : 50kHz
- **Minimum efficiency** η : 75%
- **Controller IC used** : TL494 with a gate driver (IRS2184)

3.5.2 Preliminary Calculations

Since the operation is in CCM, we have nominal duty $d = \frac{16}{80} = 0.2$

$$L = (V_{dc} - V_0) \frac{dT_s}{\Delta I_L} = 512\mu H \quad (3.14)$$

$$\text{Maximum ESR} = \frac{\Delta V_0}{\Delta I_L} = 1.6\Omega$$

$$C_{out} > \frac{\Delta I_L}{8f_s \Delta V_0} = 1.6\mu F \quad (3.15)$$

An input capacitor is also needed to ensure that harmonic currents are not drawn from the battery. The following schematic was made in Altium using a design guide for Buck converter. [6]

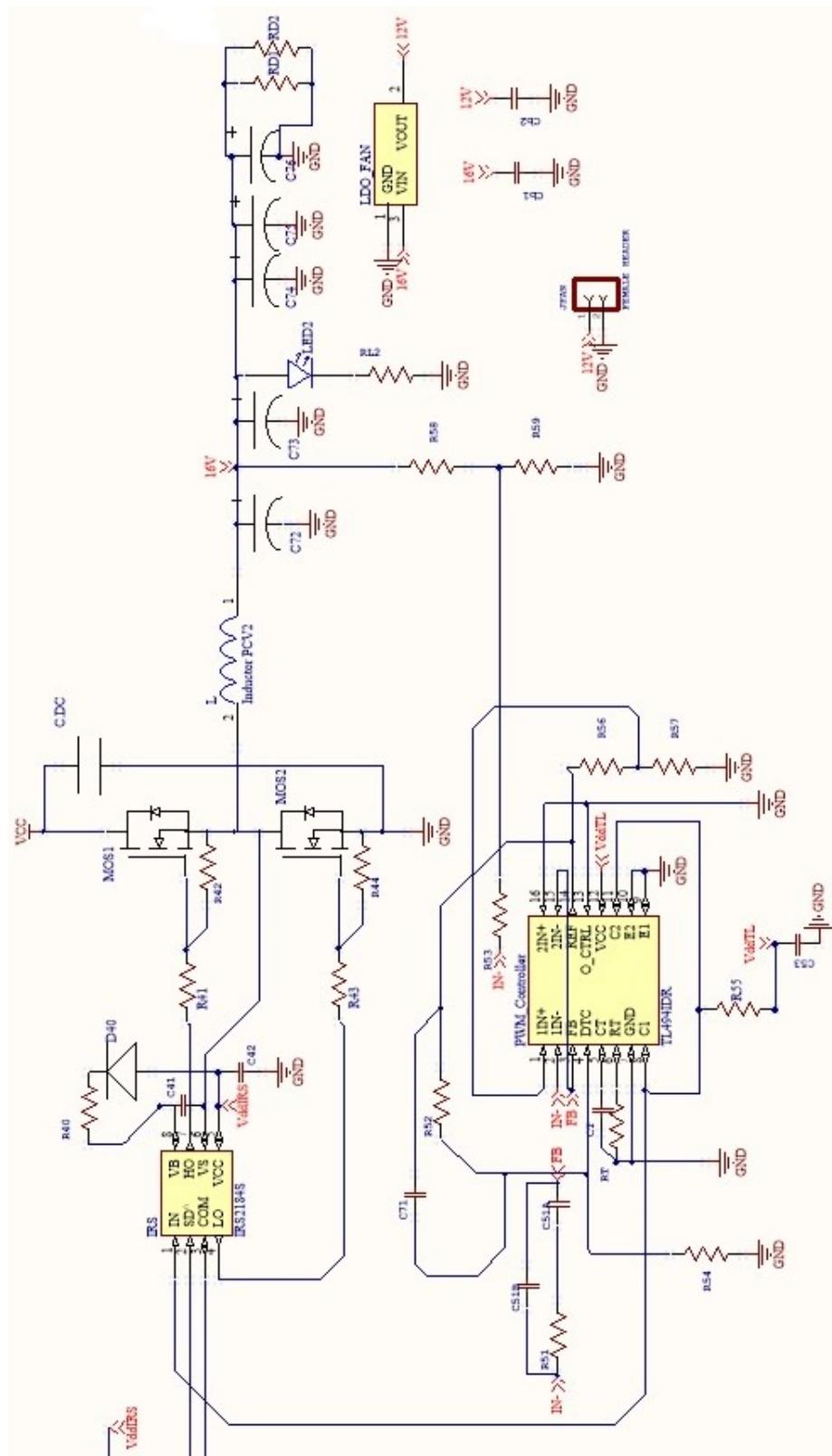
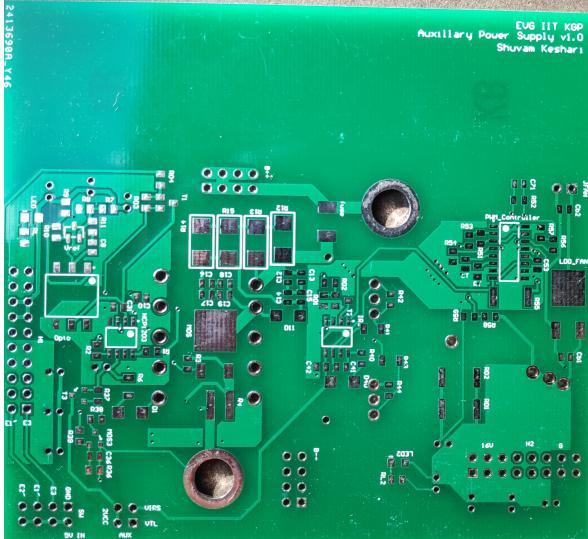


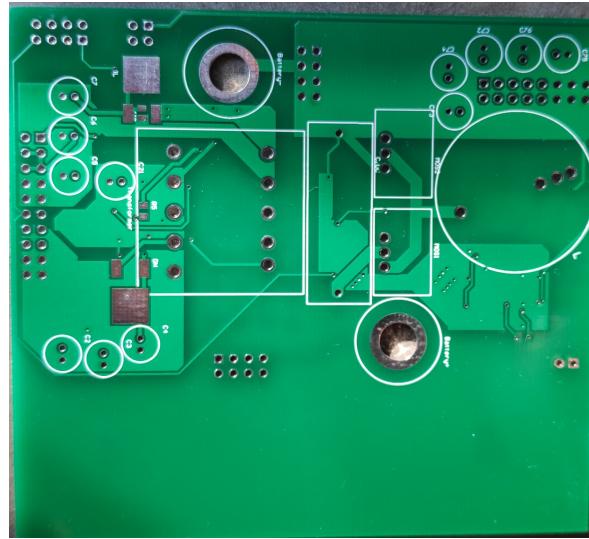
Figure 3.16: Rough Schematic of Buck Converter made in Altium Designer

3.6 Consolidated Auxiliary Power Supply Fabrication

The flyback and buck were combined into a single circuit. The hardware is shown in the following figures.



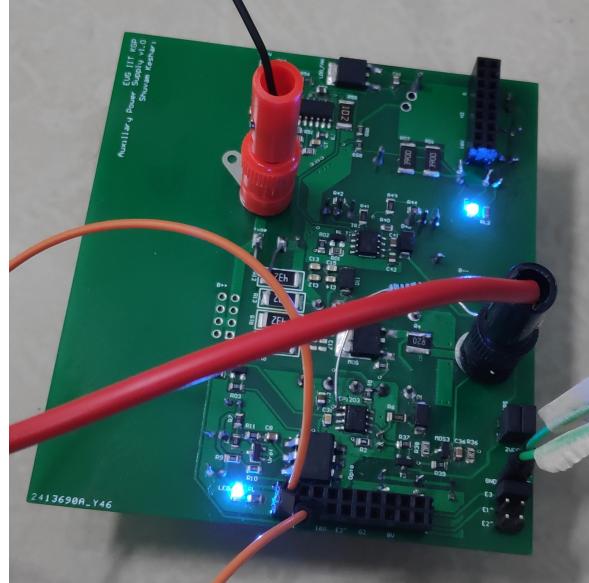
(a) Top Layer



(b) Bottom Layer



(c) Soldered PCB



(d) Working PCB

Figure 3.17: Auxillary Power Supply Hardware Fabrication and testing

The buck converter portion of the circuit had a few issues owing to the enable signals that were being used in the design. Faulty switching resulted in the mos burnout, hence a fresh design is needed with respect to the buck controller IC. This will be done in the next iteration of the circuit, which has already been sent for fabrication.

Power Factor Correction Stage

Charging involves an AC to DC conversion. The non-isolated PFC stage is essentially a boost converter that ensures unity power factor at the input side using certain techniques of current programmed control. The output of this stage is a fairly stable DC voltage that must be higher than the peak of the input sinusoidal voltage. This stage can be interleaved for a higher current rating.

4.1 Specifications

The target specifications for the PFC stage are as follows:

- **Input Voltage** V_{ac} : 200V - 220V (rms, the usual single phase lines in homes)
- **Output Voltage** V_{dc} : 400V (max 8A) with $\delta V < 5\%$
- **Output Power** P_o : 3kW (max, although the hardware was tested for 1.5kW)
- **Switching frequency** f_s : 50kHz
- **Minimum efficiency** η : 85%
- **Controller IC used** : UCC28180

4.2 Input EMI Filter

EMI or electromagnetic interference is caused when the currents switch at 50kHz in the PFC circuit, thus radiating electromagnetic fields.

An EMI filter for a power supply or any converter normally consists of passive components, including capacitors and inductors, connected together to form LC circuits. Common mode chokes are also used. The inductor(s) allow DC or low frequency currents to pass through, while blocking the harmful unwanted high frequency currents. The capacitors provide a low impedance path to divert the high frequency noise away from the input of the filter, either back into the power supply, or into the ground connection.

In addition to assisting to meet EMI regulations, the filter also has to meet safety standards. The inductor temperature rise is measured and for mains operation, the minimum electrical spacing

between line, neutral and ground are controlled. This reduces the risk of fire and electrical shock. The capacitors are also individually safety certified, depending on their position in the circuit. Special “X” capacitors have to be used across the input terminals and “Y” capacitors from the AC circuit to ground.

EMI filter design is in itself a huge area and hence anything more than a qualitative analysis was not achieved in this project.

4.3 Preliminary Calculations

For 1500W output power at 50kHz switching frequency and ripple = 0.25

$$L = \frac{V_{inrms}^2}{P_0 f_s \text{ripple}} \left(1 - \frac{V_{inpeak}}{V_{dc}} \right) = 500\mu H \quad (4.1)$$

4.4 Simulations

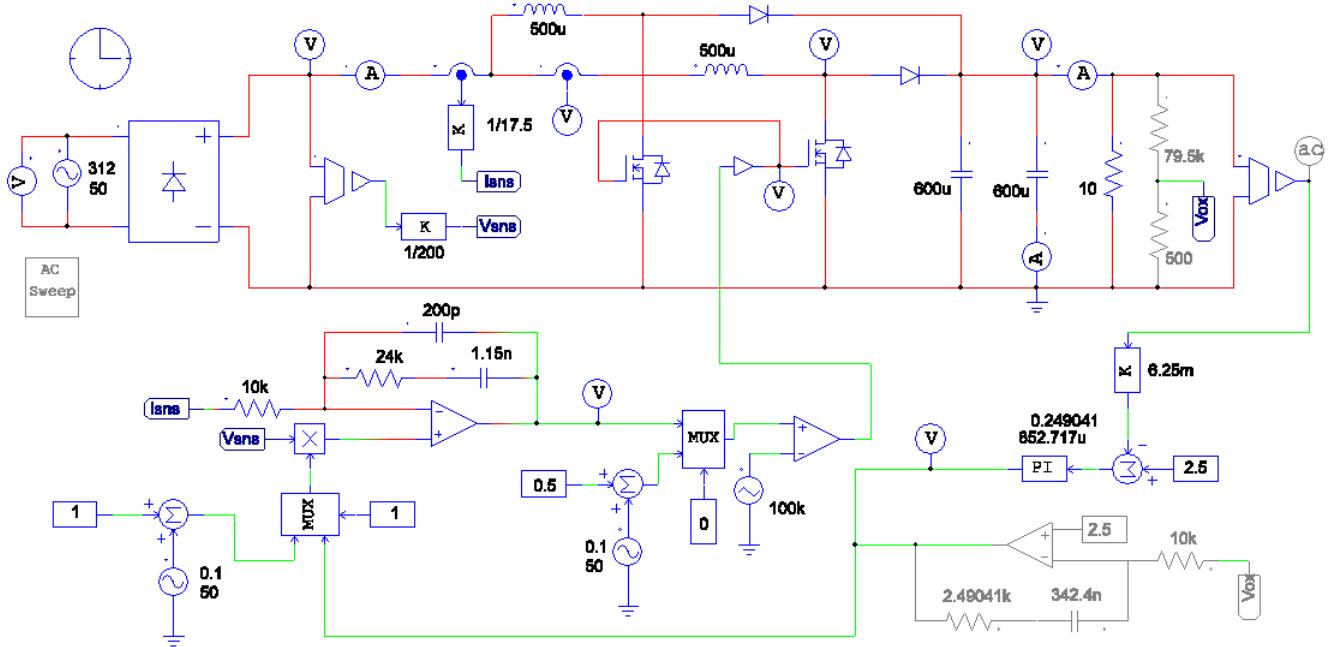


Figure 4.1: Interleaved PFC Simulation without ripple cancellation

The simulation results for the current waveforms show a huge inrush current at the start of the circuit when the outputs capacitors are discharged. This can be avoided by using a resistor in series with the PFC at the start of the circuit and bypassing it using a relay after a few ms.

The power factor obtained by simulation was 0.9994.

The PI values for the simulation was found by the Smart Control feature of PSIM.

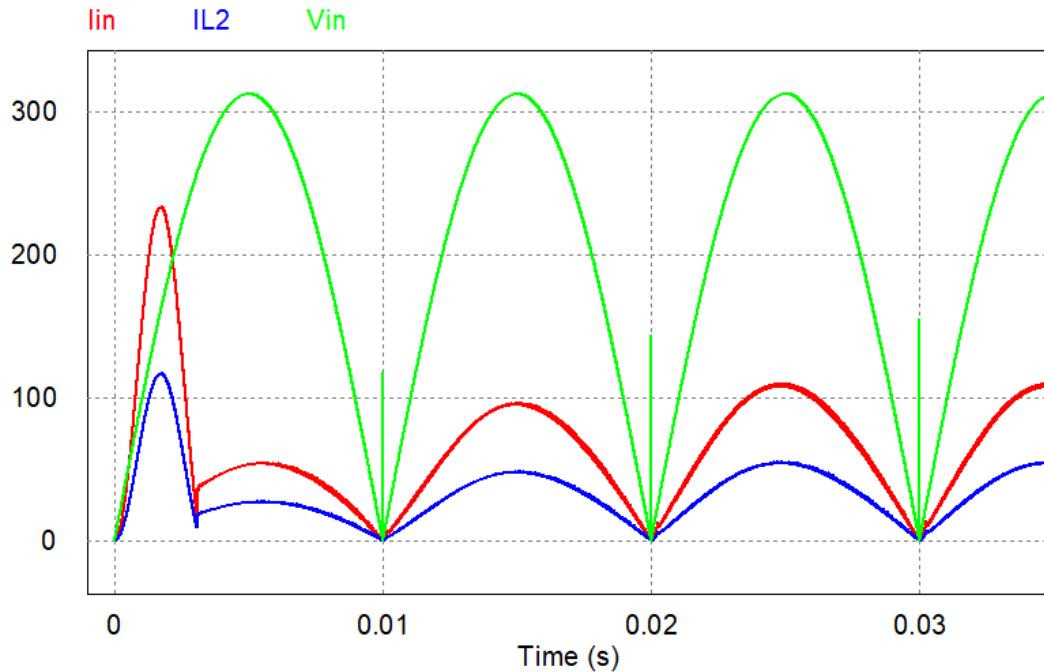


Figure 4.2: Input current waveforms showing improved power factor

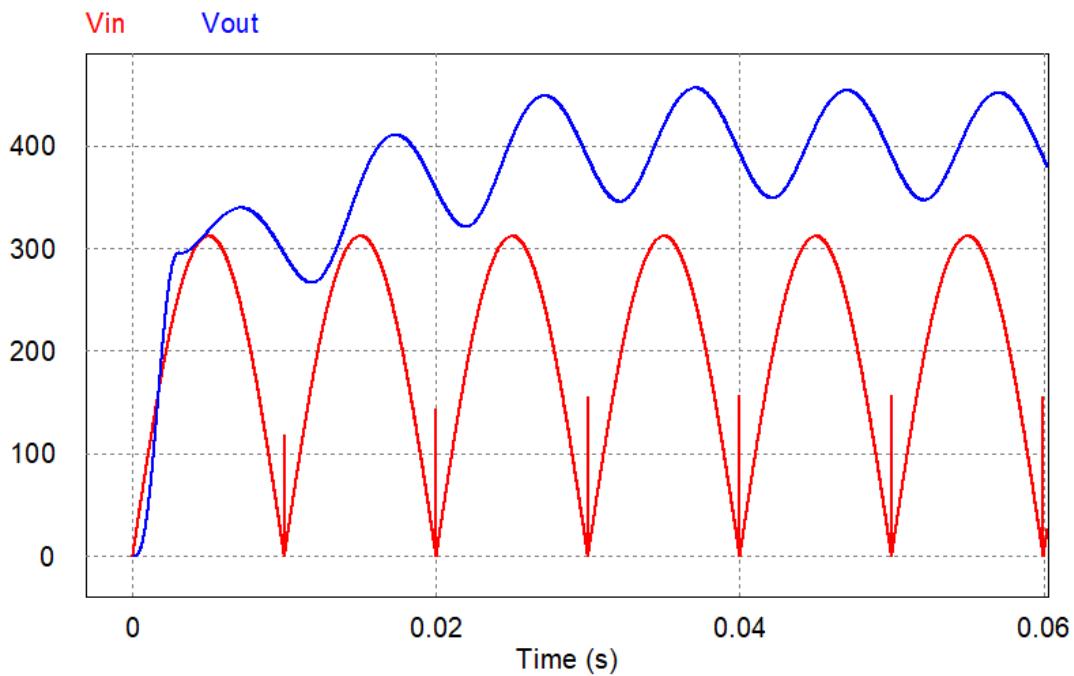


Figure 4.3: Output Voltage waveform

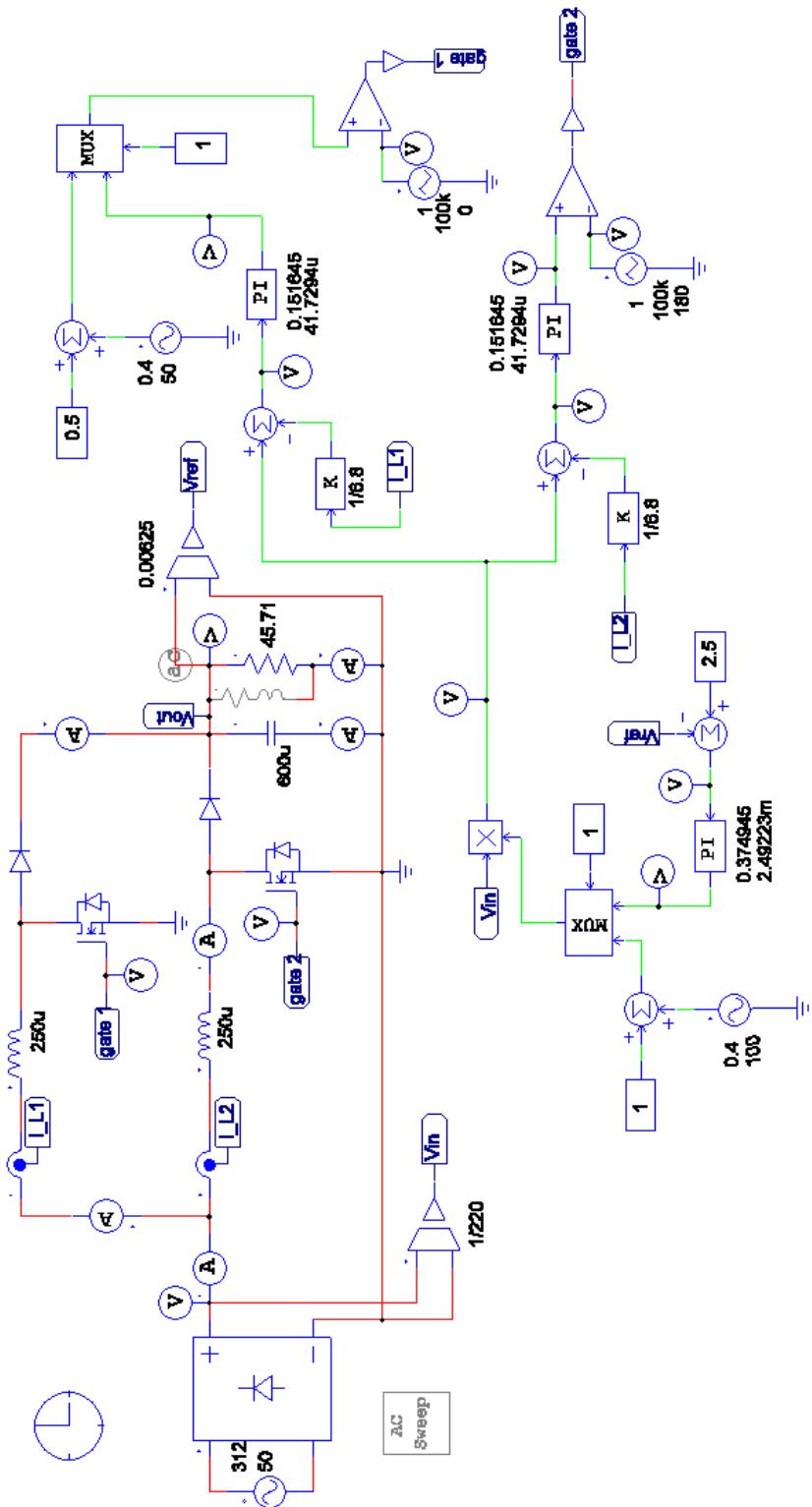


Figure 4.4: Interleaved PFC Simulation with ripple cancellation

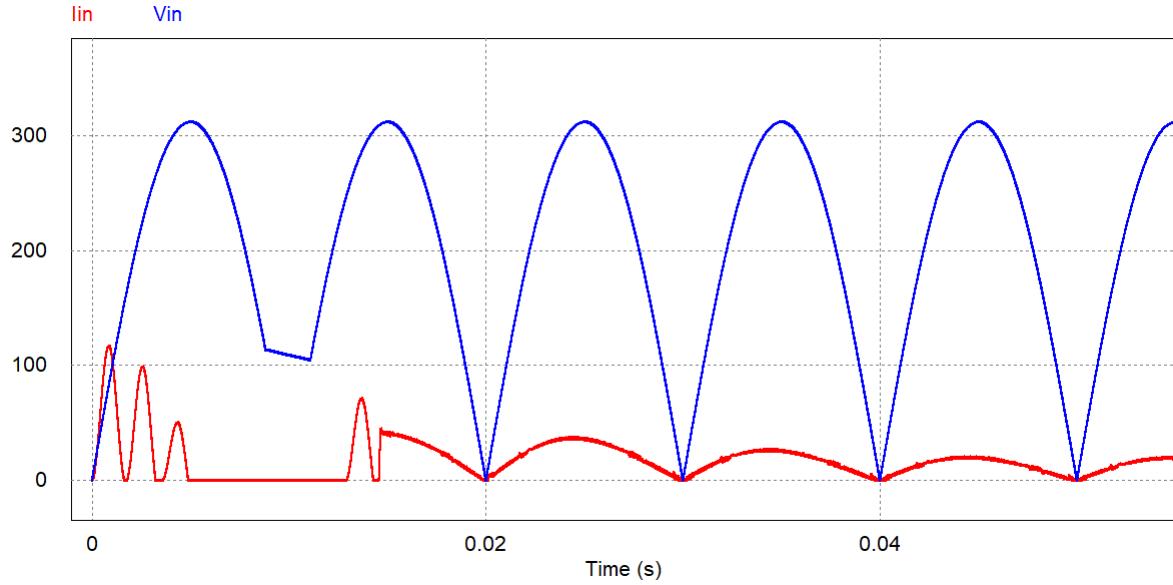


Figure 4.5: Input current waveform showing improved power factor

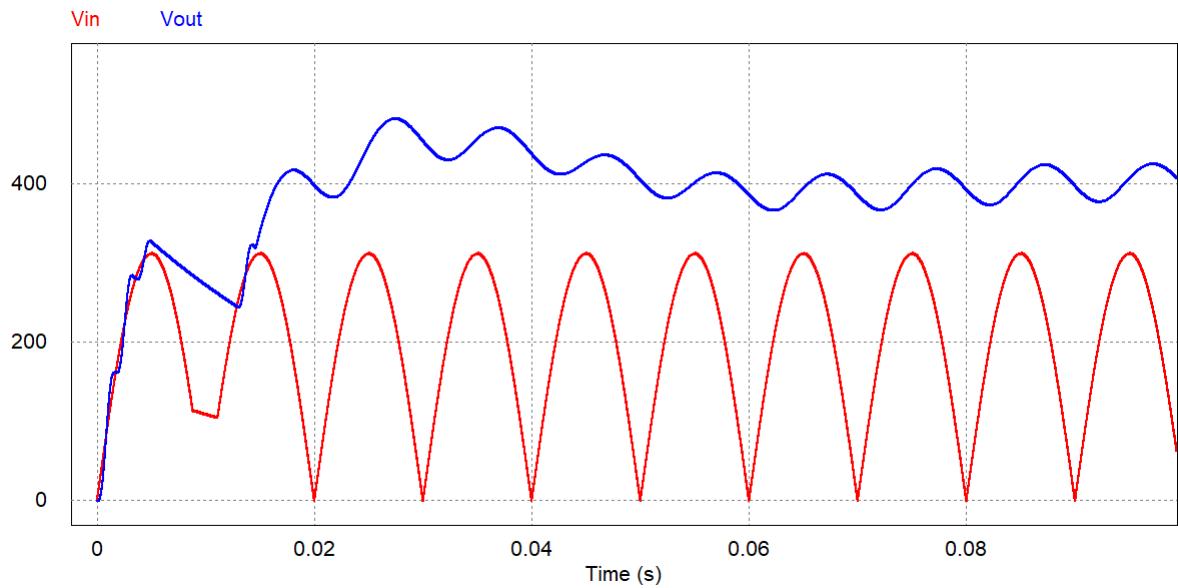


Figure 4.6: Output Voltage waveform for second simulation

From the simulation it can be seen that the circuit is working at 3.3kW.

Ripple cancellation in the two input current waveforms of the two interleaved inductors causes a further improvement of the power factor. This is achieved by a phase delay in the gate signals of the two switches. The following simulation results illustrates this aspect.

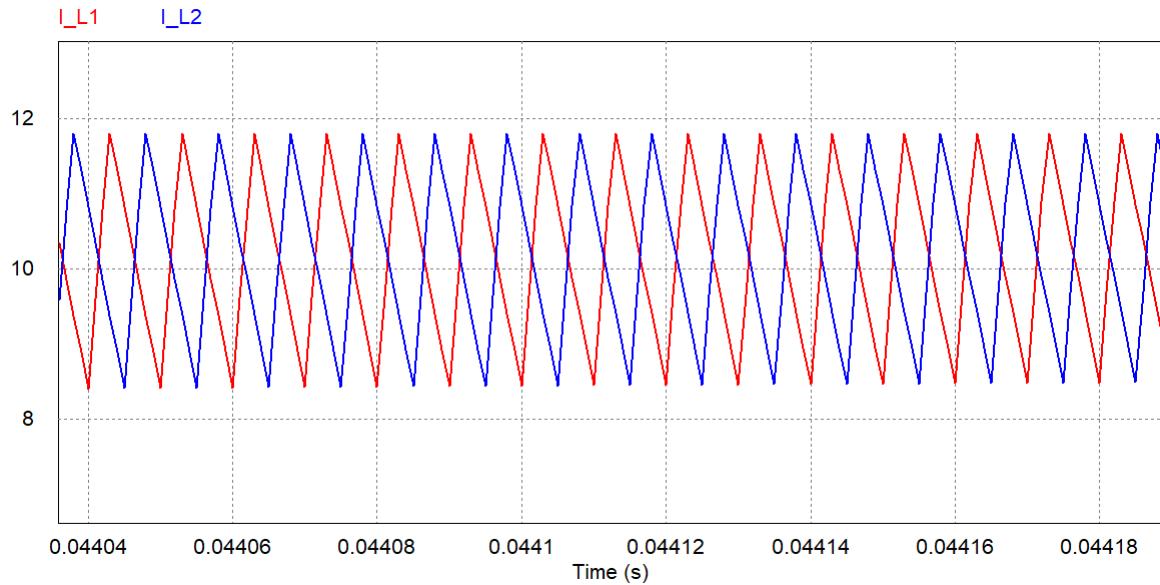


Figure 4.7: Ripple cancellation in the inductor currents

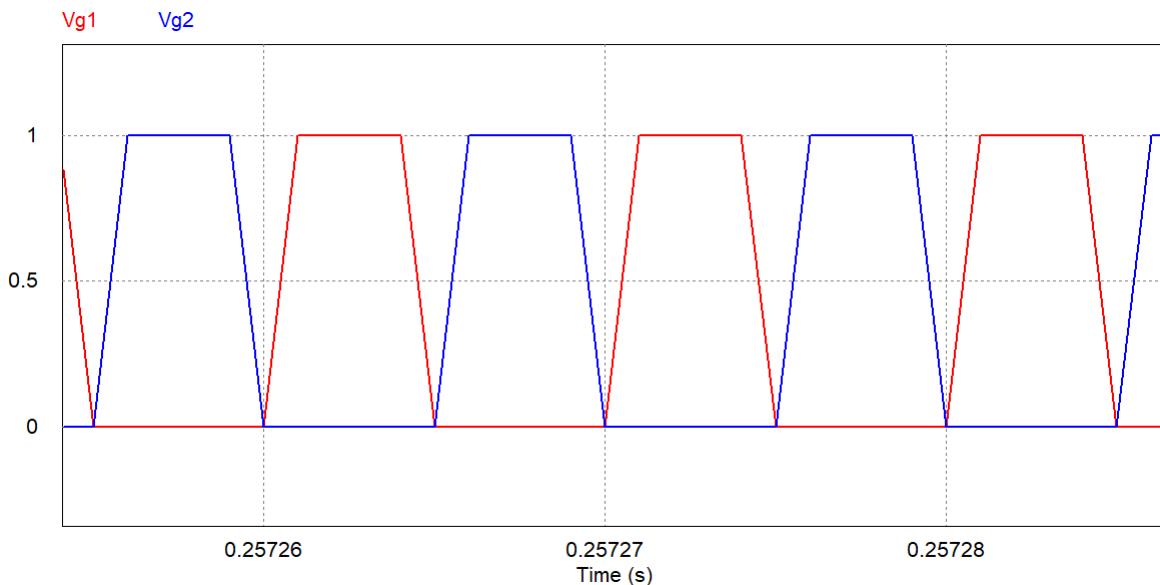


Figure 4.8: Gate signals for the two interleaved switches

4.5 Design of peripheral components

The peripheral components used in addition to the main PFC circuit are as follows:

- **Flyback Converter:** As discussed in section 3.4, the flyback converter is needed to supply regulated power to the various ICs used in the entire circuit.
- **Microcontroller board:** This board houses the processing power of the circuit. It is also used to count time for tripping the relay.
- **Control and sense board:** This board has the controller IC of the PFC circuit. It connects to the main PFC power board as well as to the μ C board and has suitable isolators as well as analog and digital planes in its PCB layout.
- **Gate driver board:** This small board houses the gate driver of the PFC mosfet.
- **Heat sink:** The heat sink holds the diode bridge, PFC mos and PFC diode, each of which is screwed with a mica sheet and thermal paste to prevent short circuit.

All the peripheral boards were also designed individually in Altium designer, taking geometry considerations in such a way that each board fits in a modular way adjacent to the other boards, resulting in a 3D structure.

4.6 Control using UCC28180 IC

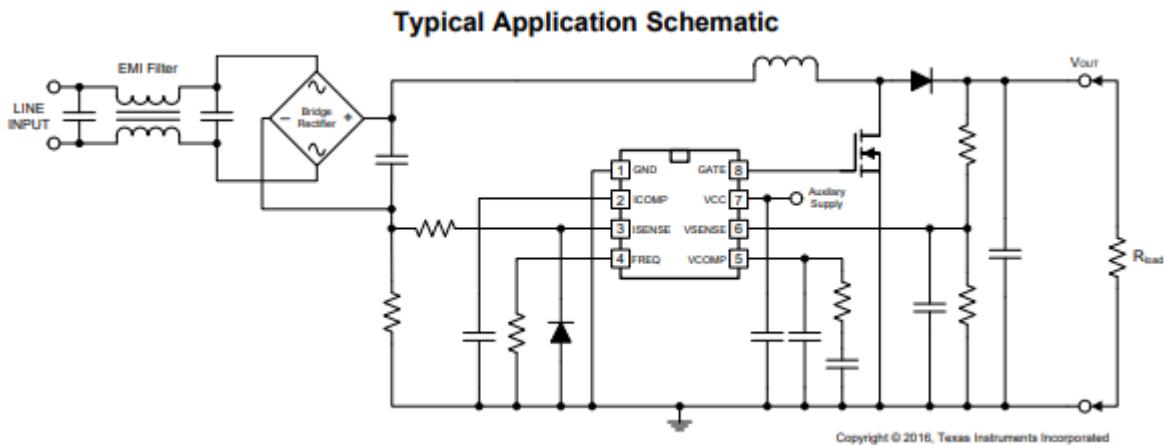


Figure 4.9: UCC28180 basic working scheme

The IC was selected because it has several useful features and is much cheaper than the alternative of doing everything using the microcontroller. [8] refers to the datasheet of the IC. Some of these features are as follows:

- Average Current-Mode Control
 - Soft Over Current and Cycle-by-Cycle Peak Current Limit Protection
 - Output Overvoltage Protection With Hysteresis Recovery
 - Audible Noise Minimization Circuitry
 - Open Loop Detection
 - Burst Mode for No Load Regulation
 - VCC UVLO, Low ICC Start-Up (max 75 μ A)

4.7 Final Schematics and Fabrication

The final schematics made in Altium Designer are as follows:

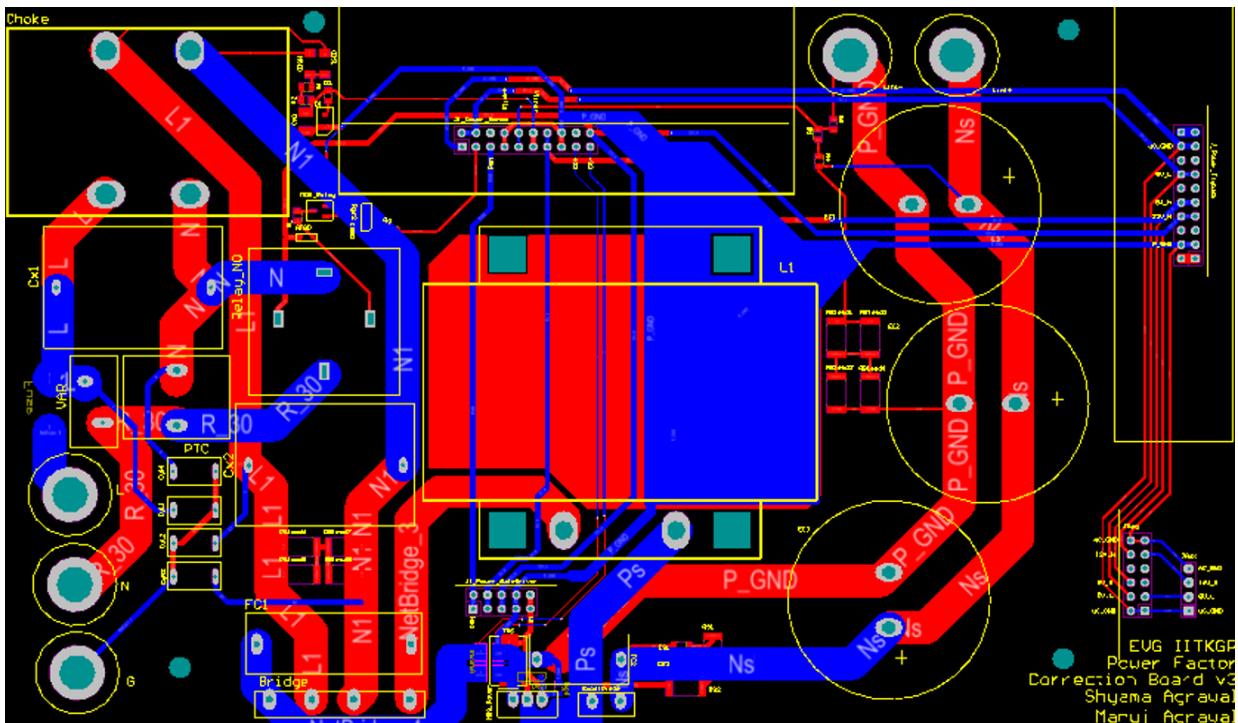
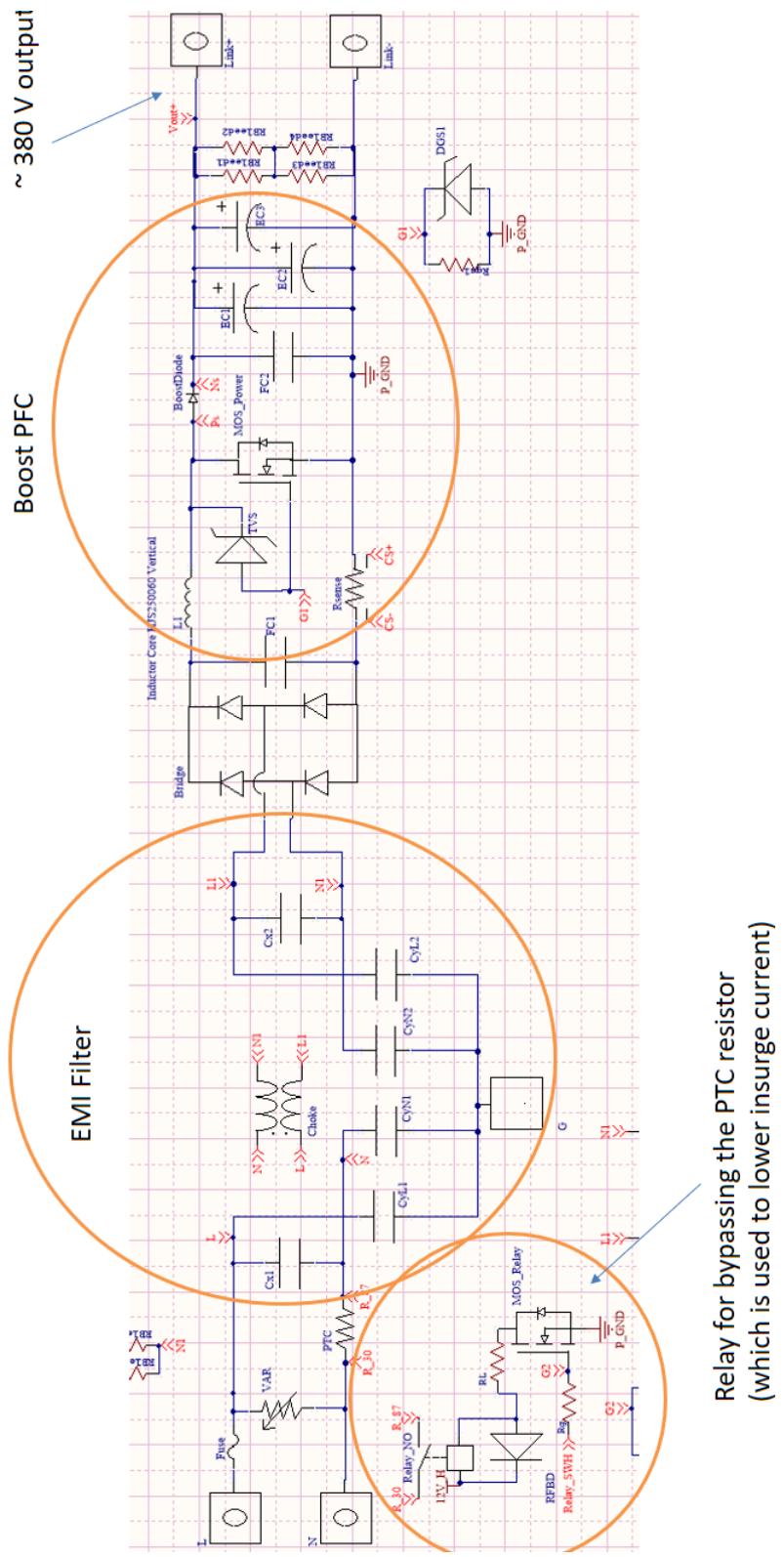


Figure 4.10: PCB Layout of PFC

The image above shows a two layered PCB made for the circuit. Blue denotes the bottom layer and red, the top layer. The ICs are soldered onto it using a soldering station.

The corresponding schematic is shown below. Note that the headers shown imply that a different board is connected to it (or more accurately, mounted on it).

Altium Schematic for the Power Factor Correction circuit (1st stage of the charger)



4.8 Hardware Results

The image below shows in detail all the different components used in the PFC circuit. Owing to its modular structure, there are no loose wires hanging around.

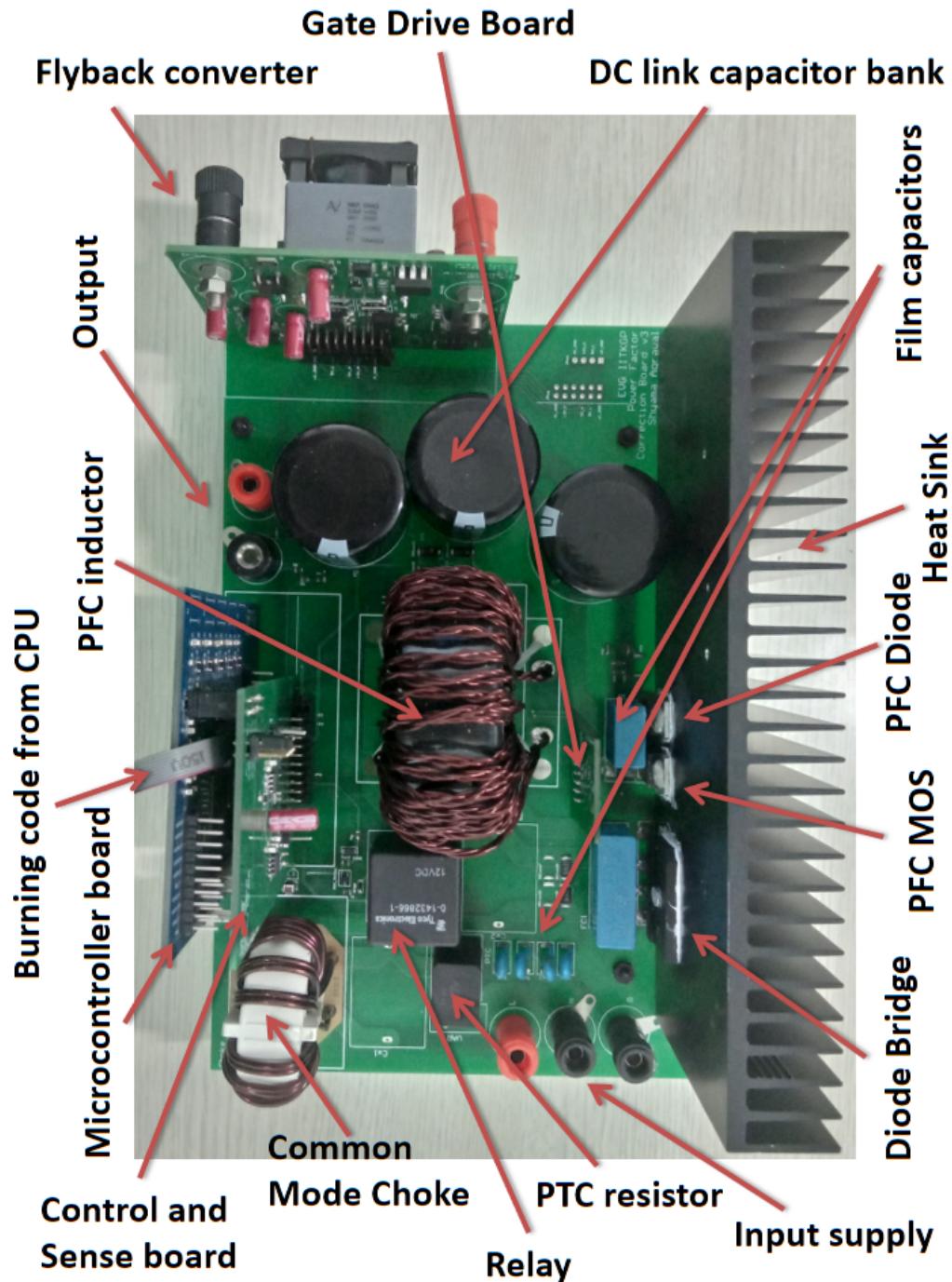


Figure 4.12: The fabricated and soldered hardware for PFC

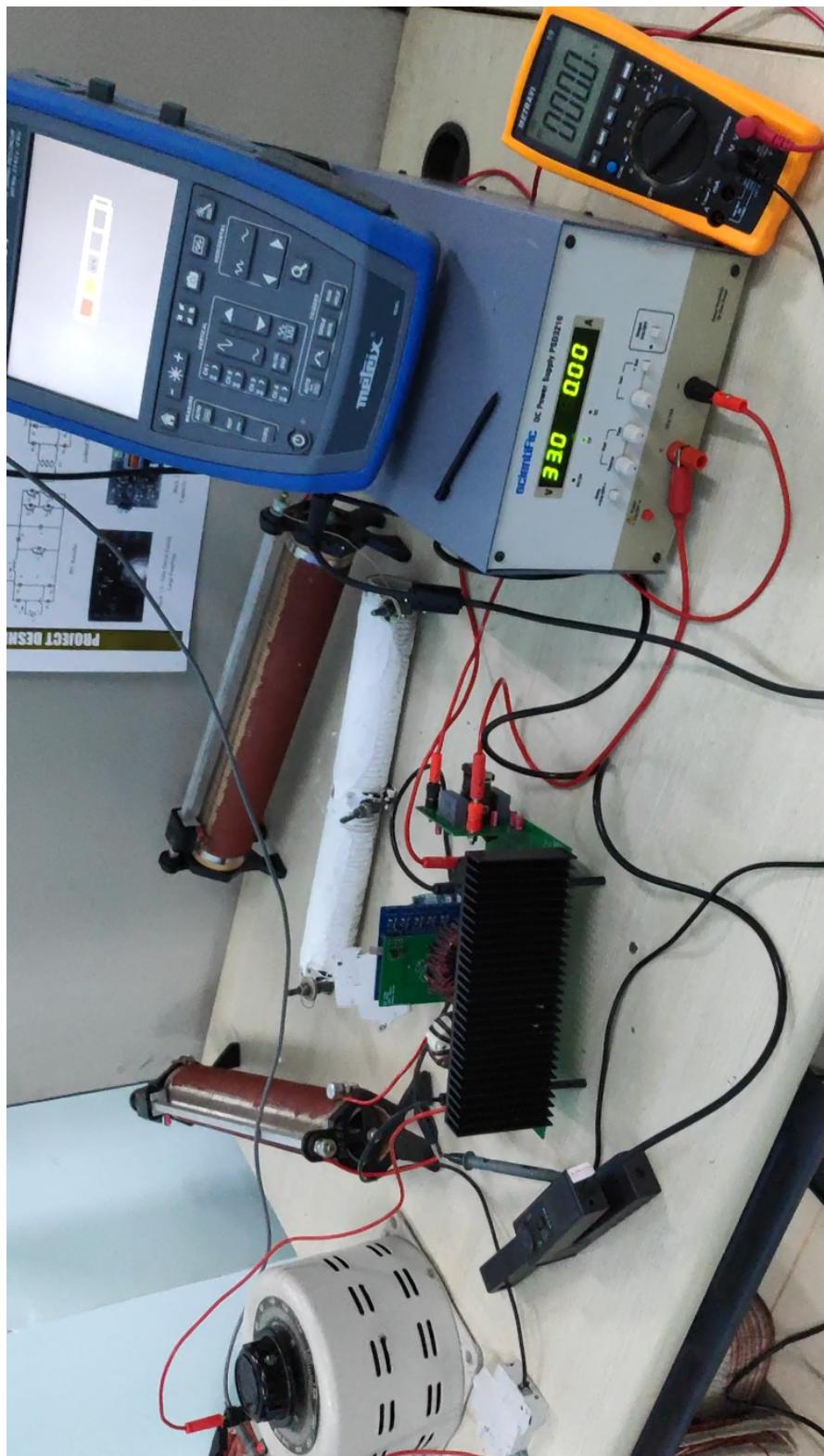


Figure 4.13: Testing Setup for the PFC circuit (CRR Lab 502, IITKGP)

4.8.1 Testing Procedure

With reference to the diagram 4.13, we shall follow these testing steps:

1. The input port of the PFC circuit is connected to an auto transformer (220V rms) through a switch.
2. The output load is passed through rheostats that are kept at around 125Ω total in series.
3. The flyback converter is supplied with a power supply to power the ICs of the circuit.
4. Input voltage and current are measured on the oscilloscope, whereas the output voltage is measured on the multimeter.
5. We start the circuit by supplying the input voltage (220V rms) from the auto transformer. The power to flyback is kept off. During this time, the output capacitor (DC link) voltage can be observed rising (circuit is complete through the PTC resistor), although there is no input current (the relay is not triggered and there are no gate pulses to the PFC mos).
6. Then we turn on the flyback converter, which immediately turns on the microcontroller and the other ICs. The microcontroller is programmed to count 15 seconds before tripping the relay to bypass the PTC resistor. This time is essential as it prevents the initial insurge current from frying the circuit.
7. As soon as the relay is tripped, the output load is engaged by turning on the load switch. After tripping the relay, the microcontroller counts another 10 seconds before it allows the PFC to start working. This enables us to see the bad power factor of the circuit without the PFC.
8. As can be seen the output load is passed through a rheostat that is kept at around 125Ω .
9. Once the PFC starts working, we can see the improvement in the power factor. The output voltage was about 400V resulting in a power output of about 1.3kW. (The wires of the rheostat were heating up very fast at these power levels and hence a gangue rheostat is planned to be procured).

4.8.2 Final waveforms

Here are the final waveforms of the tested PFC circuit. The noise observed in these waveforms could be caused by a number of factors. Line harmonics and lack of EMI filter could be two of them. But the overall working of the circuit can be seen clearly and can be improved by using a proper EMI filter.



Figure 4.14: Bad power factor without the PFC



Figure 4.15: Power factor improved to approximately unity

Phase-shifted Full Bridge Converter

The second stage of the charger is an isolated DC-DC stage for conversion to a lower voltage value and controlling current into the battery. PSFB topology is suitable for the 3kW design target (other alternative being FB-LLC) because of several reasons:

- Constant frequency operation
- Easily synchronized for parallel current sharing operation
- ZVS can be achieved with lower losses, lower EMI
- High efficiency
- CC/CV modes of charging incorporated

5.1 Specifications

The target specifications for the PSFB stage are as follows:

- Input Voltage V_{dc} : 400V (max 8A) with $\delta V < 5\%$
- Output Voltage $V_{battery}$: 80-85V max during CV charging mode
- Output Current $I_{battery}$: 40A max during CC charging mode
- Output Power P_o : 3kW
- Switching frequency f_s : 100kHz (switches)
- Minimum efficiency η : 85%
- Controller IC used : UCC28951

5.2 Simulation

The image below shows the output current being controlled at 32A (set reference). Output voltage can also be controlled, the mechanism for which will be discussed in section 5.5.

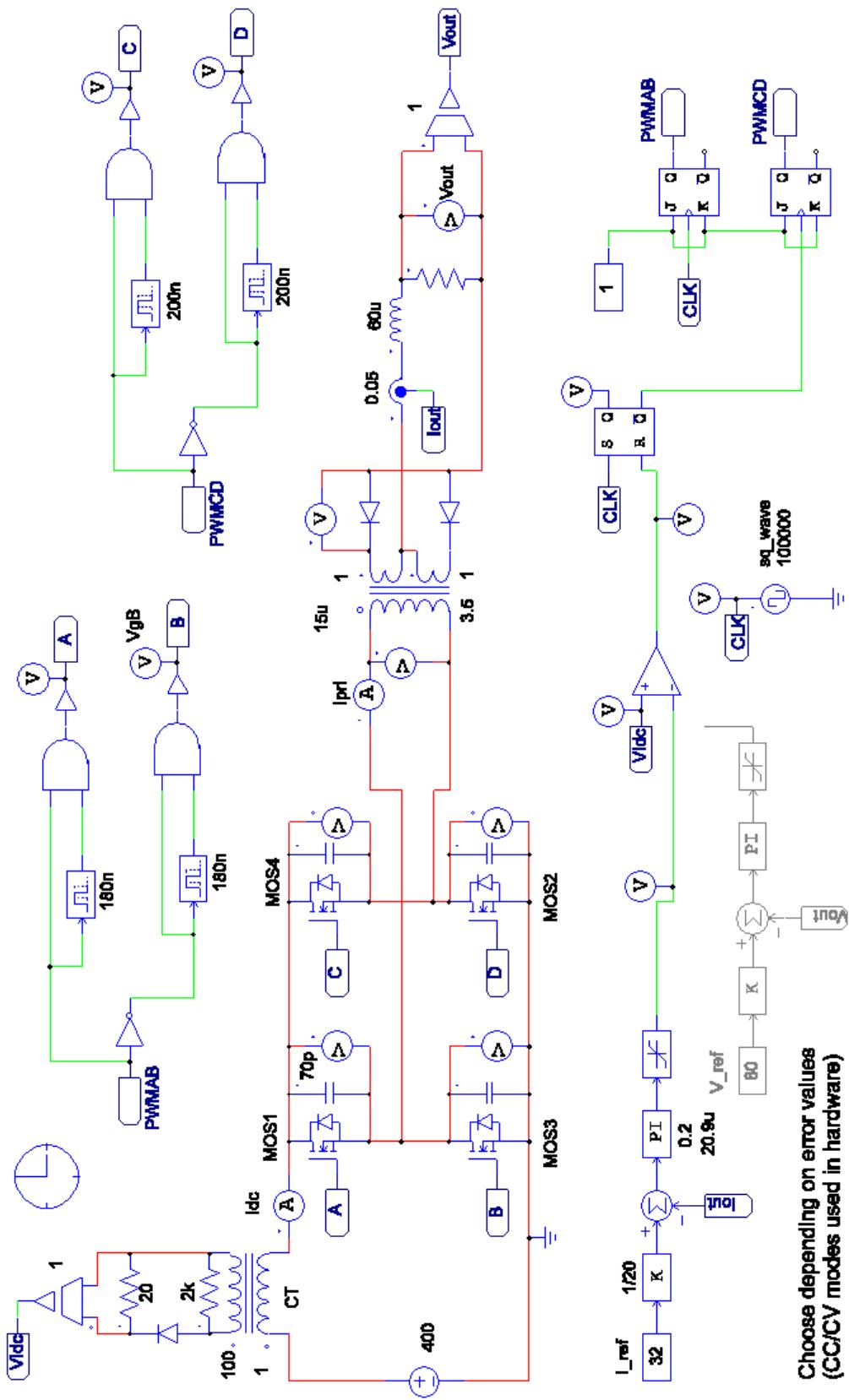


Figure 5.1: PSFB simulation with output current control (at 32A)

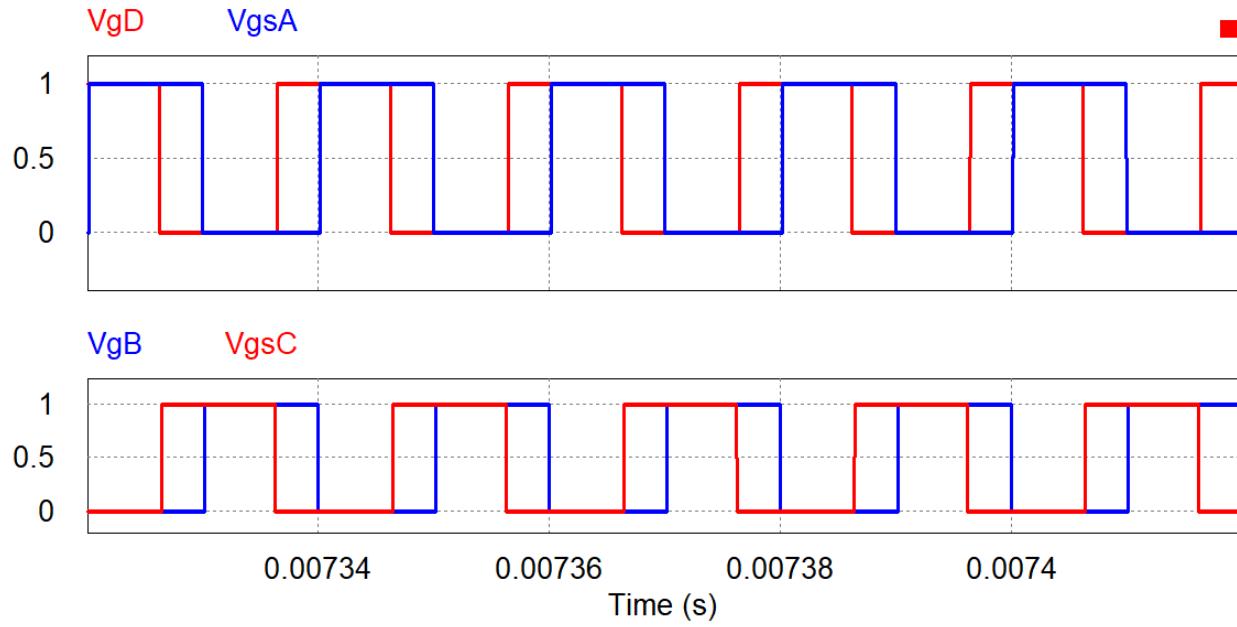


Figure 5.2: Gate signals of the 4 primary switches

The figure above shows gate signals for switches A and B (blue) are reference. That of C and D are phase shifted to achieve the PSFB mechanism. Note that AB and CD are complementary with a certain deadtime (about 200ns).

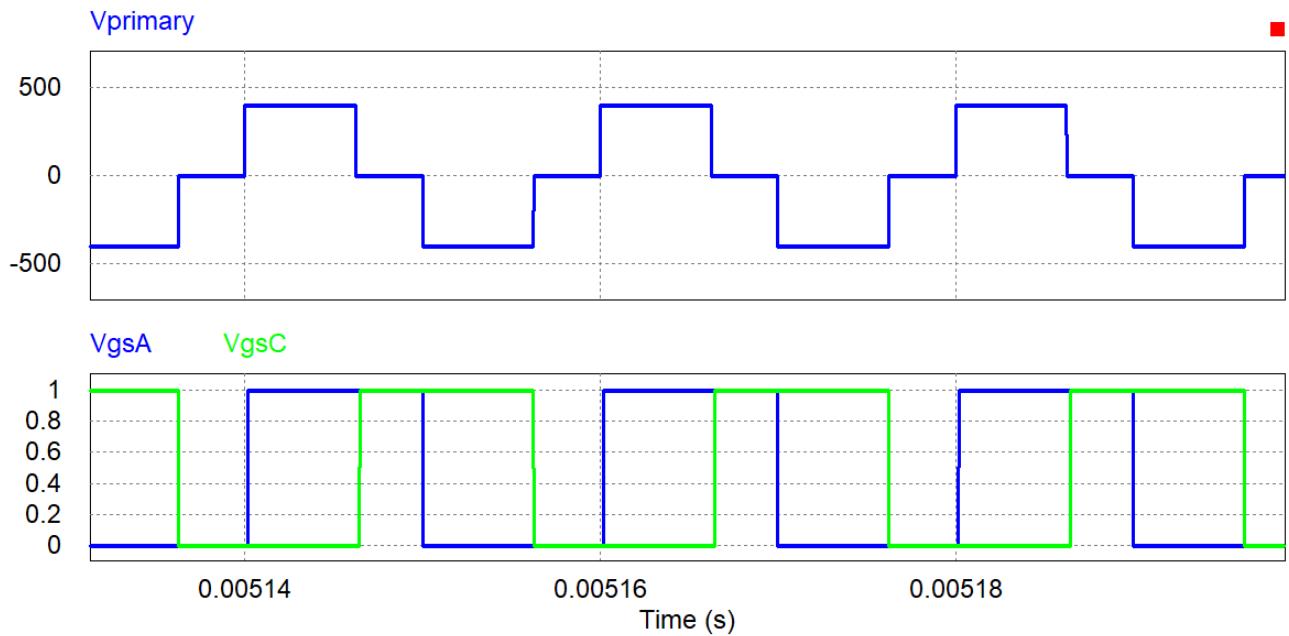


Figure 5.3: Primary voltage of the PSFB transformer

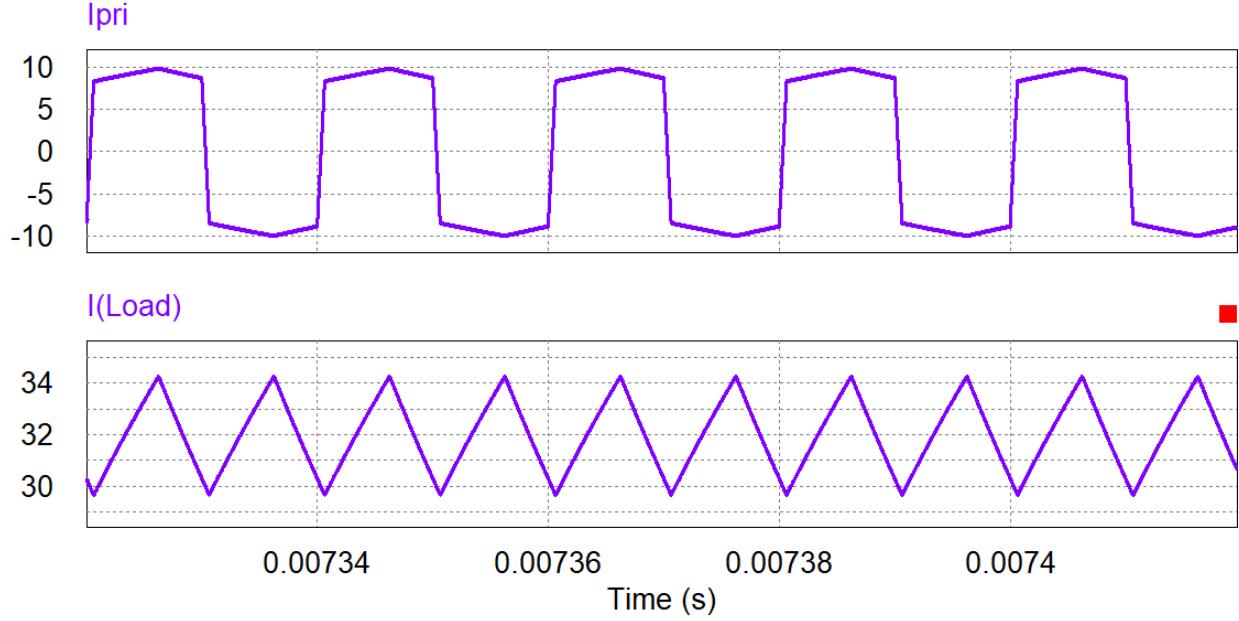


Figure 5.4: Primary and output currents

5.3 Preliminary Calculations

The transformer turns ratio was decided at 4:1:1 but the one that was manufactured was close to 7:2:2, so we shall proceed with that as the turns ratio n ($n = \frac{2}{7}$) The other aspects of the transformer were decided in the same way as in section 3.4.3

Capacitor sizing for DC link (1.5kW):

$$C = \frac{P_0}{2\pi f_{line} \Delta V V_{dc}} = 596\mu F \quad (5.1)$$

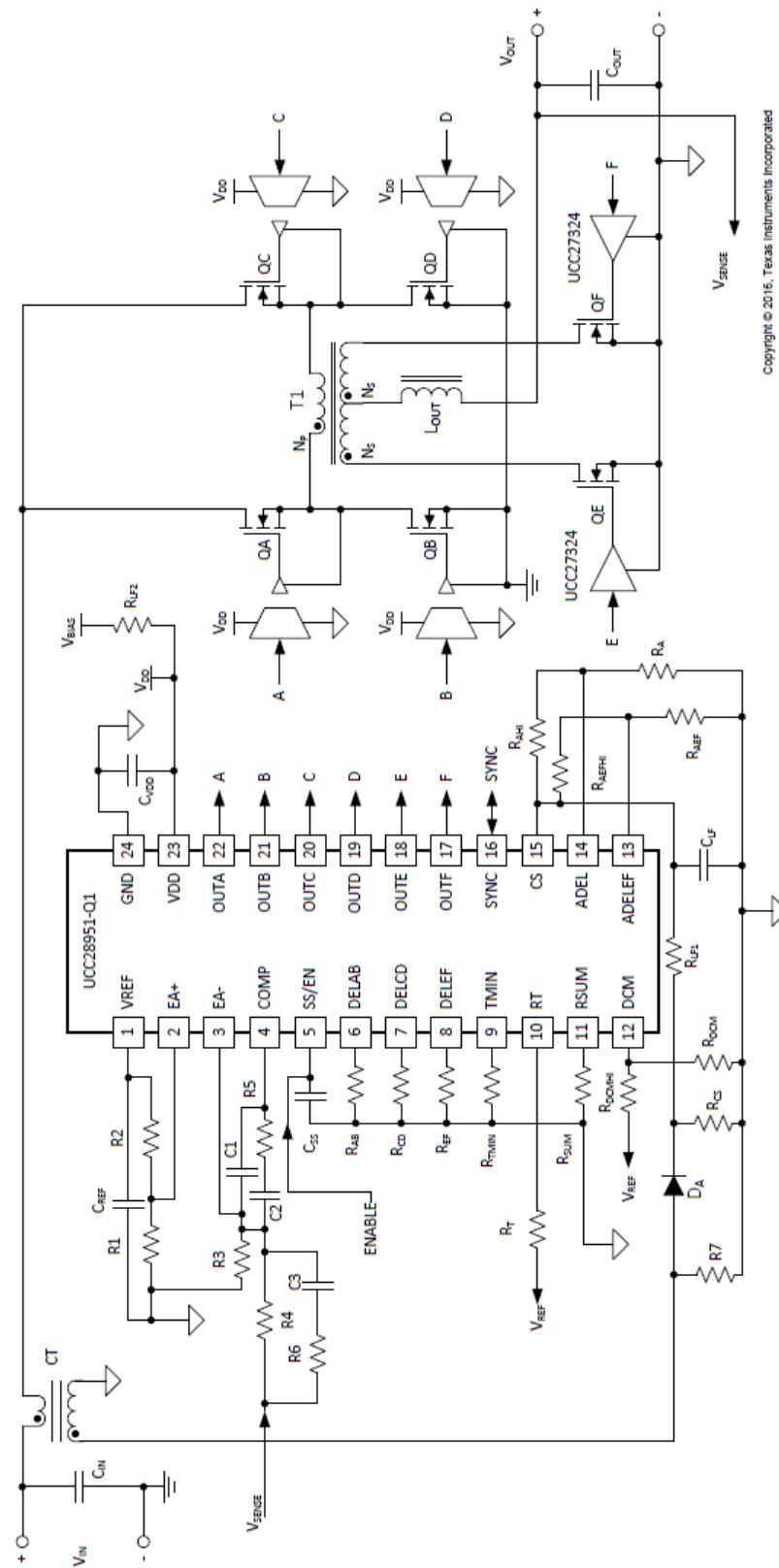
Output inductor sizing of PSFB (n is the transformer turns ratio and ΔI_L is 4A):

$$L = \frac{D}{2} \frac{nV_{dc} - V_{battery}}{\Delta I_L f_{sw}} = 43\mu H \quad (5.2)$$

The output of the PSFB is connected to the battery and hence having an output capacitor does not make sense.

5.4 Control using UCC28951 IC

The IC was selected because it has several useful features as mentioned below. [9] refers to the datasheet of the IC. The image also shows the working scheme of the IC.



Copyright © 2016, Texas Instruments Incorporated

Figure 5.5: UCC28951 basic working scheme

- Enhanced Zero-Voltage Switching (ZVS) Range
- Direct Synchronous Rectifier (SR) Control
- Light-Load Efficiency Management
- Average/Peak-Current Mode Control With Programmable Slope Compensation
- Closed-Loop Soft-Start and Enable Function
- CC/CV modes can be incorporated as is explained in the next section

5.5 Integration of CC - CV modes of charging

The way in which charging is done for a lithium ion cell is shown below: [7]

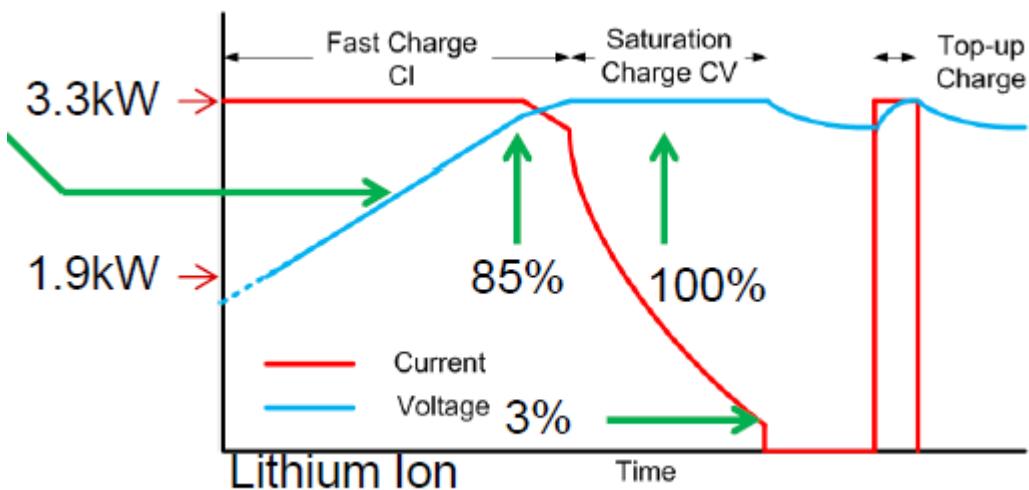


Figure 5.6: Charging of a Lithium ion type battery

From section 7.3.3 of [9], we have the following. The error amplifier in the IC has two uncommitted inputs, EA+ and EA-, with a 3-MHz unity gain bandwidth, which allows flexibility in closing the feedback loop. The EA+ is a noninverting input, the EA- is an inverting input and the COMP is the output of the error amplifier.

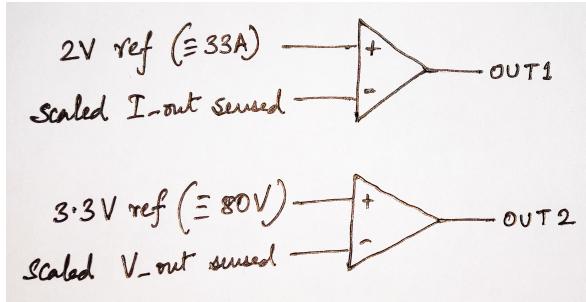
The input voltage common-mode range, where the parameters of the error amplifier are ensured, is from 0.5 V to 3.6 V. The output of the error amplifier is connected internally to the noninverting input of the PWM comparator.

The soft-start signal serves as an additional noninverting input of the error amplifier. The lower of the two noninverting inputs of the error amplifier is the dominant input and sets the duty

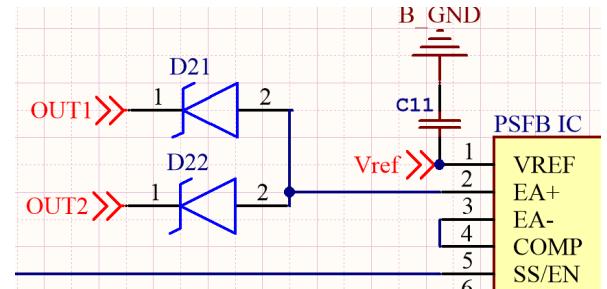
cycle where the output signal of the error amplifier is compared with the internal ramp at the inputs of the PWM comparator.

Thus it is clear that by choosing the right kind of signal at the EA+ input, we can control the mode of charging. From [7] we come to know the method to do so.

There have to be two feedback paths, one each for measuring output current and voltage. Each of them compares to reference and outputs error signals (power demand). After that diodes are implemented such that the **lowest error wins and controls the final output**. This method ensures automatic CV/CI transition. The following images illustrates this aspect as implemented in the schematic.



(a) Comparator logic



(b) Input to UCC28951

Figure 5.7: Logic for implementation of CC CV modes [7]

5.6 A word on the PSFB Transformer

Shown below is a picture of the transformer to be used (being tested to verify turns ratio). As can be seen, it is bulky and hence the PCB designing becomes difficult. Hence planar transformers, although costly are best suited for the purpose.



Figure 5.8: 3kW PSFB Transformer

5.7 Final Schematics and Fabrication

The Altium schematic below takes into consideration the CC/CV modes of charging.

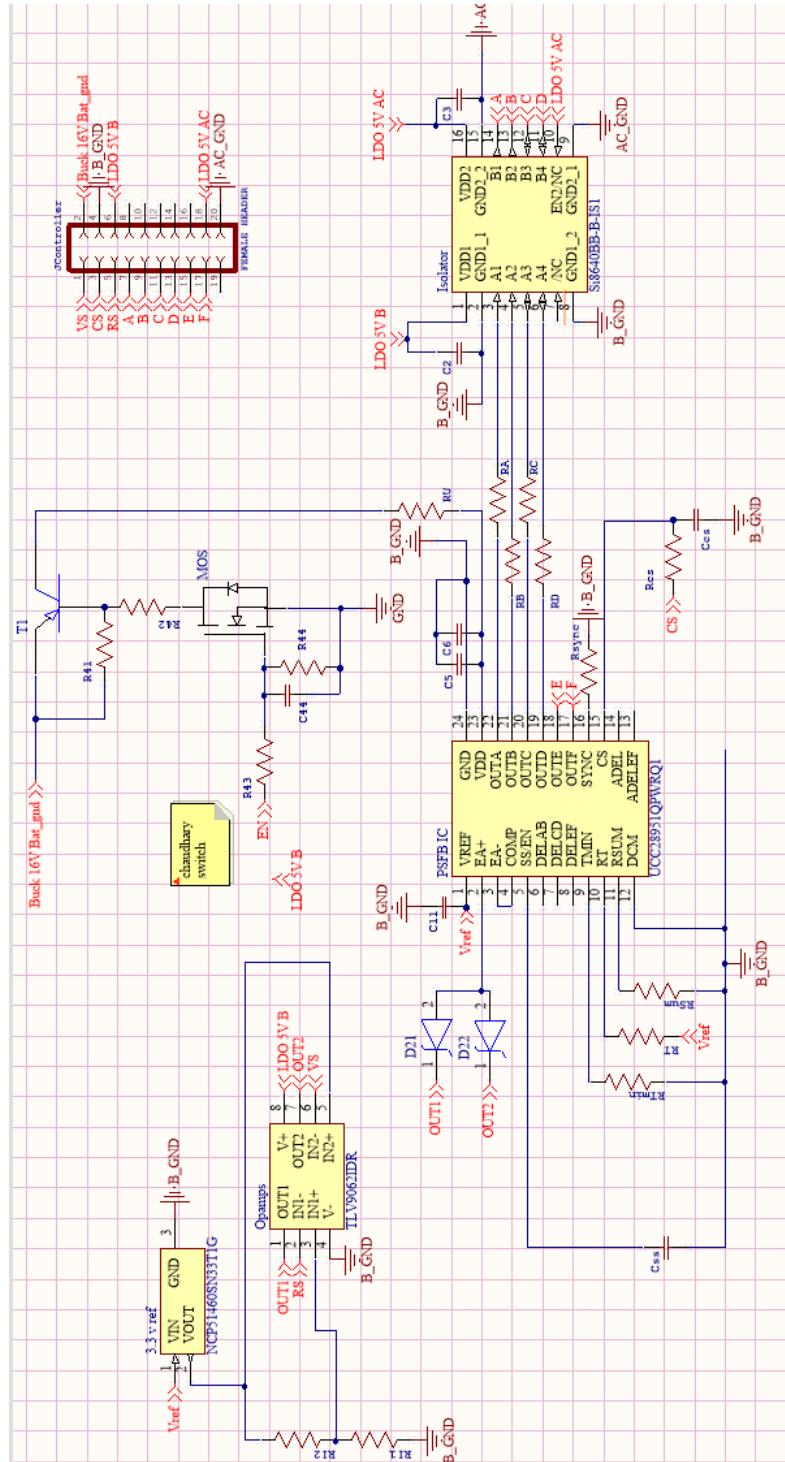


Figure 5.9: Altium Schematic for PSFB controller

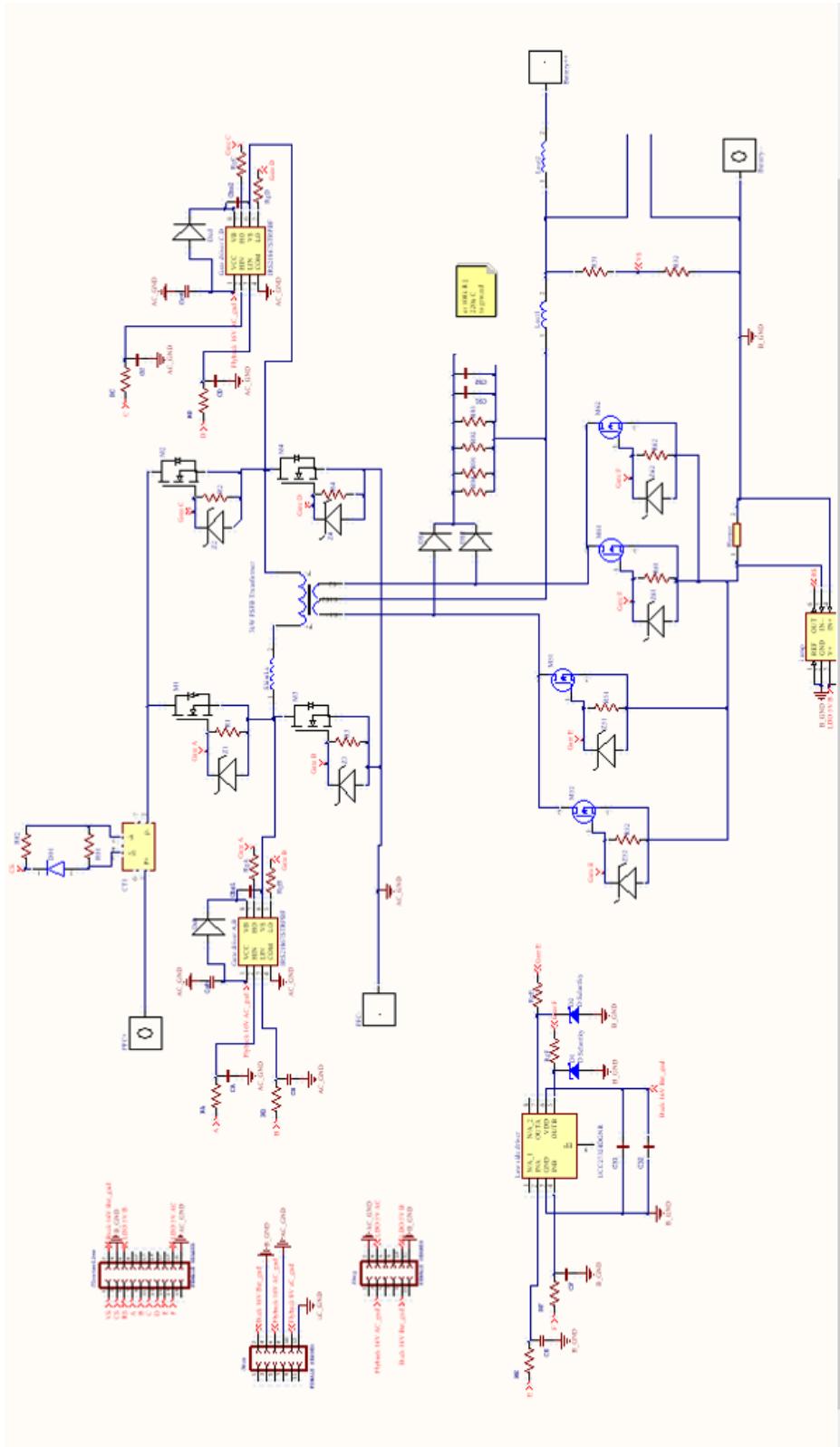


Figure 5.10: Altium Schematic for PSFB

Conclusion and Future Work

6.1 Work completed till now

- Flyback Converter design, fabrication and testing
- Buck converter design, fabrication and testing (the new design has been sent for fabrication)
- Manual enable features were included for the auxiliary power supply (one cause of problems)
- Simulations of PFC rectifier in closed loop
- Fabrication and testing of PFC hardware
- Simulation of PSFB converter with current control
- Although it was not possible to fabricate and test the hardware owing to the unprecedented lockdown, the schematics were prepared.

6.2 Future Scope

- The PSFB converter needs to be tested along with the PFC
- Component sizing can be done more efficiently to reduce the overall size and weight
- Heat sink design and fabrication can also be looked into
- A central software can also be looked into that would manage BMS and Charger simultaneously and would improve according to the utilization of the user

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