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Bias Techniques for GaN and pHEMT Depletion Mode Devices

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Introduction

Advances in process technology have led to GaN depletion mode devices finding their way out of research labs and into communications markets. In many microwave wave applications for example, the LDMOS devices that have dominated power amplifier designs are giving way to GaN solutions, particularly the final output stage where efficiency and linearity are key requirements. The high power density, high efficiency capability of GaN makes it valuable for microwave applications, and the trend of GaN devices finding their way into future communication systems is predicted to continue. As a result, there are incentives to develop novel bias techniques that provide proper bias control and temperature compensation for depletion mode devices. These techniques must be compatible with communication applications where stable operation into high capacitance loads is necessary for the wide video bandwidths found in Doherty configured amplifiers that carry 4G and LTE signals. As pHEMT devices are well established in numerous applications, the approach is to develop universal techniques that work for any type of depletion mode device.

Concepts, practical circuit recommendations, measurement data and discussion are presented in the following sections:

1.0 Depletion Mode Bias Design Requirements

Microwave power amplifier (PA) device performance is typically evaluated for a given drain quiescent current. Related to the conduction angle, the gate voltage of the device is adjusted until the desired quiescent drain current is achieved. The majority of applications require a bias point somewhere between linear Class A operation, where full 360 degree conduction occurs, and the most efficient Class C operation where only 180 degrees of the signal is conducted. Most common in the PA world is Class AB biasing, where the trade-off between linearity and efficiency falls within a usable range. Class AB biasing could be classified as "light Class AB" say for example in the carrier amplifier of a Doherty circuit. On the other end, "deep Class AB" is employed for the peaking amplifier in a Doherty configuration or the final PA stage of a transmitter. Here the efficiency is paramount to linearity, so biasing the device at a low quiescent current as possible is advantageous. Class C biasing is employed in a wide variety of constant envelope modulation applications that use a single device.

The first step towards adaptive device bias is that the gate voltage must be adjustable to the desired class of operation. Given the popularity of modern embedded controllers in microwave systems, the control method of choice is the ubiquitous DAC. The DAC value for the desired quiescent current can be determined using automated routines on a unit to unit basis at final test. This is a necessary alignment step for power amplifiers. Alternatives to DACs include mechanical potentiometers, EEPOTs, and switched resistor networks.

Beyond the fundamental step of selecting and setting the bias point, there are other factors to consider. While the gate of a depletion mode device draws negligible current at low power levels, the Schottky diode in the gate structure will start to rectify as the input power increases, sending significant current into the gate. Additional MMIC circuitry on the gate, such as level shifters or bias resistors, can require either positive or negative gate current flows. Often bypass capacitors are placed at the gate in order to improve video bandwidth, and these capacitors can be quite large, up to hundreds of microfarads. Op-amps, a common bias control device, have a tendency to oscillate into capacitive loads, requiring gate bias circuits that are stable under capacitive loading. Temperature compensation is often needed for critical linear applications, and it is advantageous if the temperature slope adjustment is independent of the bias voltage setting. A summary of the requirements for biasing depletion mode devices is provided below. The bias circuits described in this paper address these requirements.

- Applicable to any depletion mode technology: GaN, pHEMT, MESFET, etc.
- DAC adjustable and ON/OFF controllable
- Bilateral current source capable of supplying positive or negative current flow
- Low IR drop from driver to gate
- Stable driving large capacitive loads
- Stable driving impedances from open circuits to heavy current loads
- Tolerates supply voltage variations
- Independent temperature slope and bias voltage adjustments
- One wire temp sensor suitable for SMT or hybrid assemblies
- Low cost commodity components available from multiple vendors

2.0 Temperature Characteristics of TriQuint GaN Devices

What happens when a fixed voltage is placed at the gate of a depletion mode GaN or pHEMT device and the quiescent drain current measured over a wide temperature range? Figure 1 illustrates the expected result, arbitrarily normalized to 1A range. As carrier concentrations, mobility and Schottky barrier voltages change over temperature, so does the drain current. The absolute value of the current does vary from unit to unit based on pinch-off voltage variations across the wafer, as illustrated by three units 1 – 3 in Fig. 2(a). On the other hand the temperature slope is a derivative that has much less variation. In addition to a strong linear dependence, there are small percentages of second and third order terms. This semiconductor physics is remarkably consistent for a given process.

For saturated operation the above changes in quiescent current have little effect on overall output power or efficiency performance. Data presented in Section 4 will verify that a fixed gate voltage is sufficient for saturated power applications.

In the world of modern digital communications linearity and efficiency are the key parameters. Devices in receiver chains and in transmitter blocks outside of DPD loops are required to be highly linear. Final stage Doherty amplifiers, drivers and pre-drivers inside the DPD loop are required to be highly efficient and capable of being linearized with realizable polynomial functions. Maintaining a fixed quiescent bias point over temperature is one of the essential techniques to realizing high performance transmitter chains capable of meeting specifications over a wide range of operating conditions. By adjusting the gate voltage over temperature, the quiescent current can be held constant. Figure 2 presents data from the lab, the actual gate voltages required to hold the quiescent current constant for several different TriQuint GaN devices at various different current densities. Similar to the fixed voltage plot, the gate voltage required to maintain constant current over temperature shows a strong linear dependence with small second and third order contributions.

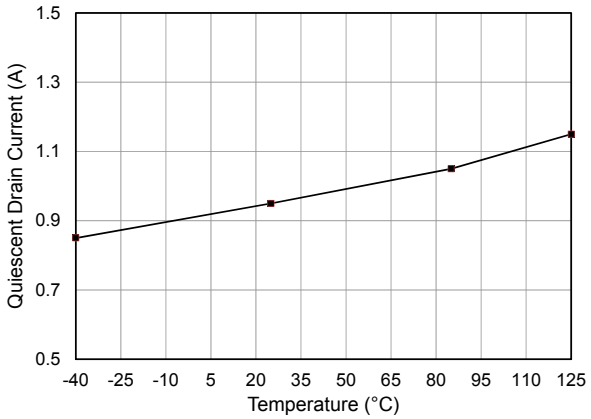


Fig. 1. Illustration of depletion mode device quiescent drain current dependence over temperature for fixed gate bias voltage.

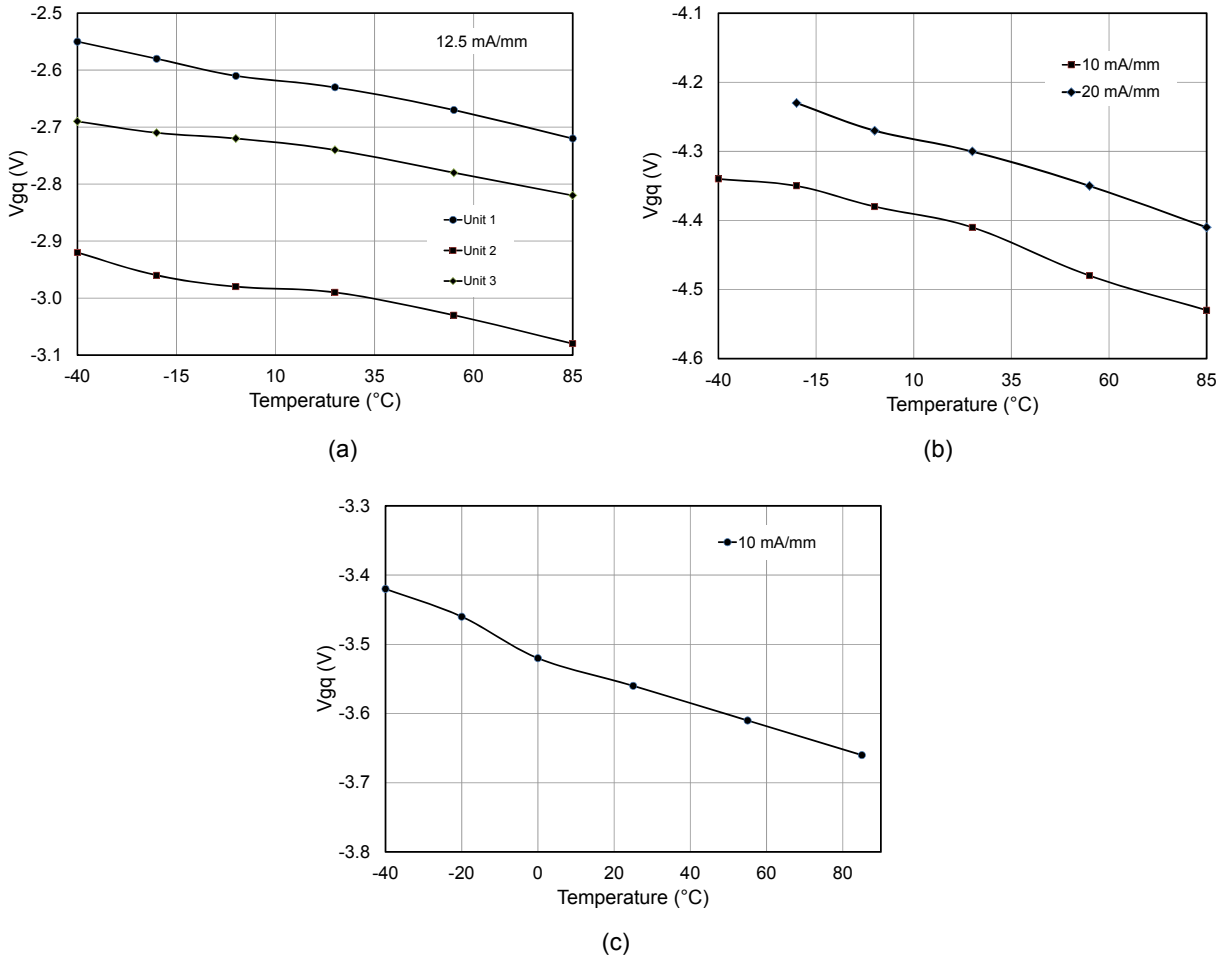


Fig. 2. Gate voltage over temperature for GaN devices at constant current density. (a) 120W 32V T1G4012032-FS, three devices at 12.5 mA/mm, (b) 30W 28V T1G6003028-FL, one device at 10 mA/mm and one device at 20 mA/mm, and (c) the 55W 28V T1G4005528-FS, one device at 10 mA/mm.

3.0 Temperature Compensation Methodology

3.1 Temp Comp Made Easy

The simplest and most expedient way to temperature compensate a depletion mode device is to ignore the entire subject. Simply apply Vgate, a fixed voltage to the gate and then accept any subsequent performance variations over temperature. This bare-bone technique is effective in a number of applications. The further a device is biased into Class AB and Class C operation, the more likely that performance using fixed gate voltage bias will be satisfactory. Saturated modulation schemes and applications with relaxed temperature requirements are all ideal candidates for fixed gate voltage bias schemes. There is a lot to be said for the simplicity shown in Fig. 3.

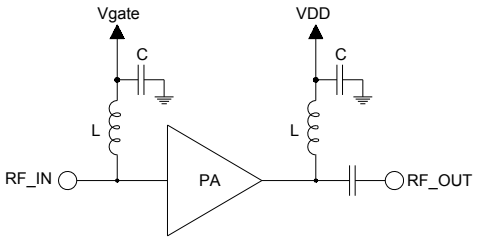


Fig. 3. Standard bias network with fixed voltage Vgate applied to device gate.

3.2 Temperature Compensation Techniques

Advancement of modern digital communications systems often pushes the technology envelope. In these systems the temperature performance of power devices is an important factor. Cellular base stations, microwave point-to-point radios and many ISM applications employ bias techniques that minimize linearity degradations as the ambient temperature varies over the course of the day and seasons.

There are two primary approaches to compensating the bias point of power amplifiers as the temperature changes:

- Closed Loop
- Open Loop

Closed loop techniques monitor the quantity in question, for example device drain current, and feed that information back to a controller. When the loop is closed by the controller, the quantity in question is maintained at the set-point value, within the accuracy of the monitor.

Open loop techniques apply the set point directly to the device and change that set point based on a temperature sensor without regard to the actual drain current. The consistencies of semiconductor devices make open loop control possible, as the temperature characteristic does not vary appreciably from unit to unit. Both closed and open loop temperature compensation can be further divided into analog or digital techniques. Figure 4 and Fig. 5 provide a summary of bias compensation techniques in block diagram form.

Each approach has its own unique set of advantages and issues. Open loop techniques have lower material cost than closed loop but require alignment at final test, and can be less accurate over temperature. Alignment can be a manual process or automated with digitally controlled devices, such as an EEPOT, adjusted by the test stand until the desired operating point is achieved. Open loop controllers cannot compensate for long term drift of devices, a phenomenon that has been observed in early generations of semiconductor processes. To account for long term drift with an open loop driver, designers can either ignore the drift or take advantage of the fact that the majority of long term drift occurs within the first hours of operation. Devices are burned-in before final alignment, a process suitable for limited volume production. Digital closed loop techniques (Fig. 4) do not require manual alignment or burn-in and can compensate for long term drift. However material costs are higher, the loops require development of PID controller algorithms and the sensors need to be stable over temperature. Complications arise with closed loop techniques when the amplifier must operate continuously, such as in cellular base stations. Information from RF power output monitoring could be added into the equations for the device drain current settings, or the RF removed during periodic maintenance cycles. This additional complexity is addressable only in the digital domain. Large analog suppliers integrate digital monitor and control functions into products designed specifically for closed loop control of multiple PA stages [1].

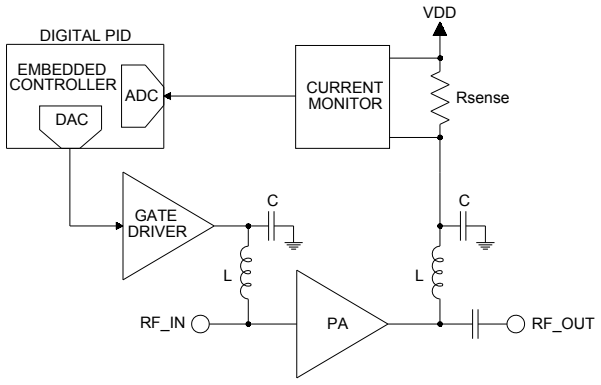


Fig. 4. Closed loop bias compensation. Bias stability over temperature is determined by the current monitor function. The embedded controller uses a Digital PID controller loop to adjust the gate voltage to the required drain current when RF is periodically turned off.

Analog closed loop techniques constantly respond to changes in drain current, making them useful only for small signal Class A constant current designs. There are several well-known analog Class A closed loop bias circuits that use a single op amp, or even just a matched transistor pair [2, 3]. Block diagrams for open loop techniques are provided in Fig. 5. The three techniques are similar in that no monitoring of the drain current is performed. Shown in Fig. 5(a), a mechanical potentiometer is used to set the gate voltage, while a DAC replaces the potentiometer in Fig. 5(b). The temperature coefficient of the voltage output is set by the resistor value from the temperature sensor feeding into the summing function. This design feature is a key contribution to the discussion of Class AB device temperature compensation. In the past tight coupling between the temperature sensor and RF device was required to track gate voltage. For the open loop designs presented here, the temperature sensor coefficient can be arbitrary because it is scaled when entering the summing function. Therefore the temp sensor does not need to be close to the RF device and its output does not have to match the RF device. Figure 5(c) differs in that the embedded controller reads the temp sensor, and then using a look-up table or interpolation trims the gate voltage to the needed value. Since the look-up table scales the temperature sensor coefficient, the response of the sensor can be arbitrary relative to the RF device, allowing for a wide flexibility in the selection of the temperature sensor.

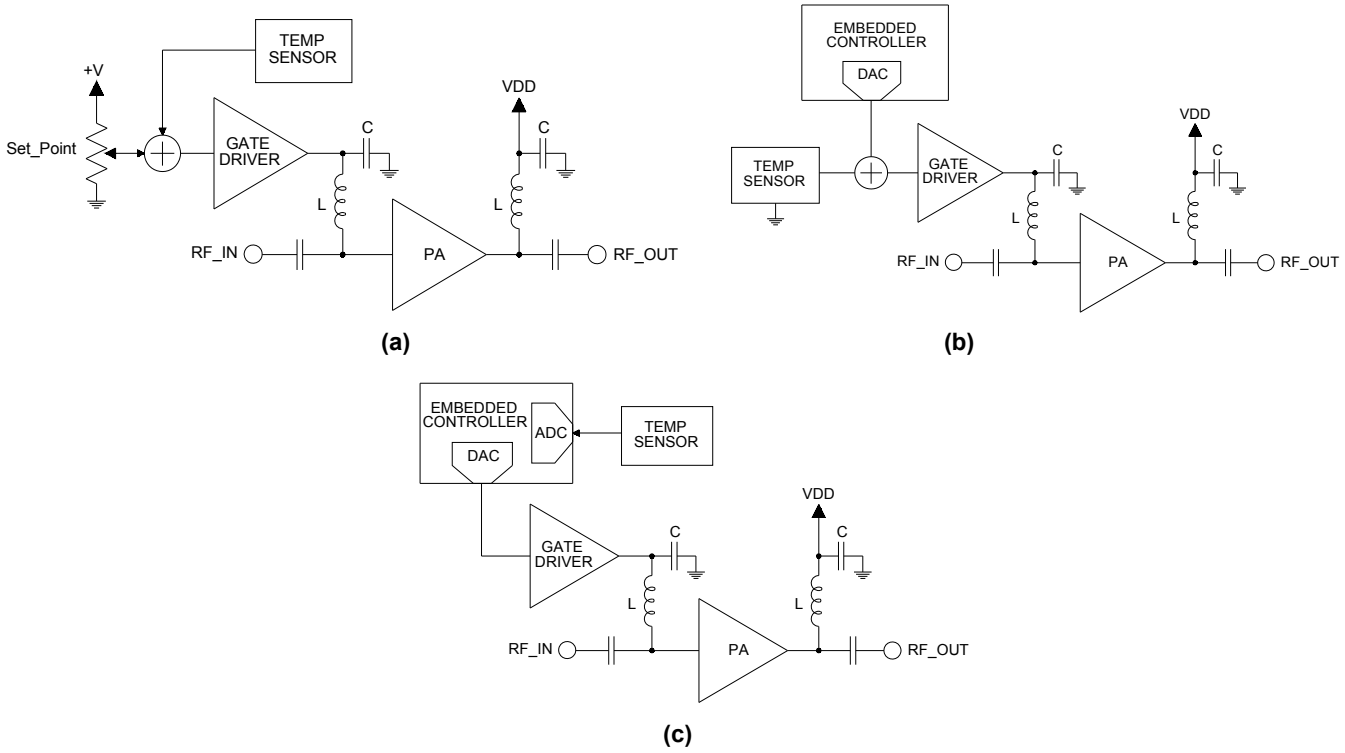


Fig. 5. Open Loop Bias Control Techniques. Gate driver controlled by (a) mechanical set-point and temperature sensor, (b) DAC set-point and temperature sensor and (c) all digital control.

4.0 Stability Considerations

Operational amplifier circuits are prone to oscillations when driving large load capacitances. When a capacitor is added to the output, a pole appears in the response as shown in Fig. 6. While the gain starts to drop at 40 dB/octave instead of 20 dB/octave, the potential for instability arises when the phase exceeds 180 degrees before the gain is less than 0 dB [4, 5], a sufficient condition for oscillation.

There are a number of ways to avoid the oscillation condition. These design "tricks" are summarized in Fig. 7. Each has its own advantages. In Fig. 7(a) a series resistor isolates the capacitive load from the op amp feedback loop. Simple and guaranteed to always work, the series resistance will need to be large enough to avoid oscillations. However if there is appreciable gate current flow, the series resistance is an impediment to getting the maximum performance out of the RF device. Current flow into the gate, typical of pHEMT devices as they approach compression, will pull the gate voltage more negative, shutting the device off. For designs that have negligible gate current flow the series resistor is a preferred approach.

Voltage regulators are designed to drive essentially unlimited large capacitances as shown in Fig.7(b). This can be useful for modern

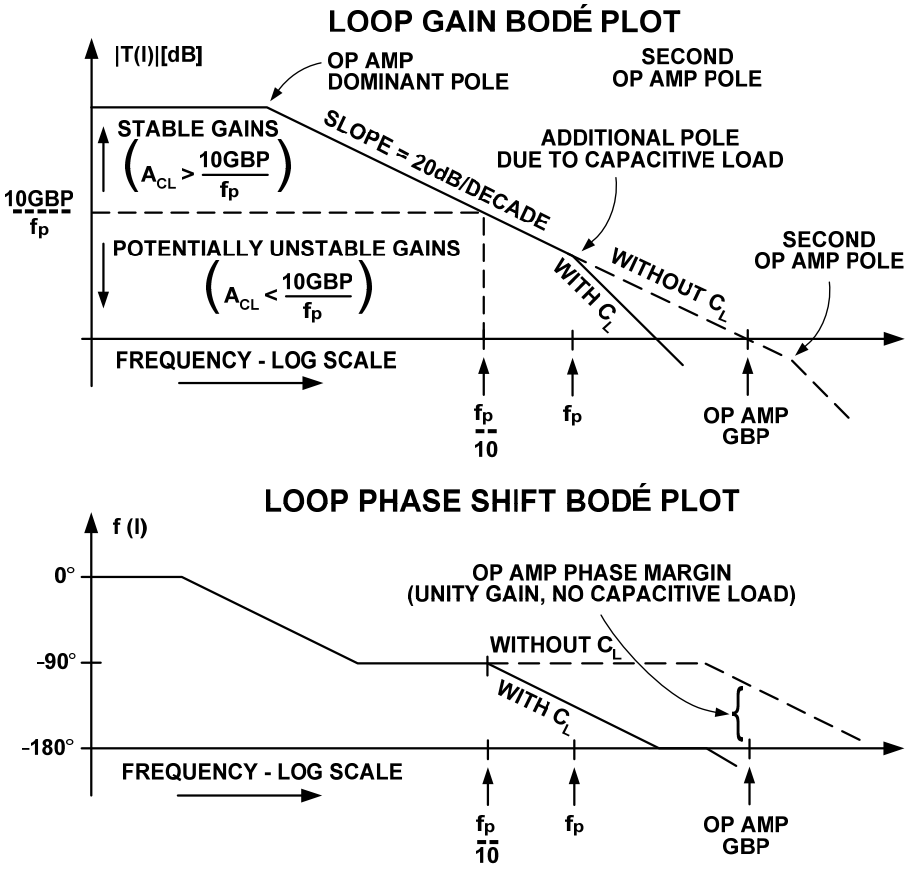


Fig. 6. Bode plot for op amp with and without capacitive loading C_L [6]. The capacitor loading adds a pole to the response. The pole quickly sends the phase to more than 180 degrees while the gain is still greater than 1, a sufficient condition for oscillation.

Doherty Amplifiers in multi-carrier environments, where video bandwidths greater than 100 MHz require significant bypassing. Commonly found in these communication amplifiers are large capacitors placed in shunt as close to the gate as possible. The disadvantage to the voltage regulator approach is additional component count and associated cost. In addition, a power consuming shunt resistor is required to maintain minimum current through the regulator and sink any negative current flow from the gate. Despite the limited negative current handling capability, many familiar with using bench power supplies and shunt resistors will find appealing similarity to this approach.

Gain may be added as shown in Fig. 7(c). Capacitive loading capability increases proportionally to the gain [6]. As the gain increases over 5X the loop dynamics are such that the added capacitive pole falls outside the loop bandwidth. Often the use of large gains is not ideal, as the dynamic range of the DAC is compressed by the gain in the driver.

Another approach employed in this work is lead-lag compensation shown in Fig. 7(d), a dual loop topology. A second loop added to the feedback path places a zero in proximity to the pole thus canceling them out [6, 7]. The references give the impression that this cancellation approach is difficult to implement. While true for high speed op amps and stringent overshoot specifications, the application here is at DC where distortion of high frequency signals is not a consideration. With the right component value selection, including the low GBW op amps employed here, a wider range of load capacitances can be tolerated with dual feedback. The design can handle gate current flow without appreciable voltage error as the series resistor is within the feedback loop. The dual loop feedback configuration has its advantages, however there is still the potential for instability under excessive capacitive loading conditions. Common practice is to employ various combinations of isolation, gain and dual feedback for universal gate driver designs.

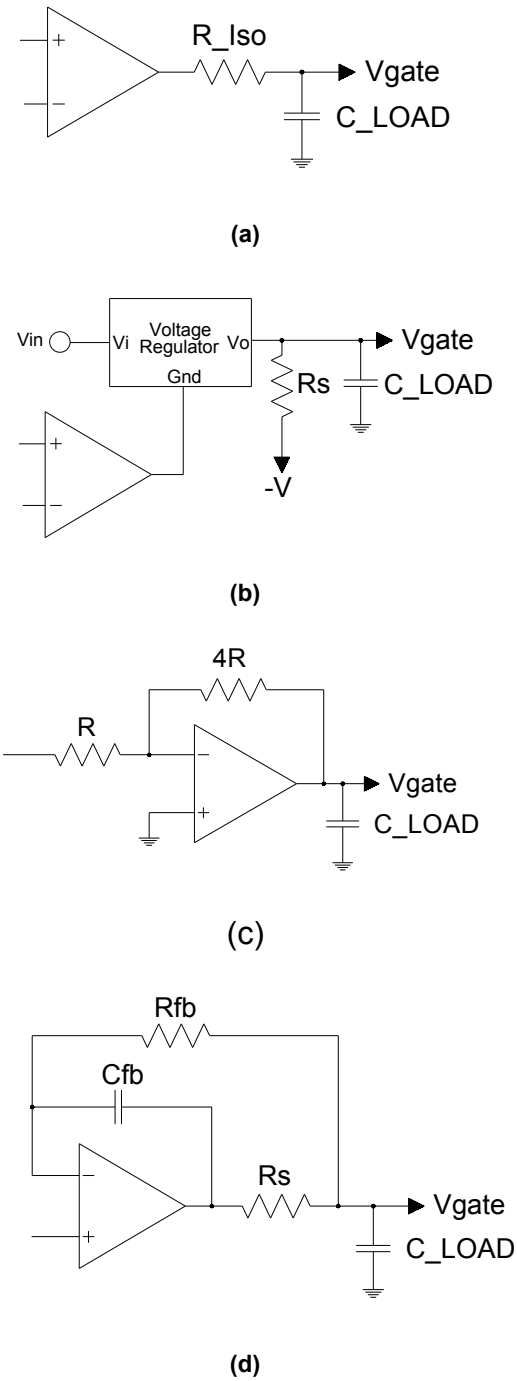


Fig. 7. Stability techniques for driving capacitive loads. (a) Isolation Resistor, (b) voltage regulator, (c) gain, and (d) dual feedback loop.

5.0 Low-Cost Analog Temperature Compensation Techniques

Conventional PN junctions are often employed as temperature sensors. Empirical work has shown that the PN junction of a BJT device is linear over a wide temperature range. In this work a generic PNP device is employed as the PN junction temperature sensor. A low-cost, single wire sensor can be formed with the collector of the PNP transistor connected to ground. Using a PNP transistor allows die attachment to ground in hybrid assemblies and use of packaged parts with surface mount technology. The single wire sensor simplifies layout & RF bypassing compared to thermistors employed in feedback loops [8].

Figure 8 illustrates the principle of operation for the low-cost gate driver with temperature compensation. Buffered by an inverting amplifier that uses half the diode voltage as reference VREF, the output of the complete temperature sensor is 0 V at room temperature, often taken to be +25 °C. In reality power amplifier heat sinks experience a temperature rise in the vicinity of the power device when the ambient temperature is held to +25 °C. So the bias resistor R_Bias to the PN junction is adjusted to achieve 0 V output at whatever temperature equilibrium is achieved at the ambient temperature setting.

The temperature sensor 0 V output at +25 °C ambient temperature provides a convenient input to a ground referenced summing junction. The advantage of the summing junction is that at room temperature the current through R_Slope is zero, allowing the DAC to set the gate voltage independent of the temperature sensor. As the temperature increases, V_TS will also increase, sending current into the summing junction through R_Slope. When temperature decreases, V_TS will decrease below 0 V, pulling current out of the summing junction. By adjusting the value of R_Slope the change in output voltage Vgate over temperature can be set.

Since the temperature response is set by the value of R_Slope, the temperature sensor does not have to be tightly coupled to the RF device. Nor does the temperature coefficient of the sensor need to be known. Whatever the coefficient and thermal coupling may be, it is scaled into the appropriate current at the summing junction by R_Slope.

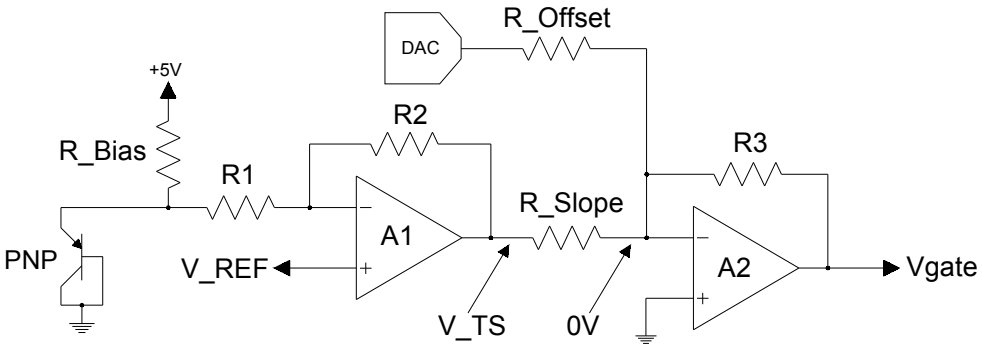


Fig. 8. Low cost temperature PNP sensor and ground referenced summing junction forms temperature compensated gate driver. R1=R2, R3=R_Offset. R_Bias is adjusted to set V_TS=0 at ambient temperature conditions. V_REF is set to ½ the PNP Vbe voltage. The PNP temperature sensor often requires a bypass capacitor to avoid RF interactions.

That allows arbitrary temperature slopes to be achieved with a fixed temperature sensor coefficient, as shown in Fig. 9. In contrast many previous Class AB open loop drivers require tight thermal coupling between a matched temperature sensor and the transistor fingers of the RF device. The use of a summing junction eliminates the need for tight thermal coupling of the temperature sensor and interactions between the offset and slope adjustments. What the approach described here does not eliminate is the need to align quiescent current at final test, a process that is easily automated using DAC or EEPOT control.

The final result is provided in Fig. 10. The voltage from the gate driver is superimposed on the actual gate voltage required to hold a constant quiescent current over temperature. This first order linear correction holds quiescent current constant over temperature, with only the small 2nd order term contributing to error.

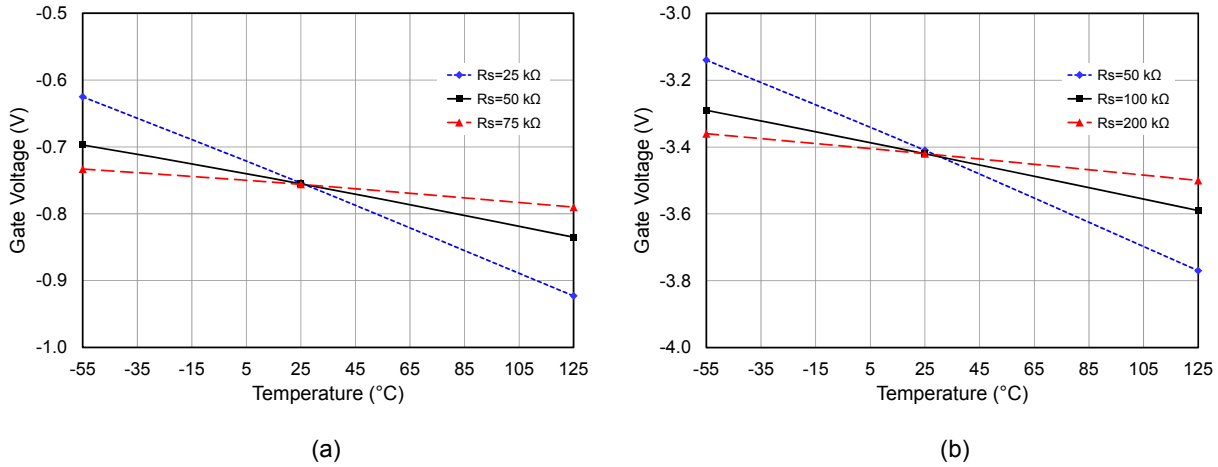


Fig. 9. Output voltage V_Gate over temperature for three values of R_Slope. (a) Voltage output at −0.75 V for pHEMT device, and (b) voltage output at −3.4 V for a GaN HEMT device.

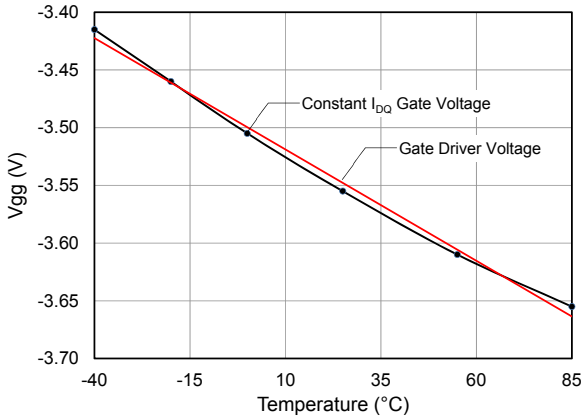


Fig. 10. Gate driver voltage provides 1st Order (linear) approximation to the required gate voltage for constant I_{DQ}. T1G4005528-FS, I_{DQ}=10 mA/mm

6.0 DAC Control

Initialization of digital to analog converters takes time while the processor boots up, loads the image and executes commands. During this startup interval most DACS will provide 0 V output, or tri-state. With zero volts at the DAC the output of A2 in Fig. 8 will also be at 0 V, an undesirable saturated drain current (I_{DSS}) condition for depletion mode devices. Under saturated channel operation inadequate heat sinking in linear applications will result in junction overheating and decreased device reliability. What's needed is a simple circuit technique that provides pinch-off gate voltage rather than zero volts while the DAC is being initialized. The addition of a simple inverting buffer as shown in Fig. 11 accomplishes this initialization state. With the DAC at zero volts during initialization the output of A3 is at the full scale DAC voltage. Inverting through A2, the pinch-off gate voltage is applied to the depletion mode device.

DACs often drive the gate directly in closed loop systems and automated test stands. During the initialization period when the DAC is at zero volts, a non-inverting circuit with offset provides pinch-off voltage levels. Figure 12 shows the non-inverting buffer and output voltage over the DAC range. The resistor divider R1-R2 at the DAC output is not only needed to make the voltage ratios work; for DACs that tri-state during initialization the shunt resistor keeps the DAC output at 0V and thus the gate at pinch-off.

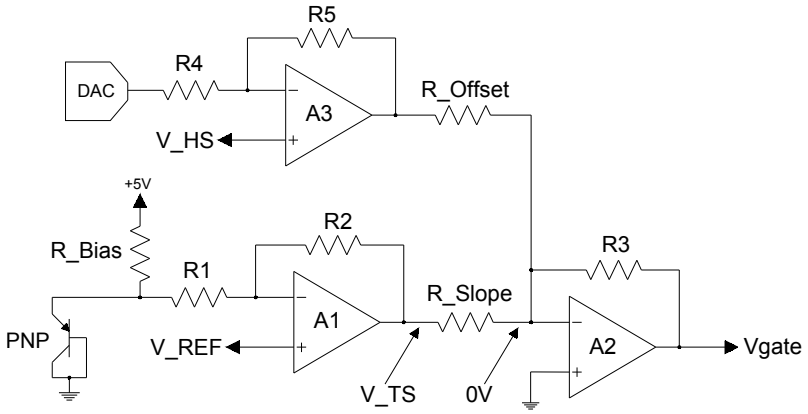


Fig. 11. Inverting the DAC around its half-scale voltage V_HS sets Vgate to −4 V while DAC initialization is completed. R4=R5, R_Offset=R3, V_TS=0 V at ambient temperature conditions.

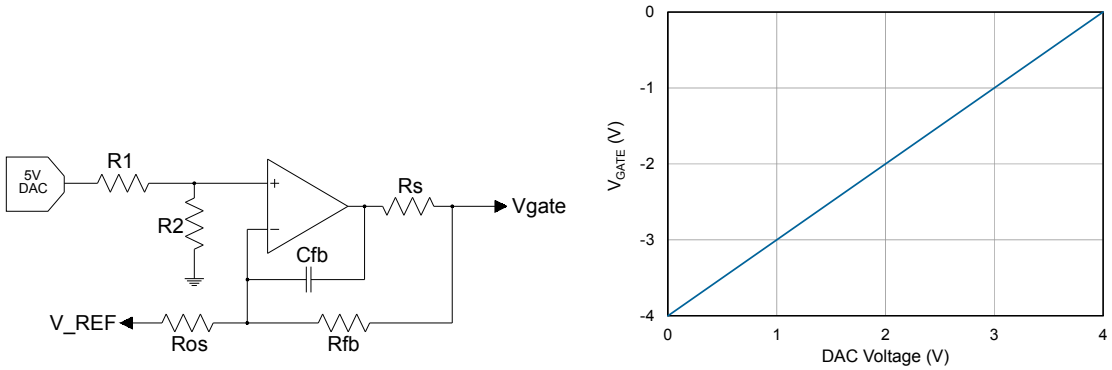


Fig.12. DAC controlled gate driver (left) and gate voltage as a function of DAC voltage for V_REF=+4 V, R1=R2=10 kΩ, Ros=Rfb=2 kΩ, Rs=25 Ω, Cfb=330 pF.

7.0 Practical Reference Designs

The principles outlined here for low-cost universal depletion mode devices bias circuits were followed to develop the two reference designs in Fig. 13 – 14 and the corresponding BOMs provided in Tables 1 – 2. Each design has a safeguard to insure that the gate voltage does not exceed 0V, which can damage the device.

In the bipolar output version in Fig. 13, the collector of Q2A is tied to ground. If U1B rails positive during the power up sequence, then the forward biased base collector junction holds the emitter to approximately 0 V. When just the op amp is used as shown in Fig. 14, a Schottky diode clamp prevents excessive voltages at the gate.

In both designs, R1 will need to be determined such that the output voltage of U1A is identical to the summation reference voltage at ambient temperature conditions and quiescent current. The potentiometer R8 is set to provide the optimal temperature performance. Once the setting is determined, the potentiometer can be left as is or replaced by a fixed value resistor. For applications with demanding temperature performance requirements, an EEPOT may be substituted and automated alignment performed on each unit at final test.

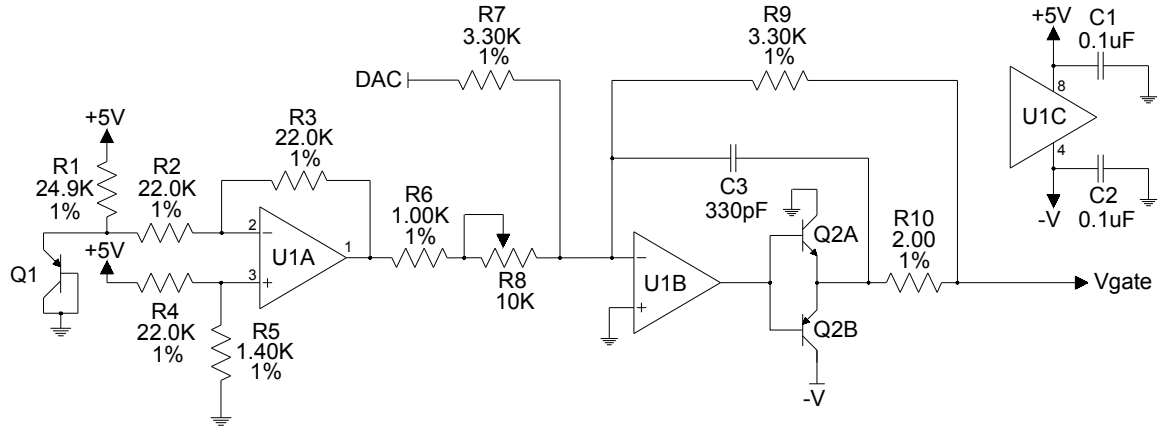


Fig. 13. Universal depletion mode bias circuit using complementary bipolar output stage. Stable driving capacitances in the uF range and capable of providing more than +/- 200 mA bi-polar current drive.

Table 1. BOM, Universal Bias Circuit, Depletion Mode; Bipolar Output Version

Ref. Des.	Value	Description
U1	n/a	LM2904, Op Amp, Dual, General Purpose, MSOP-8
Q1	n/a	MMBT2907A, Transistor, PNP, 60V, SOT-523
Q2	n/a	FMB3946, Transistor, NPN/PNP, 40V, 700mW, SOT23-6
C1, C2	0.1 uF	Capacitor, Ceramic, 16V, 10%, X7R, 0402
C3	330 pF	Capacitor, Ceramic, 50V, 10%, X7R, 0402
R1	24.9 kΩ	Resistor, Thick Film, 1/16W, 1%, 0402
R2, R3, R4	22.0 kΩ	Resistor, Thick Film, 1/16W, 1%, 0402
R5	1.40 kΩ	Resistor, Thick Film, 1/16W, 1%, 0402
R6	1.00 kΩ	Resistor, Thick Film, 1/16W, 1%, 0402
R7, R9	3.30 kΩ	Resistor, Thick Film, 1/16W, 1%, 0402
R8	10 kΩ	Trim Potentiometer, 1/2W, Top Adj, +/-10%
R10	2.00 Ω	Resistor, Thick Film, 1/16W, 1%, 0402

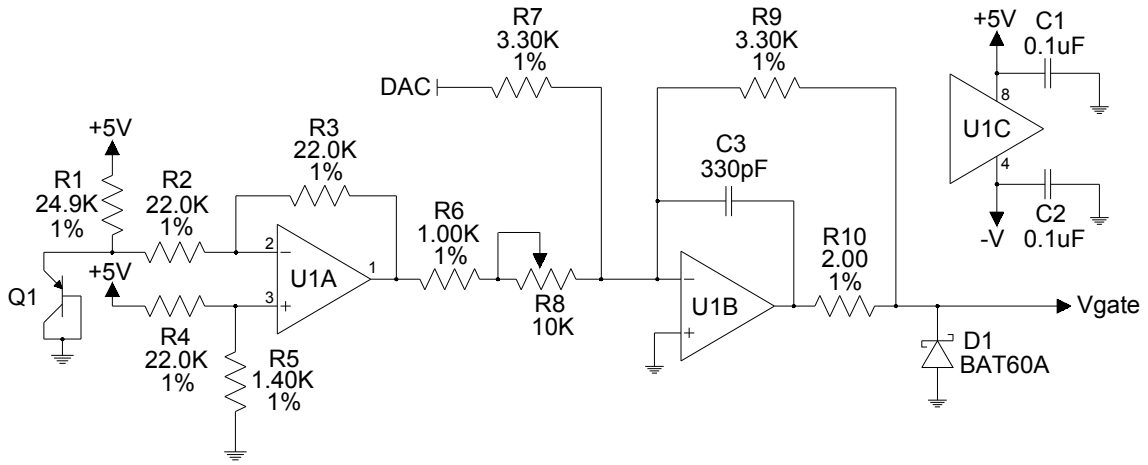


Fig. 14. Universal low-cost depletion mode bias circuit. The dual loop topology around U1B maintains stability when driving capacitive loads in the uF range. This approach is suitable for GaN biasing, and other applications under +/-20 mA gate current flow. For production R8 may be replaced with a chip resistor once the optimal value is determined.

Table 2. BOM, Universal Bias Circuit, Depletion Mode; Op Amp Output Version

Ref. Des.	Value	Description
U1	n/a	LM2904, Op Amp, Dual, General Purpose, MSOP-8
Q1	n/a	MMBT2907A, Transistor, PNP, 60V, SOT-523
D1	n/a	BAT60A, Diode, Schottky, 10V, 3A, SOD-323-2
C1, C2	0.1 uF	Capacitor, Ceramic, 16V, 10%, X7R, 0402
C3	330 pF	Capacitor, Ceramic, 50V, 10%, X7R, 0402
R1	24.9 kΩ	Resistor, Thick Film, 1/16W, 1%, 0402
R2, R3, R4	22.0 kΩ	Resistor, Thick Film, 1/16W, 1%, 0402
R5	1.40 kΩ	Resistor, Thick Film, 1/16W, 1%, 0402
R6	1.00 kΩ	Resistor, Thick Film, 1/16W, 1%, 0402
R7, R9	3.30 kΩ	Resistor, Thick Film, 1/16W, 1%, 0402
R8	10 kΩ	Trim Potentiometer, 1/2W, Top Adj, +/-10%
R10	2.00 Ω	Resistor, Thick Film, 1/16W, 1%, 0402

The circuits were fabricated on a single PCB with a common temperature sensor and a quad op amp. Figure 15(a) shows the block diagram of the bias board and Fig. 15(b) is a photograph of the completed assembly. Table 3 provides a comparison of the two circuits. The capacitive loading provided is a guideline determined by simulating the overshoot and settling times for instantaneous step changes in load current between zero load and the maximum rating.

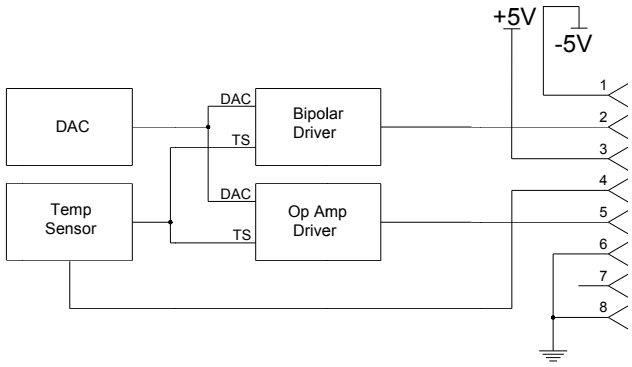


Fig. 15(a). Block diagram of the experimental bias board. To save space the temperature sensor and DAC control is common to both circuits. A jumper selects between a PNP temperature sensor on the PCB or external PNP sensor input at pin 4 of the connector. A potentiometer was substituted for the DAC.

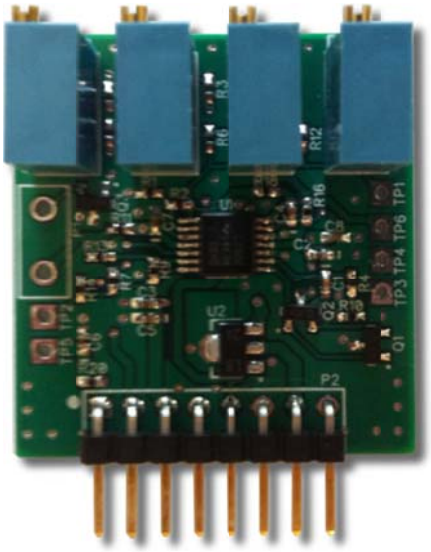


Fig. 15(b). Compact bias board with both versions of low-cost bias circuit. Actual size is 1.25" x 1.325".

Table 3. Bias Circuit Comparison

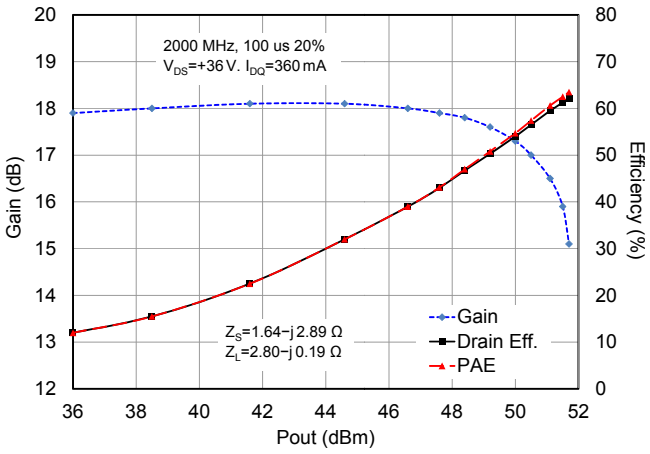
Circuit	Positive Current (mA)	Negative Current (mA)	Max. Voltage (V)	Min. Voltage (V)	Capacitive Loading
Bipolar	200	200	0	−V + 2.3	<10 uF
Op Amp	20	20		−V + 1.5	< 1 uF

8.0 Lab Verification

Verification consisted of demonstrating that the op amp circuit in Fig. 14 did not degrade linear or saturated performance compared to gate bias supplied in the traditional manner from laboratory supplies. Two bias conditions were evaluated over temperature, a fixed gate voltage V_G, and a constant drain quiescent current I_{DQ}. A TriQuint T1G4012036-FS 120 W second generation GaN RF power transistor served as the depletion mode device. At +36 V the 18 dB gain GaN device is capable of generating 24 W of linear power & 120 W of peak power in pulsed operation (Fig. 16).

The evaluation fixture was designed to interface directly with the bias board. The temperature sensor is located just outside the mounting clamp, approximately 1 cm from the GaN device as shown in Fig. 17. A photograph of the completed evaluation platform is shown in Fig. 18.

(a)



(b)

Fig. 16. T1G4012036-FS (a) device package and (b) Gain, Drain Efficiency and Output Power in pulsed operation.

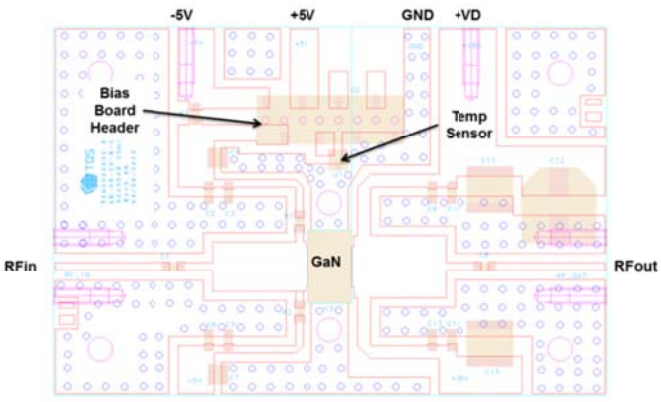


Fig. 17. PCB layout for T1G4012036-FS 120W GaN Device.

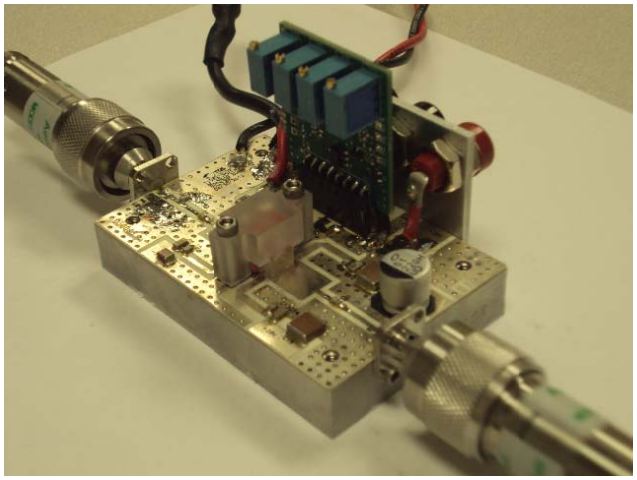


Fig. 18. Assembled high power GaN evaluation board with bias controller card.

Operating at 2140 MHz with a drain voltage of +32 V, both CW and a fully loaded WCDMA signals were employed to collect data. Thermocouples were placed where the device clamp screws into the fixture and on the thermal forcing plate.

Saturated performance with constant V_G and I_{DQ} is provided in Fig. 19 while linear performance under the same conditions is shown in Fig. 20. For saturated CW operation the 3 dB compression point (P_{3dB}) over temperature was consistent between the two bias methods. Not shown is the 51% efficiency of the device that varied less than 0.5% for the two bias conditions. Fixed gate voltages are sufficient for saturated operation; there is little advantage to maintaining constant quiescent current over temperature.

Linear operation places a premium on efficiency and distortion performance. Figure 20 shows the drain current over temperature for the two bias schemes at (a) 40 dBm of WCDMA output power, and (b) quiescent bias. Differences in drain currents are observable between the two bias methods.

Given that drain current at a fixed output power is inversely proportional to efficiency, there is an obvious expectation from this data. Constant V_G bias will result in lower efficiency at hot temperatures and improved efficiency at cold temperatures. Efficiency is expected to relatively constant for the constant I_{DQ} case given that the current is not changing applicably over temperature.

Figure 21 shows that to be the case. For the constant V_G bias, efficiency drops at hot temperatures as the current increases for a fixed 40 dBm output power, while there is improvement at cold temperatures due to the lower drain current. Also plotted is the efficiency using the op amp circuit, showing that it does not appreciably change the efficiency compared to laboratory supplies.

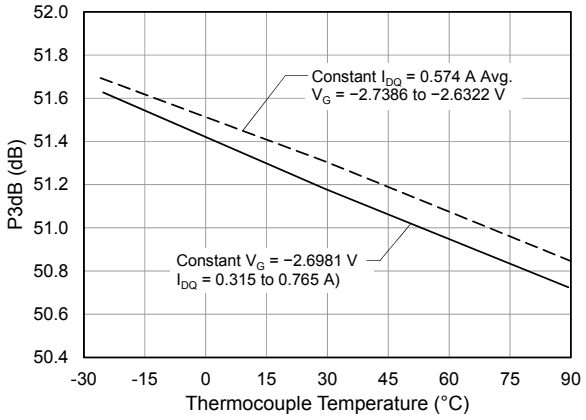
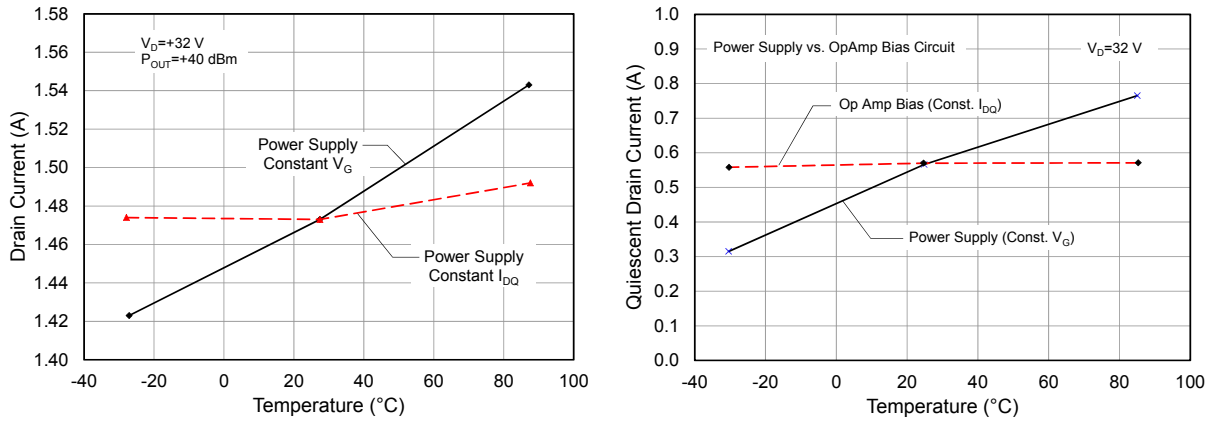


Fig. 19. P3dB vs. Temperature for constant V_G & constant I_{DQ}. The 0.1 dB offset between the two plots attributable to bench-to-bench differences. V_D =+32 V, F=2150 MHz CW drive.



(a) (b)

Fig. 20. T1G4012036-FL drain current over temperature for (a) 40 dBm WCDMA output power and (b) quiescent current state where the op amp circuit was aligned to hold the I_{DQ} constant over temp. V_D=32V, F=2150 MHz.

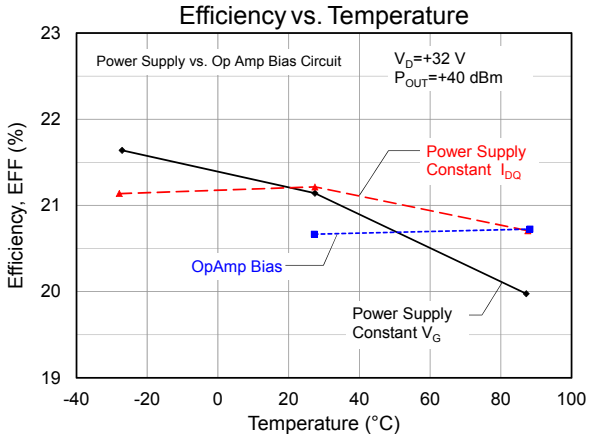


Fig. 21. Drain efficiency over temperature for constant V_G set by a power supply, and constant I_{DQ} set by both power supply and the op amp bias circuit. F=2150 MHz, Pout=40 dBm.

Additional efficiency data that compares laboratory power supply bias to the op amp circuit is given in Fig. 22. Efficiency over the drive-up level test is comparable for the two bias methods. Linearity data is presented in Fig. 23 for 40 dBm of fully loaded WCDMA output power. This data indicates the advantage of maintaining a constant quiescent current over temperature when linearity is a critical specification. There are no significant differences in linearity between a power supply and the op amp circuit supplying the gate voltage to the device. Constant V_G results in degraded distortion performance while constant I_{DQ} maintains linearity over the temperature range. Gain drift over temperature is expected from RF devices regardless of the bias technique. Fig. 24 confirms that constant V_G or constant I_{DQ} bias does not influence gain drift to any great extent. The op amp circuit bias provides the same result as the lab power supply. Regardless of the bias method gain drift occurs due to other factors such as transconductance variation over temperature.

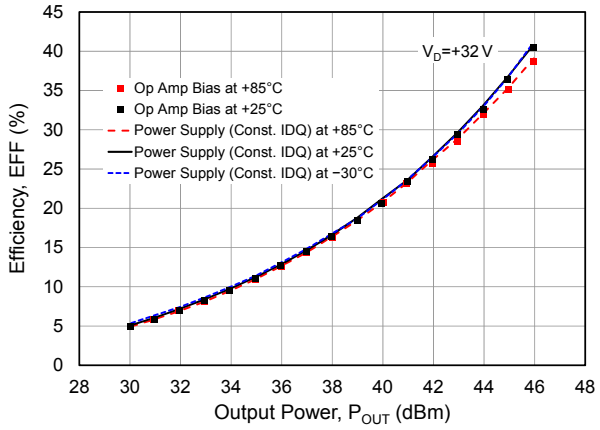


Fig. 22. Efficiency vs. output power for gate bias supplied by the op amp circuit and lab power supply. F=2150 MHz, V_D=+32 V.

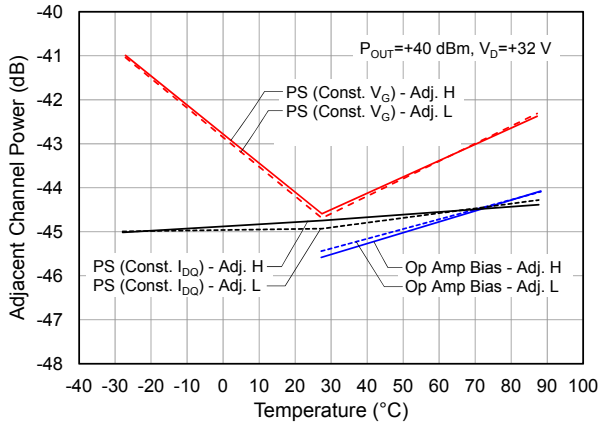


Fig. 23. WCDMA Adjacent Channel Leakage Ratio (ACLR) vs. temperature using power supply and op amp bias.

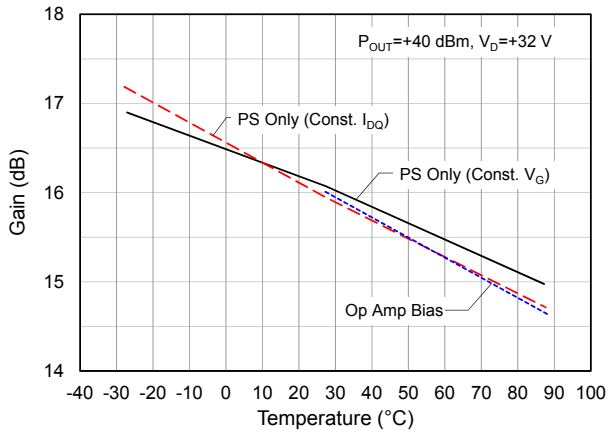


Fig. 24. Gain vs. temperature for constant V_G and constant I_{DQ} bias conditions. F=2150 MHz, V_D=+32 V.

9.0 Conclusions

The requirements and fundamental operating principles behind open-loop bias methods for depletion mode devices have been presented. The outlined approaches are suitable for any depletion mode devices including GaN and pHEMT RF power devices. Summation junctions are employed to provide linear temperature compensation of drain quiescent current. The temperature slope unique to depletion mode devices is easily compensated by the determination of a single resistor value, and the bias level may be set using a DAC. Three different low cost reference designs were presented, each with its own advantages for a given application. Experimental verification has been provided using a 120 W GaN Device under both CW and WCDMA excitation. Validation of the circuit designs was accomplished by comparing op amp gate driver data laboratory power supplies. Conclusions from the data collection are that saturated operation does not require temperature compensation, while distortion and efficiency in linear operation benefit from maintaining a constant I_{DQ} over temperature. The circuits & principles described here form the basis of a complete suite of biasing options for depletion mode RF devices.

10.0 Acknowledgements

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