Sheet: SPLA Board — Power

5V

5V   (SNES)

3.3V   (USB, FPGA, Various)

2.5V   (FPGA)

1.1V   (FPGA)

File: spla-board-power.sch

Sheet: SPLA Board — USB

USB 2.0 High Speed
480 Mbps / 60MBps

File: spla-board-usb.sch

8-bit Sync FIFO
60 MHz

Sheet: SPLA Board — FPGA

File: spla-board-fpga.sch

(wide bus)
21.47727 MHz
3.579545 MHz

Sheet: SPLA Board — Level Shifters

File: spla-board-level-shifters.sch

(wide bus)
21.47727 MHz
3.579545 MHz

Sheet: SPLA Board — PPU

File: spla-board-ppu.sch

24-bit R/G/B bus
21.47727 MHz
3.579545 MHz

Sheet: SPLA Board — Analog

File: spla-board-analog.sch

Analog R/G/B
21.47727 MHz
3.579545 MHz

+3V3
Decoupling Capacitors

C3
4.7uF
C5
0.1uF
GND

+3V3

C4
4.7uF
C6
0.1uF
GND

+1V8 +3V3

C7
3.3uF
GND

U2
50 VREGIN
49 VREGOUT

VPHY
VPLL
VCORE
VCORE
VCORE
VCORE
VCCIO
VCCIO
VCCIO
VCCIO

FT2232H

ADBUS0 16 FIFO_D0
ADBUS1 17 FIFO_D1
ADBUS2 18 FIFO_D2
ADBUS3 19 FIFO_D3
ADBUS4 21 FIFO_D4
ADBUS5 22 FIFO_D5
ADBUS6 23 FIFO_D6
ADBUS7 24 FIFO_D7

ACBUS0 26 FIFO_RXF
ACBUS1 27 FIFO_TXE
ACBUS2 28 FIFO_RD
ACBUS3 29 FIFO_WR
ACBUS4 30
ACBUS5 32 FIFO_CLKOUT
ACBUS6 33 FIFO_OE
ACBUS7 34 FIFO_SIWU

BDBUS0 38 SPI_CLK
BDBUS1 39 SPI_MOSI
BDBUS2 40 SPI_MISO
BDBUS3 41 SPI_CS
BDBUS4 43 DONE
BDBUS5 44 INIT
BDBUS6 45 PROGRAM
BDBUS7 46

BCBUS0 48
BCBUS1 52
BCBUS2 53
BCBUS3 54
BCBUS4 55 JTAG_TCK
BCBUS5 57 JTAG_TDI
BCBUS6 58 JTAG_TDO
BCBUS7 59 JTAG_TMS

PWREN 60 USB_PWREN
SUSPEND 36 USB_SUSPEND

USB_ID
C1
0.1uF
R1
0
(Not sure what this 0-Ohm resistor is for.)
GND

GND

Shield
6 GND
5
4 ID
2 D-
3 D+
1 VBUS

USB_B_Micro
J1

USB self-powered

USB_D- 7 DM
USB_D+ 8 DP

REF 6 REF
R6
12K
GND

RESET 14 RESET
R7
1K
+3V3

+3V3
Weak pullup resistors

R2
10K
R4
10K
R5
10K

U3
1 CS
8 VCC
2 SCLK
3 DI
4 DO
5 GND
93LCxxA
EEDO
R3
2.2K
GND

+3V3

EECS 63 EECS
EECLK 62 EECLK
EEDATA 61 EEDATA

2 OSCI

3 OSCO

13 TEST

AGND
GND

+3V3

C2
0.1uF

X1
1 OE
GND 2
VDD
OUT 3
O252012MEDH4MI
GND

GND

CLK_12MHZ

CMOS digital oscillator, rather than FTDI's crystal suggestion

D1
LED

R12
68

(3.3V - 2.0V) / 20mA = 65 ohm

GND

U1A LFE5U-45F-BG256 — Bank 0

Pin	Net
C4	FPGA_D2
B4	FPGA_COLOR2
E5	FPGA_D6
D5	FPGA_D1
C5	FPGA_D0
B5	FPGA_PRIO1
A5	FPGA_CHR0
E6	FPGA_CHR2
A6	FPGA_PPU2_HVCMODE
D6	LVL_PD_DIR
C6	FPGA_PPU2_HBLANK
B6	FPGA_CHR1
E7	FPGA_PPU2_VBLANK
D7	FPGA_PPU2_TST15
C7	FPGA_PPU2_5MOUT
B7	FPGA_CHR3
A7	FPGA_PPU2_PED
A8	FPGA_5M
A2	FPGA_PPU2_TOUMEI
B3	FPGA_PPU2_RESOUT0
A3	FPGA_COLOR1
A4	FPGA_PRIO0
E4	FPGA_D7
D4	FPGA_D3

Pins: PT11A, PT11B, PT13A, PT13B, PT15A, PT15B, PT18A, PT18B, PT20A, PT20B, PT31A, PT31B, GR_PCLKO_1,PT33A, GR_PCLKO_0,PT33B, PCLKTO_1,PT36A, PCLKCO_1,PT36B, PCLKTO_0,PT38A, PCLKCO_0,PT38B, ULC_GPLL1T_IN,PT4A, ULC_GPLL1C_IN,PT4B, PT6A, PT6B, PT9A, PT9B

VCCIO0 (F6, F7) +3V3

U1B LFE5U-45F-BG256 — Bank 1

VCCIO1 (F10, F11) +3V3

Pins: PCLKT1_1,PT42A, PCLKC1_1,PT42B, PCLKT1_0,PT44A, PCLKC1_0,PT44B, GR_PCLK1_0,PT47A, GR_PCLK1_1,PT47B, PT49A, PT49B, PT51A, PT51B, PT53A, PT53B, PT56A, PT56B, PT58A, PT58B, PT69A, PT69B, PT71A, PT71B, PT74A, PT74B, PT76A, PT76B, PT78A, PT78B, PT80A, PT80B, PT83A, PT83B, URC_GPLL1TIN,PT85A, URC_GPLL1C_IN,PT85B

Nets: FPGA_PPU2_PALMODE, FPGA_PPU2_RESET, FPGA_OVER, FPGA_PPU2_3.58M, FPGA_HCLD, FPGA_XIN, FPGA_PARD, FPGA_PPU1_RESET, FPGA_FIELD, FPGA_VCLD, FPGA_COLOR0, FPGA_PAWR, FPGA_PPU1_HVCMODE, FPGA_VBWR, FPGA_PPU1_PALMODE, FPGA_PPU2_EXTLATCH, FPGA_PPU1_MASTER, FPGA_VRD, FPGA_VAA0, FPGA_VAWR, FPGA_PPU1_EXTSYNC, FPGA_BODGE1, FPGA_VAA2, FPGA_BODGE3, FPGA_VDB7, FPGA_VDB6, FPGA_VAA1, FPGA_VAA3, FPGA_VAA4, FPGA_VAA5

U1C LFE5U-45F-BG256 — Bank 2

VCCIO2 (H11, J11) +3V3

Pins: URC_GPLL0T_IN,PR11A, URC_GPLL0C_IN,PR11B, PR11C, PR11D, PR14A, PR14B, PR14C, PR14D, PR17A, PR17B, PR17C, PR17D, PR20A, PR20B, PR20C, PR20D, PR23A, PR23B, VREF1_2,PR23C, PR23D, PR26A, PR26B, PR26C, PR26D, GR_PCLK2_1,PR29A, GR_PCLK2_0,PR29C, PR29D, PCLKT2_1,PR32A, PCLKC2_1,PR32B, PCLKT2_0,PR32C, PCLKC2_0,PR32D

Nets: FPGA_VAA7, FPGA_VAA6, FPGA_BODGE2, FPGA_VAA10, FPGA_VAA9, FPGA_VAA8, FPGA_VDB4, FPGA_VDB2, FPGA_VAA11, FPGA_VAA12, FPGA_VDB5, FPGA_VDB3, LVL_VA_DIR, FPGA_VAB0, FPGA_VAB1, FPGA_VAB3, FPGA_VDB1, FPGA_VDB0, FPGA_VDB2, FPGA_VAB4, FPGA_VDA5, FPGA_VAB5, FPGA_VAB6, FPGA_VAB7, FPGA_VAB8, FPGA_VAA13

U1D LFE5U-45F-BG256 — Bank 3

VCCIO3 (K11, L11) +3V3

Pins: PCLKT3_1,PR35A, PCLKC3_1,PR35B, PCLKT3_0,PR35C, PCLKC3_0,PR35D, GR_PCLK3_0,PR38A, GC_PCLK3_1,PR38C, PR38D, PR41A, PR41B, PR41C, PR41D, PR44A, VREF1_3,PR44B, PR44D, PR59A, PR59B, PR59C, PR59D, PR62A, PR62B, PR62C, PR62D, PR65A, PR65B, PR65C, PR65D, PR68A, PR68B, LRC_GPLL0T_IN,PR68C, LRC_GPLL0C_IN,PR68D

Nets: FPGA_VAB9, FPGA_VAB10, FPGA_VA14, FPGA_VAB13, FPGA_VDA6, FPGA_VDA4, FIFO_CLKOUT, FPGA_VDA2, FPGA_VAB12, LED4, FPGA_VDA3, FPGA_VDA1, LED6, FPGA_VAB0, FIFO_D0, LVL_VD_DIR, FPGA_VDA0, FIFO_RXF, FIFO_TXE, FIFO_D1, FIFO_D2, FPGA_VAB11, FIFO_D3, FIFO_D4, FIFO_D5, FIFO_D7, FIFO_D6, FIFO_RD, FIFO_OE, FIFO_SIWU, FIFO_WR

U1E LFE5U-45F-BG256 — Bank 6

VCCIO6 (J6, J7) +3V3

Pins: PCLKT6_1,PL35A, PCLKC6_1,PL35B, PCLKT6_0,PL35C, PCLKC6_0,PL35D, GR_PCLK6_0,PL38A, GR_PCLK6_1,PL38C, PL38B, PL38D, PL41A, PL41B, PL41C, PL41D, PL44A, VREF1_6,PL44B, PL44C, PL44D, PL59A, PL59B, PL59C, PL59D, PL62A, PL62B, PL62C, PL62D, PL65A, PL65B, PL65C, PL65D, PL68A, PL68B, LLC_GPLL0T_IN,PL68C, LLC_GPLL0C_IN,PL68D

Nets: ANALOG_B6, ANALOG_B5, ANALOG_B3, FPGA_PPU2_TST2, FPGA_PPU2_TST4, ANALOG_B2, FPGA_B_OE, FPGA_PPU2_TST3, ANALOG_B0, ANALOG_G7, ANALOG_R7, FPGA_PPU2_TST5, FPGA_PPU2_TST7, ANALOG_G6, ANALOG_G5, ANALOG_R6, ANALOG_G4, ANALOG_G3, ANALOG_G2, ANALOG_G1, FPGA_PPU2_TST6, ANALOG_R5, ANALOG_G0, ANALOG_R3, CLK_12MHZ, ANALOG_R4

U1F LFE5U-45F-BG256 — Bank 7

VCCIO7 (H6, H7) +3V3

Pins: ULC_GPLL0T_IN,PL11A, ULC_GPLL0C_IN,PL11B, PL11C, PL11D, PL14A, PL14B, PL14C, PL14D, PL17A, PL17B, PL17C, PL17D, PL20A, PL20B, PL20C, PL20D, PL23A, PL23B, VREF1_7,PL23C, PL23D, PL26A, PL26B, PL26C, PL26D, GR_PCLK7_1,PL29A, GR_PCLK7_0,PL29C, PL29D, PCLKT7_1,PL32A, PCLKC7_1,PL32B, PCLKT7_0,PL32C, PCLKC7_0,PL32D

Nets: FPGA_BURST, FPGA_PPU2_RESOUT1, FPGA_D4, FPGA_D5, FPGA_CSYNC, LVL_TST_DIR, FPGA_PA0, FPGA_PPU2_TST14, LVL_TST_OE, FPGA_PPU2_TST12, LVL_PA_DIR, FPGA_PA1, FPGA_PA2, FPGA_PPU2_TST13, FPGA_PPU2_TST11, FPGA_PPU2_TST10, FPGA_PPU2_TST0, FPGA_PA3, FPGA_PA5, FPGA_PPU2_TST8, FPGA_PPU2_TST9, FPGA_PPU2_TST1, FPGA_PA6, ANALOG_CLK, FPGA_PA7, FPGA_PA4, ANALOG_B7

U1G LFE5U-45F-BG256 — Bank 8

+3V3 VCCIO8 (L6) +3.3V

CFG[2..0] = 001 (Slave SPI mode)

Pin	Signal	Net
N9	MCLK,SCK,CCLK	SPI_CLK
N10	CFG_0	
P10	CFG_1	
R10	CFG_2	
P9	DONE	DONE
T9	INIT	INIT
T7	D1,MISO,IO1,PB11A	SPI_MISO
T8	D0,MOSI,IO0,PB11B	SPI_MOSI
R8	S,CS,PB13A	SPI_CS
P8	CS1,PB13B	ANALOG_R0
N8	HOLD,DI,BUSY,CSSPI,CE	
M8	DOUT,CSO,PB15B	ANALOG_R_OE
M9	WRITE	
T6	D7,IO7,PB4A	USB_PWREN
R6	D6,IO6,PB4B	ANALOG_G_OE
R7	D5,MISO2,IO5,PB6A	USB_SUSPEND
P7	D4,MOSI2,IO4,PB6B	ANALOG_R2
N7	D3,IO3,PB9A	ANALOG_R1
M7	D2,IO2,PB9B	
R9	PROGRAM	PROGRAM

GND

U1H LFE5U-45F-BG256 — JTAG

Pin	Signal	Net
T11	TMS	JTAG_TMS
T10	TCK	JTAG_TCK
R11	TDI	JTAG_TDI
M10	TDO	JTAG_TDO

J_JTAG J2

R13 4.7k, R14 4.7k +3V3 GND

LED4 LED6 — D4 LED, D6 LED — R26 68, R27 68 — GND

(3.3V - 2.0V) / 20mA = 65 ohm

U1I LFE5U-45F-BG256 — Power

+1V1 (G6, G7, G9, L8, L9, L10)
+2V5 (G11, L7) VCCAUX

VCC pins and many GND pins (A1, A16, D2, J15, F8, G8, G10, H1, H8, H9, H10, H16, J8, J9, J10, K6, K7, K8, K9, N2, N15, T1, T2, T15, T16, ...)

TODO: Add decoupling capacitors

GND

Various Control Signals

DIR = A-to-B

+3V3 +3V3 +5V
U20
GND VCCA VCCB
OE
DIR
74LVC8T245-Q1

TP1 TP_FPGA_XIN
FPGA_PAWR A1 B1 TAP_PAWR TP2 TP_TAP_XIN
FPGA_PARD A2 B2 TAP_PARD
FPGA_XIN A3 B3 TAP_XIN
FPGA_PPU1_RESET A4 B4 TAP_PPU2_RESET
FPGA_PPU2_RESET A5 B5 TAP_PPU2_RESET
FPGA_PPU2_PALMODE A6 B6 TAP_PPU2_PALMODE
FPGA_PPU2_TST15 A7 B7 TAP_PPU2_TST15
FPGA_PPU2_HVCMODE A8 B8 TAP_PPU2_HVCMODE
GND

TODO: Rearrange these pins for PCB layout.

DIR = B-to-A

+3V3 +5V
U32
GND VCCA VCCB
OE
DIR
74LVC8T245-Q1

FPGA_PPU2_RESOUT0 A1 B1 TAP_PPU2_RESOUT0
FPGA_PPU2_TOUMEI A2 B2 TAP_PPU2_TOUMEI
FPGA_PPU2_RESOUT1 A3 B3 TAP_PPU2_RESOUT1
FPGA_PPU2_5MOUT A4 B4 TAP_PPU2_5MOUT
FPGA_PPU2_VBLANK A5 B5 TAP_PPU2_VBLANK
FPGA_PPU2_HBLANK A6 B6 TAP_PPU2_HBLANK
FPGA_BURST A7 B7 TAP_BURST
FPGA_CSYNC A8 B8 TAP_CSYNC
GND

J6
J_SAMPLE

Test signals
(NC or GND on original board)

+3V3 +5V
U16
GND VCCA VCCB
LVL_TST_OE OE VCCB
LVL_TST_DIR DIR
74LVC8T245-Q1

FGPA_PPU2_TST14 A1 B1 TAP_PPU2_TST14
FGPA_PPU2_TST13 A2 B2 TAP_PPU2_TST13
FGPA_PPU2_TST12 A3 B3 TAP_PPU2_TST12
FGPA_PPU2_TST11 A4 B4 TAP_PPU2_TST11
FGPA_PPU2_TST10 A5 B5 TAP_PPU2_TST10
FGPA_PPU2_TST9 A6 B6 TAP_PPU2_TST9
FGPA_PPU2_TST8 A7 B7 TAP_PPU2_TST8
A8 B8
GND

Inter-PPU Bus

DIR = B-to-A

+3V3 +5V
U30
GND VCCA VCCB
OE
DIR
74LVC8T245-Q1

FPGA_CHR3 A1 B1 TAP_CHR3
FPGA_CHR2 A2 B2 TAP_CHR2
FPGA_CHR1 A3 B3 TAP_CHR1
FPGA_CHR0 A4 B4 TAP_CHR0
FPGA_PRIO1 A5 B5 TAP_PRIO1
FPGA_PRIO0 A6 B6 TAP_PRIO0
FPGA_COLOR2 A7 B7 TAP_COLOR2
FPGA_COLOR1 A8 B8 TAP_COLOR1
GND

Note: These pins left disconnected, for lack of a better level-shifting solution.

TAP_PPU1_TST0
TAP_PPU1_TST1
TAP_PPU1_TST2

R25
0
GND

DIR = A-to-B

+3V3 +3V3 +5V
U15
GND VCCA VCCB
OE
DIR
74LVC8T245-Q1

Extra 5V signals for bodging.

FPGA_BODGE1 A1 B1 BODGE1
FPGA_BODGE2 A2 B2 BODGE2
FPGA_BODGE3 A3 B3 BODGE3
FPGA_PPU2_EXTLATCH A4 B4 TAP_PPU2_EXTLATCH J3 J_BODGE
FPGA_PPU1_EXTSYNC A5 B5 TAP_PPU1_EXTSYNC
FPGA_PPU1_MASTER A6 B6 TAP_PPU1_MASTER GND
FPGA_PPU1_PALMODE A7 B7 TAP_PPU1_PALMODE
FGPA_PPU1_HVCMODE A8 B8 TAP_PPU1_HVCMODE
GND

+3V3 +5V
U17
GND VCCA VCCB
LVL_TST_OE OE VCCB
LVL_TST_DIR DIR
74LVC8T245-Q1

FGPA_PPU2_TST7 A1 B1 TAP_PPU2_TST7
FGPA_PPU2_TST6 A2 B2 TAP_PPU2_TST6
FGPA_PPU2_TST5 A3 B3 TAP_PPU2_TST5
FGPA_PPU2_TST4 A4 B4 TAP_PPU2_TST4
FGPA_PPU2_TST3 A5 B5 TAP_PPU2_TST3
FGPA_PPU2_TST2 A6 B6 TAP_PPU2_TST2
FGPA_PPU2_TST1 A7 B7 TAP_PPU2_TST1
FGPA_PPU2_TST0 A8 B8 TAP_PPU2_TST0
GND

DIR = B-to-A

+3V3 +5V
U31
GND VCCA VCCB
OE
DIR
74LVC8T245-Q1

FPGA_COLOR0 A1 B1 TAP_COLOR0
FPGA_VCLD A2 B2 TAP_VCLD
FPGA_HCLD A3 B3 TAP_HCLD
FPGA_FIELD A4 B4 TAP_FIELD
FPGA_OVER A5 B5 TAP_OVER
FPGA_5M A6 B6 TAP_5M
FPGA_PPU2_3.58M A7 B7 TAP_PPU2_3.58M
FPGA_PPU2_PED A8 B8 TAP_PPU2_PED
GND

Peripheral Bus

+3V3 +5V
U22
GND VCCA VCCB
OE
LVL_PA_DIR DIR
74LVC8T245-Q1

FPGA_PA0 A1 B1 TAP_PA0
FPGA_PA1 A2 B2 TAP_PA1
FPGA_PA2 A3 B3 TAP_PA2
FPGA_PA3 A4 B4 TAP_PA3
FPGA_PA4 A5 B5 TAP_PA4
FPGA_PA5 A6 B6 TAP_PA5
FPGA_PA6 A7 B7 TAP_PA6
FPGA_PA7 A8 B8 TAP_PA7
GND

VRAM Address Bus

+3V3 +5V
U24
GND VCCA VCCB
OE
LVL_VA_DIR DIR
74LVC8T245-Q1

FPGA_VAA4 A1 B1 TAP_VAA4
FPGA_VAA5 A2 B2 TAP_VAA3
FPGA_VAA2 A3 B3 TAP_VAA2
FPGA_VAA1 A4 B4 TAP_VAA1
FPGA_VAA0 A5 B5 TAP_VAA0
FPGA_VAWR A6 B6 TAP_VAWR
FPGA_VBWR A7 B7 TAP_VBWR
FPGA_VRD A8 B8 TAP_VRD
GND

+3V3 +5V
U26
GND VCCA VCCB
OE
LVL_VA_DIR DIR
74LVC8T245-Q1

FPGA_VAB6 A1 B1 TAP_VAB6
FPGA_VAB5 A2 B2 TAP_VAB5
FPGA_VAB4 A3 B3 TAP_VAB4
FPGA_VAB3 A4 B4 TAP_VAB3
FPGA_VAB2 A5 B5 TAP_VAB2
FPGA_VAB1 A6 B6 TAP_VAB1
FPGA_VAB0 A7 B7 TAP_VAB0
FPGA_VAA13 A8 B8 TAP_VAA13
GND

VRAM Data Bus

+3V3 +5V
U28
GND VCCA VCCB
OE
LVL_VD_DIR DIR
74LVC8T245-Q1

FPGA_VDA7 A1 B1 TAP_VDA7
FPGA_VDA6 A2 B2 TAP_VDA6
FPGA_VDA5 A3 B3 TAP_VDA5
FPGA_VDA4 A4 B4 TAP_VDA4
FPGA_VDA3 A5 B5 TAP_VDA3
FPGA_VDA2 A6 B6 TAP_VDA2
FPGA_VDA1 A7 B7 TAP_VDA1
FPGA_VDA0 A8 B8 TAP_VDA0
GND

+3V3 +5V
U29
GND VCCA VCCB
OE
LVL_VD_DIR DIR
74LVC8T245-Q1

FPGA_VDB7 A1 B1 TAP_VDB7
FPGA_VDB6 A2 B2 TAP_VDB6
FPGA_VDB5 A3 B3 TAP_VDB5
FPGA_VDB4 A4 B4 TAP_VDB4
FPGA_VDB3 A5 B5 TAP_VDB3
FPGA_VDB2 A6 B6 TAP_VDB2
FPGA_VDB1 A7 B7 TAP_VDB1
FPGA_VDB0 A8 B8 TAP_VDB0
GND

TODO: Consider adding decoupling capacitors to all these chips.

+3V3 +5V
U23
GND VCCA VCCB
OE
LVL_PD_DIR DIR
74LVC8T245-Q1

FPGA_D0 A1 B1 TAP_D0
FPGA_D1 A2 B2 TAP_D1
FPGA_D2 A3 B3 TAP_D2
FPGA_D3 A4 B4 TAP_D3
FPGA_D4 A5 B5 TAP_D4
FPGA_D5 A6 B6 TAP_D5
FPGA_D6 A7 B7 TAP_D6
FPGA_D7 A8 B8 TAP_D7
GND

+3V3 +5V
U25
GND VCCA VCCB
OE
LVL_VA_DIR DIR
74LVC8T245-Q1

FPGA_VAA12 A1 B1 TAP_VAA12
FPGA_VAA11 A2 B2 TAP_VAA11
FPGA_VAA10 A3 B3 TAP_VAA10
FPGA_VAA9 A4 B4 TAP_VAA9
FPGA_VAA8 A5 B5 TAP_VAA8
FPGA_VAA7 A6 B6 TAP_VAA7
FPGA_VAA6 A7 B7 TAP_VAA6
FPGA_VAA5 A8 B8 TAP_VAA5
GND

+3V3 +5V
U27
GND VCCA VCCB
OE
LVL_VA_DIR DIR
74LVC8T245-Q1

FPGA_VAB11 A1 B1 TAP_VAB11
FPGA_VAB12 A2 B2 TAP_VAB12
FPGA_VAB10 A3 B3 TAP_VAB13
FPGA_VA14 A4 B4 TAP_VA14
FPGA_VAB10 A5 B5 TAP_VAB10
FPGA_VAB9 A6 B6 TAP_VAB9
FPGA_VAB8 A7 B7 TAP_VAB8
FPGA_VAB7 A8 B8 TAP_VAB7
GND

Sheet: /SPLA Board – PPU/
File: spla-board-ppu.sch

Title: SPLA Board – PPU

Size: A3 | Date: 2020-04-12 | Rev: 8
KiCad E.D.A. kicad 5.1.5-52549c586ubuntu18.04.1 | Id: 5/7

Input Voltage Bias

+5V
R322 301, 1%
R321 1.65k, 1%
ANALOG_B
R323 649, 1%
GND
ALINE_B

+5V
R222 301, 1%
R221 1.65k, 1%
ANALOG_G
R223 649, 1%
GND
ALINE_G

+5V
R122 301, 1%
R121 1.64k, 1%
ANALOG_R
R123 649, 1%
GND
ALINE_R

V = 0v – 3.0v
V = 0.554v – 2.378v
Vrange = 1.824v

Transmission Line Termination

R311 0
C311 NOSTUFF
GND
R211 0
C211 NOSTUFF
GND
R111 0
C111 NOSTUFF
GND

ATERM_B
ATERM_G
ATERM_R

J13 J_ANALOG
1 2
3 4
5 6

(Same as below)

+3.3VA
C307 0.1uF C308 10uF
GND GND

ASCALED_B
R301 16k R302 16k
AOP_F_B
C301 1pF
AOP_P_B
C302 1pF
GND
AOP_N_B
U63 LMH6611
+3.3VA
R308 0
GND
AOP_OUT_B
R309 22
R303 0
R304 INF
GND
C309 390pF
GND
ADC_B

+3.3VA +3.3VA
C353 10uF C351 0.1uF   C352 0.1uF C354 10uF
GND GND   GND GND

VIN 19
VRTS 16
VRT 17
VRB 23
VRBS 22
AVDD 14 15 18
DVDD 11 13
D0 3 ANALOG_B0
D1 4 ANALOG_B1
D2 5 ANALOG_B2
D3 6 ANALOG_B3
D4 7 ANALOG_B4
D5 8 ANALOG_B5
D6 9 ANALOG_B6
D7 10 ANALOG_B7
CLK 2 ANALOG_CLK
OE 1 ANALOG_B_OE
AVSS 20 21 DVSS 24 2
U53 ADC1173
GND GND

AREF_HI
AREF_LO

(Same as below)

+3.3VA
C207 0.1uF C208 10uF
GND GND

ASCALED_G
R201 16k R202 16k
AOP_F_G
C201 1pF
AOP_P_G
C202 1pF
GND
AOP_N_G
U62 LMH6611
+3.3VA
R208 0
GND
AOP_OUT_G
R209 22
R203 0
R204 INF
GND
C209 390pF
GND
ADC_G

+3.3VA +3.3VA
C253 10uF C251 0.1uF   C252 0.1uF C254 10uF
GND GND   GND GND

VIN 19
VRTS 16
VRT 17
VRB 23
VRBS 22
D0 3 ANALOG_G0
D1 4 ANALOG_G1
D2 5 ANALOG_G2
D3 6 ANALOG_G3
D4 7 ANALOG_G4
D5 8 ANALOG_G5
D6 9 ANALOG_G6
D7 10 ANALOG_G7
CLK 2 ANALOG_CLK
OE 1 ANALOG_G_OE
U52 ADC1173
GND GND

AREF_HI
AREF_LO

Non-inverting Sallen-Key Low-Pass Filter

+3.3VA
Decoupling
C107 0.1uF C108 10uF
GND GND

Opamp Feedback
Analog Input
ASCALED_R
R101 16k R102 16k
AOP_F_R
C101 1pF
AOP_P_R
C102 1pF
GND
AOP_N_R
U61 LMH6611
+3.3VA
R108 0
Ignore DISABLE
GND
AOP_OUT_R
R103 0
R104 INF
Topology Option
GND

RC low-pass filter
Cutoff = 1/(2*pi*R109*C109) = 18.55MHz
Output Filter
R109 22
C109 390pF
GND
Analog Output
ADC_R

Design Cutoff Frequency = 10MHz
Cutoff = 1/(2*pi*sqrt(R101*R102*C101*C102)) = 9.947MHz
Q = 0.5

+3.3VA +3.3VA
C153 10uF C151 0.1uF   C152 0.1uF C154 10uF
GND GND   GND GND

VIN 19
VRTS 16
VRT 17
VRB 23
VRBS 22
D0 3 ANALOG_R0
D1 4 ANALOG_R1
D2 5 ANALOG_R2
D3 6 ANALOG_R3
D4 7 ANALOG_R4
D5 8 ANALOG_R5
D6 9 ANALOG_R6
D7 10 ANALOG_R7
CLK 2 ANALOG_CLK
OE 1 ANALOG_R_OE
U51 ADC1173
GND GND

AREF_HI
AREF_LO

+5V
U76 TLV73333PDBV
IN 1 OUT 5
EN 3
GND 2
3.3VA_IN
GND

+3.3VA
Decoupling
C407 0.1uF C408 10uF
GND GND

C401 100pF
R401 33k R402 33k
C402 100pF
GND
U74 LMH6611
AREF_HI_OP
+3.3VA
R408 0
Ignore DISABLE
GND

Design Cutoff Frequency = 50kHz
Cutoff = 1/(2*pi*sqrt(R401*R402*C401*C402)) = 48.23kHz
Q = 0.5

+3.3VA
Decoupling
C507 0.1uF C508 10uF
GND GND

C501 100pF
R501 33k R502 33k
C502 100pF
GND
U75 LMH6611
AREF_LO_OP
+3.3VA
R508 0
Ignore DISABLE
GND

+3.3VA
PWR_FLAG
J14 J_AREF
1 2
3 4
5 6
7 8
R601 1.65k, 1%
AREF_HI = 2.412V
R602 3.48k, 1%
R603 1k, 1%
AREF_LO = 0.538V
GND

J8 J_AREF_AMP
1 2
3 4
TP3 TP_AREF_HI
TP4 TP_AREF_LO
AREF_HI
AREF_LO

TODO: Validate all this nonense with somebody who knows what they're doing.

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File: spla-board-analog.sch
Title:
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