Compact implementations of pairings

Anthony Van Herrewege

Day. sup.: Dr. Lejla Batina, Miroslav Knezevic, Dr. Ir. Nele Mentens
Prom.: Prof. Dr. Ir. Ingrid Verbauwhede, Prof. Dr. Ir. Bart Preneel
Ass.: Prof. Dr. Ir. Wim Dehaene, Dr. Ir. Frederik Vercauteren

22 May 2009

Notes

Outline

1 Pairings

2 Implementation

3 Results

Notes

Overview

- Several available pairings:

  Weil, Tate, η_T, Ate, ...
- Bilinearity property:

$$e(P_1 + P_2, Q) = e(P_1, Q) \cdot e(P_2, Q)$$

- *Optimized* Tate pairing:

$$\hat{e}(P, Q) : E(\mathbb{F}_q)[l] \times E(\mathbb{F}_q)[l] \mapsto \mu_l$$

$$\mu_l = \text{group of } l\text{th roots of } \mathbb{F}_{q^k}^*$$

Notes

Possibilities

- Identity-based encryption
- Short signatures
- Non-interactive key agreement
- Tripartite key agreement in 1 round
- ...

Notes

Restrictions

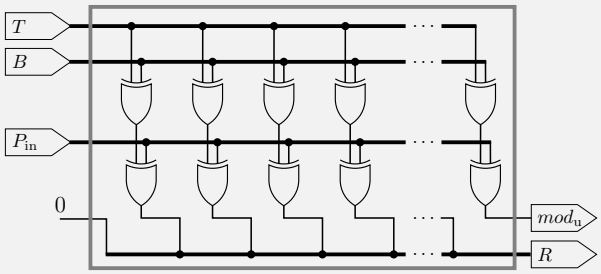
Avoid the use of flip-flops and muxes:

Cell	Area $\left[\frac{\text{gate}}{\text{bit}}\right]$
D flip-flop (reset)	6
D flip-flop (no reset)	5.5
D latch	4.25
3 input MUX	4
2 input XOR	3.75
2 input MUX	2.25
2 input NAND	1
NOT	0.75

Notes

MALU - Addition & Reduction in $\mathbb{F}_{2^m}$

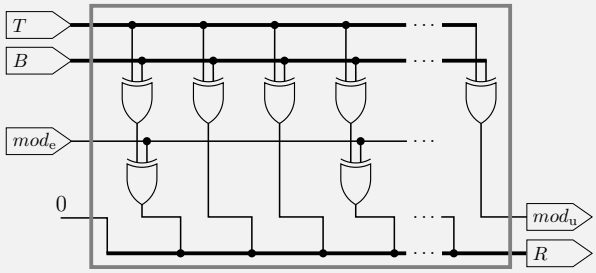
$$R = (T + B \pmod{P_{\text{in}}})_{0:m-2} \ll 1$$
$$mod_{\text{u}} = (T + B \pmod{P_{\text{in}}})_{m-1}$$



Notes

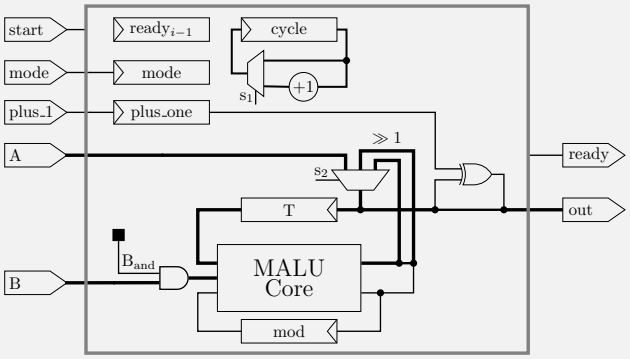
MALU - Addition & Reduction in $\mathbb{F}_{2^m}$

Optimized MALU needs $\Delta = m - (\text{Hamm}(P) - 1)$ less XORs:



Notes

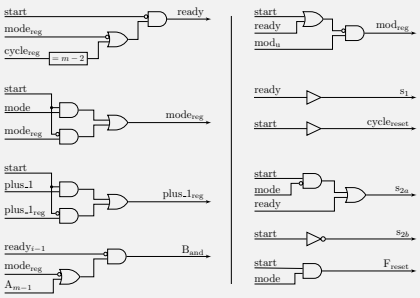
$\mathbb{F}_{2^m}$ Multiplication & Addition



Notes

$\mathbb{F}_{2^m}$ Multiplication & Addition

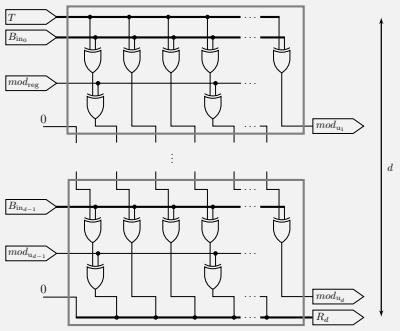
No FSM needed, simple logic:



Notes

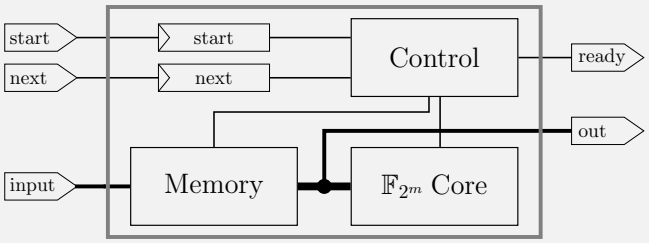
$\mathbb{F}_{2^m}$ Multiplication & Addition

Speed up calculation by daisy-chaining MALUs ($m \bmod d$!):



Notes

Controller for Miller's algorithm

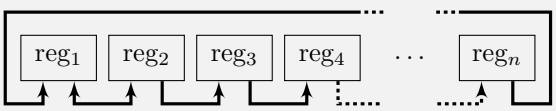


Notes

Memory design

Initial design:

$$\bar{t} = O\left(\frac{n^2}{3}\right) \qquad \overline{w} = O\left(\frac{n^3}{3}\right)$$

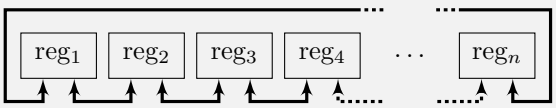


Notes

Memory design

Final design:

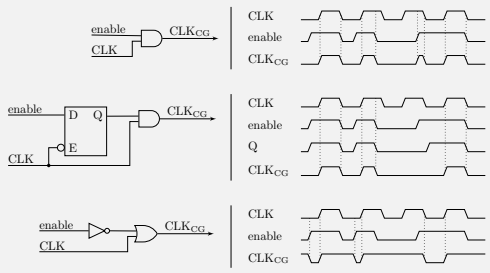
$$\bar{t} = O\left(\frac{n}{4}\right) \qquad \overline{w} = O(n)$$



Notes

Optimizations

- Remove reset from registers $\left(-0.5\ \frac{\text{gate}}{\text{bit}}\right)$
- Implement clock gating:

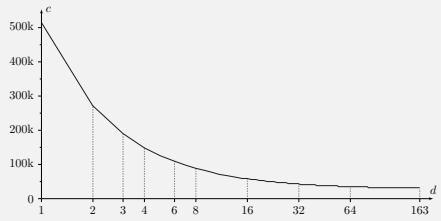


Notes

Runtime

- FSM with 553 states
- Total n° of clock cycles c for one pairing:

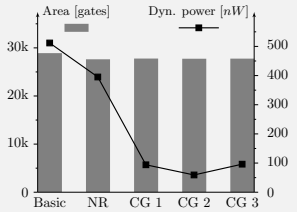
$$c = 21681 + 4322 + 2998 \cdot \left\lceil \frac{m}{d} \right\rceil$$



Notes

Synthesis

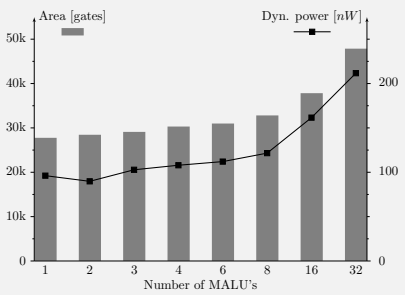
Implementation	Area [gates]		Power @ 10 kHz [nW]			
			Dynamic		Leakage	
Basic	28 876		512		117	
No Reset	27 596	96%	395	77%	107	92%
CG 1	27 751	96%	94	18%	109	94%
CG 2	27 713	96%	59	12%	102	88%
CG 3	27 734	96%	96	19%	110	94%



Notes

Synthesis - Continued

Component	Opp. [gates]	
MALU	458	1.7%
$\mathbb{F}_{2^m}$ core		
Logic	783	2.8%
Registers	962	3.5%
Controller		
Logic	13 044	47%
Registers	12 487	45%
Total	27 734	100%



Notes

Comparison

	This work		Beuchat *et al.*
	1 MALU	2 MALUs	
Field	$\mathbb{F}_{2^{163}}$	$\mathbb{F}_{2^{163}}$	$\mathbb{F}_{3^{97}}$
Pairing	Tate	Tate	η_T
Security [bit]	652	652	922
Technology [μm]	0.13	0.13	0.18
Area [gates]	27 430	28 155	193 765
f [MHz]	10.3	5.44	200
Calc. time [μs]	$50 \cdot 10^3$	$50 \cdot 10^3$	46.7
Power [mW]	$98.3 \cdot 10^{-3}$	$48.6 \cdot 10^{-3}$	672
Efficiency [$\frac{nJ}{\text{bit}}$]	7.54	3.73	34.0

$$\text{Efficiency} = \frac{\text{power} \times \text{calc. time}}{\text{bits security}}$$

Notes

Conclusion

- Very small: < 30k gates
- Extremely low power: < 220 nA
- Energy efficiency improvement up to more than $25\times$ possible

Definitely possible to use in constrained environments

- Example with 3 MALUs:

Area $= 29$k gates	$f = 9.70$ Mhz
Power $= 100\ \mu$A	Time $= 19.6$ ms

Notes

The end

Questions?

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