THE IMPACT OF CLOCK GATING SCHEMES ON THE POWER DISSIPATION OF SYNTHESIZABLE REGISTER FILES

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ABSTRACT

In this paper, the power dissipation of synthesizable register files with respect to different clock gating schemes is examined. Clock gating is a well-known technique for power reduction of sequential circuits. Although different clock gating schemes exist, there is no fundamental difference in the power dissipation of sequential logic because the data input signals of disabled flip-flops do not change when the clock signal is disabled. However, it is shown here that in contrast to sequential logic the clock gating scheme has significant impact on the power dissipation of register files due to signal changes of the data input port. The major result of this work is that the power dissipation of register files can be reduced significantly, if a clock gating scheme different from that one usually recommended for sequential logic is applied.

1. INTRODUCTION

One of the most important challenges in modern VLSI design is the reduction of power dissipation. The limited energy capacitance of batteries used for mobile systems and devices like laptops, mobile phones, digital cameras or personal digital assistance (PDA) constrains the operating time without battery recharging. In addition, with increasing clock frequencies and chip complexity the costs for heat removal and packaging due to a significant power dissipation has become a major concern [1, 2, 3].

Besides reduction of power dissipation, increased chip complexity changed the design methodology for complex CMOS circuits from the traditional full custom design style to an automated semi-custom design flow. The main reason for these structural changes is the design productivity which must cope with the exponential increase in design complexity. Even with the introduction of an automated semi-custom design flow, the ever increasing design complexity has led to the necessity of further productivity improvements. In order to achieve this, design reuse with synthesizable processors and soft IP cores has become the focus of attention in the last years. These cores are often implemented on register transfer level (RTL) as soft macros applying a hardware description language (HDL) like Verilog or VHDL. Data stores are an important power critical part of these architectures. They can be implemented either as RAM or as synthesizable register files. For large data stores RAM is often preferred due to its area efficiency. Nevertheless, in context of soft IP cores, RAM has several drawbacks compared to synthesizable register files. RAMs are designed on the physical level like hard macros such that they are very technology dependent, integration into the design causes high efforts especially in the backend of the design flow (timing closure). Synthesizable register files fit very well into the design flow. They are synthesized as part of the RTL model, static timing analysis and formal verification are applicable, testing can be performed using scan chains. In addition, they are local data stores which can be scaled to arbitrary sizes suitable for the application and no complex memory controllers are needed. Therefore, they are often used for soft IP cores, digital filters or application specific processor cores.

For these reasons, we focus on the power reduction of synthesizable register files. Clock gating is often used in order to reduce the power dissipation of disabled modules [4, 5] and can be applied for synthesizable register files as power efficient write access control logic. It is very well integrated into semi-custom design flows nowadays [6]. Dedicated clock gating cells are integrated into the clock path by the synthesis tool such that edge triggered flip-flops can be disabled, by setting the clock signal of the flip-flops to a predefined, constant value. The power dissipation due to transitions on the data signal of a flip-flop highly depends on the state of the clock signal [7, 8]. In this paper it is shown, that in contrast to usual sequential circuits different clock gating schemes [4] lead to significant differences in power dissipation, if they are applied to register files.

The paper is organized as follows: In Section 2 and 3 the power dissipation of flip-flops usually used in standard cell libraries and of register files is examined and modeled. The impact of the clock gating scheme chosen on power dissipation of conventional sequential logic and register files is addressed in Section 4. In Section 5 experimental results are presented.

2. POWER DISSIPATION OF LIBRARY FLIP-FLOPS

As synthesizable register files consist of flip-flops, the power dissipation of a typical flip-flop of a semi-custom library is discussed in this section. These flip-flops are mostly realized as edge-triggered master-slave D flip-flops. Unless otherwise expressly mentioned, we consider these flip-flops exclusively in the following. As positive and negative edge-triggered flip-flops do not differ in principle, we restrict our considerations on positive-edge triggered flip-flops. In order to discuss the power dissipation, the schematic of a flip-flop is shown in Fig. 1 a) and b). In order to simplify the discussion concerning normal operation, additional logic like reset, set or scan logic is not considered in the following. This can be included in the power model, if necessary but has no influence on further discussions.

In the following, we discuss the power consumption of the flip-flop assuming transitions on the data input signal *D* and a stable clock signal *CK*. In Fig. 1 a) the clock signal is *CK*='1'. Since the master latch is not transparent in this case, only the input gate

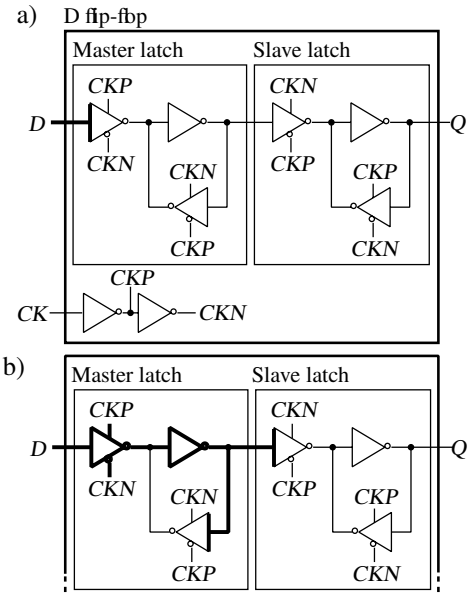

Fig. 1. Schematic of a positive edge-triggered D flip-flop. a) Internal nodes, which are recharged, if the clock signal is equal to '1'. b) Internal nodes, which are recharged, if the clock signal is equal to '0'.

capacitances (marked bold) are reloaded. Fig. 1 b) shows the situation when the clock signal is *CK*='0'. Transitions on the data signal affect the internal nodes (marked bold) of the master latch and the gate capacitances of the slave latch. For this reason, the power consumption of the flip-flop is much higher if the clock signal is '0'. The results of simulations of flip-flops of typical industrial standard cell libraries (e.g. 0.18μ process technology) show that the energy consumed by the flip-flop increases by the factor of 35 – 40 in the case of a transparent master latch.

In order to model this behavior of a flip-flop on the highest level of abstraction, we consider the power dissipation P_{FDH} and P_{FDL} of the flip-flop datapath for a high or low state of the clock signal. The power dissipation of the clock path is denoted as P_{FC}. The switching activity α_{FDH} and α_{FDL} is defined as the number of signal changes of the data per clock period during high and low phase of the clock signal. The switching activity of the clock signal is $\alpha_{\mathrm{FC}} = 1$. Let V_{DD} be the supply voltage and f be the clock frequency of the flip-flop. The total dissipated power P_{F} of a flip-flop F is given by the following equation:

$$P_{\mathrm{F}} = P_{\mathrm{FD}} + P_{\mathrm{FC}} = P_{\mathrm{FDL}} + P_{\mathrm{FDH}} + P_{\mathrm{FC}} \quad (1)$$

$$= (\alpha_{\mathrm{FDL}} C_{\mathrm{FDL}} + \alpha_{\mathrm{FDH}} C_{\mathrm{FDH}} + \alpha_{\mathrm{FC}} C_{\mathrm{FC}}) V_{\mathrm{DD}}^2 f. \quad (2)$$

The parameter C_{x} with $x \in \{\mathrm{FDL}, \mathrm{FDH}, \mathrm{FC}\}$ is the equivalent capacitance which models the power dissipation on the standard cell abstraction level. This equivalent capacitance is defined as: $C_{\mathrm{x}} = P_{\mathrm{x}}/(\alpha_{\mathrm{x}} V_{\mathrm{DD}}^2 f)$. Thus, the power dissipation of all transistors of a standard cell and the short circuit currents across n- and p-transistors are included. A more detailed power model on transistor level is not required for our purpose. The effect mentioned above that the dissipated power of the flip-flop depends on the clock phase can be formulated as follows:

$$\frac{C_{\mathrm{FDL}}}{C_{\mathrm{FDH}}} \sim 35 - 40 \quad \text{or} \quad C_{\mathrm{FDL}} \gg C_{\mathrm{FDH}}. \quad (3)$$

This equation has special impact on synthesizable register files as shown in Section 4.

3. POWER DISSIPATION OF SYNTHESIZABLE REGISTER FILES

Clock gating is a well-known technique for power efficient addressing in register file structures [4]. Modern EDA-tools used in semi-custom design flows are capable of integrating clock gating circuits or special clock gating cells into the design [6]. Fig. 3 b) depicts a register file of n registers with w bits connected to the data bus D. The address logic is realized by one clock gating cell CG for each word-level register. In most applications the value of only one register changes at each clock cycle while the remaining registers are not altered. The addressed register and the corresponding clock gating cell are indicated in Fig. 3 b) by the shaded elements.

The total power dissipation P_{RFCG} of the register file with clock gating consists of the power dissipation of the clock-gating cells P_{CG}, the power dissipation of the flip-flops P_{F} and the power dissipation of the multiplexer P_{M} (not shown in Fig. 3). The register file without clock gating is denoted as P_{RF}.

$$P_{\mathrm{RF}} = \sum_{i=1}^{nw} P_{\mathrm{F}}(i) + P_{\mathrm{M}} \quad (4)$$

$$P_{\mathrm{RFCG}} = \sum_{i=1}^{n} P_{\mathrm{CG}}(i) + \sum_{i=1}^{nw} P_{\mathrm{F}}(i) + P_{\mathrm{M}}. \quad (5)$$

As only one word-level register is addressed for the register file with clock gating and all registers are assumed to be identical, we obtain:

$$P_{\mathrm{RF}} = nwP_{\mathrm{FC}} + nwP_{\mathrm{FD}} + P_{\mathrm{M}} \quad (6)$$

$$P_{\mathrm{RFCG}} = nP_{\mathrm{CG}} + wP_{\mathrm{FC}} + nwP_{\mathrm{FD}} + P_{\mathrm{M}}. \quad (7)$$

Obviously, the product nwP_{FC} of P_{RF} is larger than $nP_{\mathrm{CG}} + wP_{\mathrm{FC}}$ of P_{RFCG} especially for large n and w such that $P_{\mathrm{RFCG}} \ll P_{\mathrm{RF}}$. Therefore, clock gating should be applied for low power register files in any case. In commercial semi-custom design flows, automated clock gating has been established as a standard methodology [6, 9].

4. LOW POWER REGISTER FILES USING CLOCK GATING WITH A LOGIC HIGH DISABLED CLOCK

Clock gating can be implemented in two ways. The clock input of the registers is disabled by the clock gating cell either with a logic high or low signal. Both versions are discussed in detail in [4] and [9]. For a logic low disabled clock, the clock gating cell can be implemented using an AND gate and a latch denoted as scheme 1 in [4], see Fig. 2 a). The AND gate switches off the clock signal during the second half of the period, while the latch switches off the clock signal in the first half of the clock period, if the clock is disabled with EN ='0'. Thus, glitches of the enable signal EN, which may occur before the end of the clock period, are not propagated to the gated clock signal $CG1$.

For a logic high disabled clock, the corresponding clock gating cell is shown in Fig. 2 b). To avoid glitch propagation into the gated clock signal $CG2$ the enable signal has to settle within the first half of the clock cycle. This is no limitation in most cases, since the logic depth of the write enable signal is limited and can

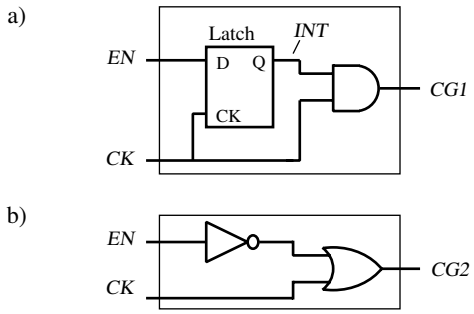

Fig. 2. a) Clock gating scheme 1, b) clock gating scheme 2.

be assured by the application of a timing constraint for logic synthesis. Especially for register files, this is the case. This scheme of clock gating is denoted as scheme 2 in [4].

4.1. Power Dissipation Using Clock Gating Scheme 1 and 2

The significant difference of both clock gating schemes concerning power dissipation of register files is the logic level of the gated clock signal. As shown in Section 2, the flip-flop's master latches are transparent to changes on the data input if *CK*='0'. If clock gating with scheme 1 is applied, this is the case for all disabled registers. If transitions on the data signal of disabled registers occur, power dissipation can be reduced significantly if clock gating with scheme 2 is applied.

Whether data transitions occur when the clock is switched off depends on the circuit architecture. If the clock is switched off for a circuit as shown in Fig. 3 a), no transitions on the data path will occur, if we assume that the asynchronous delay of the data paths are smaller than one clock cycle. This should generally be the case. Therefore, the power dissipation of the circuit in Fig. 3 a) is not effected significantly, whether clock gating scheme 1 or scheme 2 is chosen. As scheme 1 gives the opportunity of a full clock cycle for the enable signal, the clock gating scheme 1 has been established in most semi-custom design design flows.

In contrast to the circuit shown in Fig. 3 a), the power dissipation can be reduced significantly, if the clock gating scheme 2 is applied to register files as shown in Fig. 3 b). Data transitions occur at the data input of all registers of the register file when data are written to one register. During the write access, the majority of registers $(n-1)$ are switched off due to clock gating. The average power dissipation of a register file P_{RFCG1} and P_{RFCG2} with clock gating scheme 1 and 2 is:

$$P_{\mathrm{RFCG1}} = P_{\mathrm{M}} + nP_{\mathrm{CG1}} + wP_{\mathrm{FC}} + w(P_{\mathrm{FDH}} + (n-1)P_{\mathrm{FDL}}) \quad (8)$$

$$P_{\mathrm{RFCG2}} = P_{\mathrm{M}} + nP_{\mathrm{CG2}} + wP_{\mathrm{FC}} + w((n-1)P_{\mathrm{FDH}} + P_{\mathrm{FDL}}). \quad (9)$$

The difference $P_{\Delta} = P_{\mathrm{RFCG1}} - P_{\mathrm{RFCG2}}$ with $P_{\mathrm{FDL}} \gg P_{\mathrm{FDH}}$ is:

$$P_{\Delta} \approx n(P_{\mathrm{CG1}} - P_{\mathrm{CG2}}) + w(n-2)P_{\mathrm{FDL}} \quad (10)$$

$$= n(P_{\mathrm{CG1}} - P_{\mathrm{CG2}}) + w(n-2)\alpha_{\mathrm{FDL}} C_{\mathrm{FDL}} V_{\mathrm{DD}}^2 f. \quad (11)$$

According to (11), the absolute power savings using scheme 2 increases linear with the transition probability α_{FDL}, the wordlength of the data bus w and the number of registers n connected to the data bus. The value of α_{FDL} is strongly data dependent. If uncorrelated data which change every clock cycle are assumed, the transition probability is $\alpha_{\mathrm{FDL}} = 0.25$. If additional glitches occur

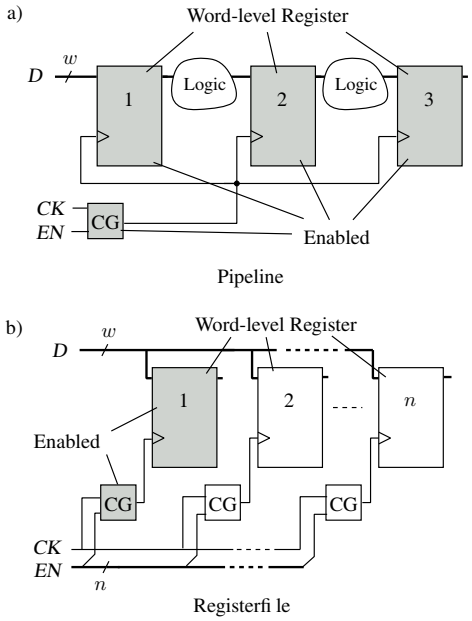

Fig. 3. Pipeline architecture a), register file b).

on the input of the register file due to combinatorial logic, the transition probability can be $\alpha_{\mathrm{FDL}} \gg 0.25$. For example, this is the case if the register file is used in a single cycle processor architecture such that the ALU is connected to the register file input. Even if $\alpha_{\mathrm{FDL}} < 0.25$, a significant part of the power dissipation can be saved (see Section 5). Simulations of an ARM7 processor core applying Dhrystone-Benchmark stimuli show a switching activity α_{FDL} of the data signal of 0.23 including glitches. Even for $\alpha_{FDL} = 0$ the power savings is $P_{\Delta} = n(P_{\mathrm{RFCG1}} - P_{\mathrm{RFCG2}})$ which is due to the difference of the clock gating cells. The clock gating cell of scheme 2 is less complex compared to the latch and AND gate of scheme 1 such that less power is dissipated in the clock gating cell of scheme 2.

For these reasons, clock gating scheme 2 should be used for low power register files. This is an important exception to the widely accepted recommendation to use clock gating scheme 1 in general because no significant power reduction can be achieved with scheme 2 in usual sequential logic as stated in [9].

5. EXPERIMENTAL RESULTS

In Table 1, the power consumption of the flip-flops and the register file including the flip-flops, the clock-gating cells and the multiplexers are shown. The power savings achieved with clock gating scheme 2 are given as relative numbers compared to scheme 1. The register files were synthesized from a VHDL RTL model applying a commercial synthesis tool. The power simulations were performed on transistor-level (0.18μ technology) using the gate level netlist from synthesis.

For high switching activities of $\alpha_{\mathrm{FD}} = 0.25$ power savings of about 70 % have been achieved. The switching activity is $\alpha_{\mathrm{FD}} = 0.25$, if the data changes each clock cycle and an equal probability of 0's and 1's are assumed. Due to (11), the power savings are linear with the switching activity. This is consistent with the simulation results of Table 1 and the graphical representation in Fig. 4.

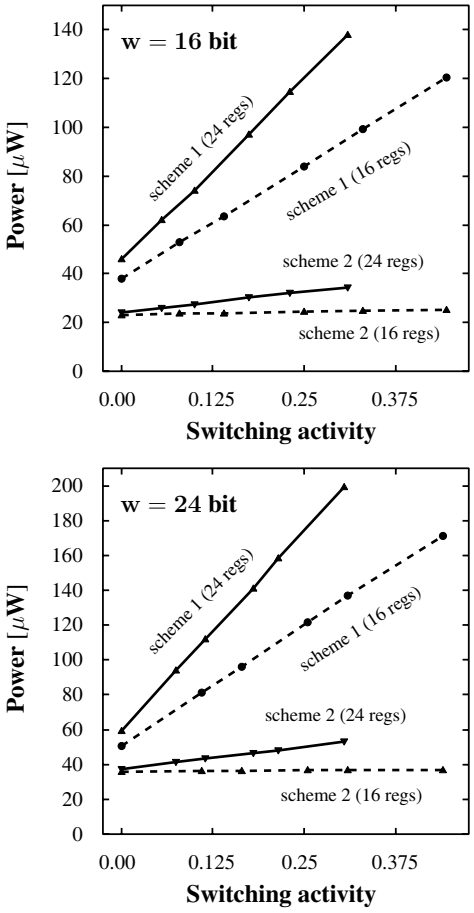

Fig. 4. Power consumption of the register file using clock gating scheme 1 and scheme 2.

For a switching activity of $\alpha_{FD} = 0.025$, which is equivalent to only one change of data every 10 cycles, the extrapolated figure for power reduction is still between 35 % and 40 %. If there are no transitions on the data input signal ($\alpha_{FD} = 0$), the power savings are still over 30 % although only the transitions on the clock signal of the clock gating cells cause the power dissipation. Switching activities $\alpha_{FD} > 0.25$ may also be relevant, if glitches occur at the data input of the register file. This is the case, if the register file is connected to combinatorial logic like a ALU or multiplexer. A typical application for this scenario is a single cycle architecture.

6. CONCLUSION

In this paper, the power dissipation of synthesizable register files was modeled for different clock gating schemes. The energy consumption due to transitions of the data signal of master-slave D flip-flops is strongly dependent on the state of the clock signal. If the clock signal is '0', the master latch of the flip-flop is transparent and the power dissipation of the flip-flop due to transitions on the data signal is significantly higher than if the clock signal is '1'. This is an important issue, because the clock signal of disabled flip-flops is set to a predefined, constant value if clock gating is applied. Although this is negligible for conventional sequential logic because the data inputs of disabled flip-flops do not change in this case, synthesizable register files strongly benefit from clock gating scheme 2. The clock signal of disabled flip-flops is set to '1' in this case. Depending on the transition activity of the data signal, the power dissipation of the register file can be reduced significantly if an alternative clock gating scheme is applied.

Table 1. Simulation results for the power consumption of the flip-flops and the register file including the flip-flops, clock-gating cells and multiplexers for a 0.18μ process technology.

α_{FD}	Flip-flops scheme 1 [μW]	Flip-flops scheme 2 savings	Register file scheme 1 [μW]	Register file scheme 2 savings
16 bit wordlength – 16 word-level registers				
0.00	18.06	0.3%	37.44	38.1%
0.08	32.90	44.0%	52.89	55.4%
0.14	43.55	57.1%	63.55	62.5%
0.25	63.94	69.9%	83.95	70.9%
0.33	79.23	75.2%	99.25	74.9%
0.45	100.39	80.2%	120.48	79.2%
24 bit wordlength – 16 word-level registers				
0.00	29.80	0.1%	50.78	29.2%
0.11	60.11	50,0%	81.16	55.3%
0.17	74.90	59.7%	95.98	62,0%
0.25	100.44	69.9%	121.57	69,9%
0.31	115.67	73.8%	136.84	73.2%
0.44	150.18	79.6%	171.42	78,4%

7. REFERENCES

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