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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/599,191	05/18/2017	Hoon Lee	8836S-1189 (ID-260303-US)	2207

22150 7590 09/18/2018

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EXAMINER	
JAGER, RYAN C	

ART UNIT	PAPER NUMBER
2842	

NOTIFICATION DATE	DELIVERY MODE
09/18/2018	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

garramone@chauiplaw.com
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Office Action Summary	Application No. 15/599,191	Applicant(s) Lee et al.	
	Examiner RYAN C JAGER	Art Unit 2842	AIA Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☑ Responsive to communication(s) filed on 04 September 2018.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL.** 2b) ☑ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5) ☑ Claim(s) 1-20 is/are pending in the application.

5a) Of the above claim(s) 11-15 is/are withdrawn from consideration.

6) ☐ Claim(s) _____ is/are allowed.

7) ☑ Claim(s) 1-2,9-10 and 16-20 is/are rejected.

8) ☑ Claim(s) 3-8 is/are objected to.

9) ☐ Claim(s) _____ are subject to restriction and/or election requirement

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to **PPHfeedback@uspto.gov.**

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☑ The drawing(s) filed on 5/18/17 is/are: a)☑ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☑ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☑ All b)☐ Some** c)☐ None of the:

1.☑ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☑ Notice of References Cited (PTO-892)

2) ☑ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date 5/18/17.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date _____.

4) ☐ Other: _____.

1. The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

DETAILED ACTION

2. Non-final communication in response to communication filed 9/4/18.

Election/Restrictions

3. Applicant's election without traverse of species I, figures 1-13, claims 1-10, 16-20 in the reply filed on 9/4/18 is acknowledged.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a)(1) the claimed invention was patented, described in a printed publication, or in public use, on sale or otherwise available to the public before the effective filing date of the claimed invention.
>
> (a)(2) the claimed invention was described in a patent issued under section 151, or in an application for patent published or deemed published under section 122(b), in which the patent or application, as the case may be, names another inventor and was effectively filed before the effective filing date of the claimed invention.

5. Claim(s) 1,2,9,10,16-20 is/are rejected under 35 U.S.C. 102(a)(2) as being anticipated by Jung 9443565.

With respect to claim 1 figures 6 and 7 of Jung disclose a delay locked loop comprising:

a delay line [124] configured to delay an input clock signal [DCLK] in units of unit delay in response to a delay control code [SELn] to generate an output clock signal [OCLK];

a delay circuit [136,134] configured to delay the output clock signal to generate a delay clock signal [FCLK];

a phase detector [130] configured to compare the input clock signal and the delay clock signal to generate a phase detection signal [UP/DN];

a delay code generator [150] configured to compare the input clock signal and the delay clock signal to detect a phase difference there between and generate a delay code [CONS] using the phase difference; and

a delay controller [133] configured to generate the delay control code using the delay code and the phase detection signal.

With respect to claim 2 figures 6 and 7 of Jung disclose the delay locked loop of claim 1, wherein the delay code generator maintains the delay code, generated using a first cycle of the input clock signal, during a locking process of the delay locked loop.

With respect to claim 9 figures 6 and 7 of Jung disclose the delay locked loop of claim 1, wherein the delay controller generates an initial delay control code using the delay code and shifts the initial delay control code in response to the phase detection signal to generate the delay control code.

With respect to claim 10 figures 6 and 7 of Jung disclose the delay locked loop of claim 1, wherein the delay code and the delay control code are initialized by a reset signal. [col. 8, lines 61-67].

With respect to claim 16 figures 6 and 7 of Jung disclose a method of performing a coarse lock process using a delay locked loop [fig. 6], the method comprising:

receiving, at a phase detector [130], an input clock signal [DCLK] and a delay clock signal [FCLK], wherein the delay clock signal is an output clock signal [OCLK] of the delay locked loop that is delayed for a predetermined amount of time [134,136];

determining, by the phase detector, a phase difference between the input clock signal and the delay clock signal to generate a phase detection signal [UP/DN];

receiving, at a delay code generator [150], the input clock signal and the delay clock signal;

generating, by the delay code generator, a delay code [CONS] using the input clock signal and the delay clock signal;

receiving, at a delay controller [133], the phase detection signal and the delay code;

generating, by the delay controller, a delay control code [SELn] using the phase detection code and the delay code; and

receiving, at a delay line [124], the input clock signal and the delay control code to generate the output clock signal.

With respect to claim 17 figures 6 and 7 of Jung disclose the method of claim 16, wherein in a first cycle of the input clock signal, the delay code generator generates an initial delay code, and after the first cycle, the initial delay code is maintained.

With respect to claim 18 figures 6 and 7 of Jung disclose the method of claim 16, wherein the delay locked loop performs a first loop and a second loop,

the first loop includes receiving the phase detection signal and the delay code at the delay controller and generating the delay control code, and

the second loop includes receiving the input clock signal and the delay clock signal at the delay code generator and generating the delay code.

With respect to claim 19 figures 6 and 7 of Jung disclose the method of claim 16, further comprising:

comparing, by the phase detector, the input clock signal with the delay clock signal to determine that the delay locked loop is coarse-locked; and

completing the coarse lock process by generating a coarse lock signal. [figure 5 shows coarse lock step]

With respect to claim 20 figures 6 and 7 of Jung disclose the method of claim 16, further comprising:

comparing, by the phase detector, the input clock signal with the delay clock signal to determine that the delay locked loop is not coarse-locked;

generating the phase detection signal using the input clock signal and the delay clock signal, wherein the phase detection signal is either a code rising signal or a code falling signal [UP/DN]; and

updating the delay control code using the phase detection signal.

Allowable Subject Matter

6. Claims 3-8 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to RYAN C JAGER whose telephone number is (571)272-7016. The examiner can normally be reached on 8:30 - 5:30 PM.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is

encouraged to use the USPTO Automated Interview Request (AIR) at http://www.uspto.gov/interviewpractice.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lincoln Donovan can be reached on 571-272-7016. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Ryan Jager/
Primary Examiner, Art Unit 2842
9/12/18