CANBERRA

Features

- 900 ns Fixed Dead Time ADC
- 8K channel resolution
- Digital offset in 128 channel increments
- Exceptional linearity (differential <±0.9%, integral <±0.025%)
- Pulse Height Analysis using either automatic peak detection or delayed triggering
- Analog Sample Voltage Analysis
- Pulse pileup rejection and live time correction interfaces
- Compatible with Loss Free Counting Systems[1]

1. US patent 4,476,384.
2. G. P. Westphal, Nuclear Instruments and Methods 163 (1979) 189-196.

Model 8715
Analog-to-Digital Converter

Description

The Model 8715 Analog-to-Digital Converter (ADC) is an ultra-fast 900 ns, Fixed Dead Time, analog-to-digital-converter for high count rate nuclear spectroscopy. This highly linear, 8K ADC contributes no system dead time to spectroscopy systems using traditional Gaussian or Triangular Shaping amplifiers.

The Model 8715 boasts differential and integral linearity performance that until now was only possible with Wilkinson ADCs. Its exceptional linearity improves peak shape and resolution, thereby improving the overall performance of your spectroscopy system. It requires a single NIM width.

Concentric Gain and Range controls together with Digital Offset allow the user to maximize the use of limited MCA memory by selecting only the specific energy range of interest. This can be particularly useful for multi-input applications such as alpha spectroscopy, thus eliminating the need for older biased amplifiers. These digital controls accomplish the same end, more accurately and repeatably.

Conversion for the Pulse Height Analysis (PHA) mode can be initiated AUTOmatically using an internal peak detector operating on the input pulse, or can be DELAYED up to 100 µs after the leading edge of the input pulse passes the input threshold. A front panel INSPEct test point is provided so that the user can monitor the Linear Gate (LG) time between LLD crossing and the beginning of conversion for either mode. Conversions may be enabled/disabled by COINCidence/ANTIcoincidence gating applied at any time during the Linear Gate interval.

Voltage sampling and subsequent conversion for the Sampled Voltage Analysis (SVA) mode is initiated by the leading and trailing edges, respectively, of a Gate pulse applied in the Coincidence mode. The same Lower and Upper Level Discriminators (LLD/ULD) limits are used for acceptance of the peak input during the positive gate time. The Model 8715 provides front panel, screwdriver adjustable, multi-turn potentiometers for the control of the LLD/ULD, as well as the ADC Zero.

The Model 8715 provides the connections required for use with current CANBERRA amplifiers that perform pileup rejection and live time correction (PUR/LTC). These ADC/amplifier interfaces are also required to use the Westphal Loss Free Counting or Precision Live Time techniques.[2]

The Model 8715 ADC is fully compatible with all current CANBERRA MCAs (with external ADC interface options such as the Model 556B), Digital Stabilizer and Analog Multiplexers.

CANBERRA IS THE NUCLEAR MEASUREMENTS BUSINESS UNIT OF AREVA.   www.canberra.com

We are 66 **Measurement solutions for nuclear safety and security.**   M2562 8/07 Printed in U.S.A.

Model 8715 Analog-to-Digital Converter

Specifications

INPUTS

- **ADC IN** – Accepts positive unipolar or bipolar (positive lobe leading) pulses for PHA, and dc level or pulses for the SVA mode; amplitude 0 to +10 V, +12 V maximum; rise time 0.25 to 100 µs maximum; width 0.5 µs minimum; Z_{in} = 5 kΩ, direct coupled; front panel BNC.

- **GATE IN** – Accepts a positive logic pulse or dc level; high amplitude ≥+2.5, Low amplitude ≤400 µV, 0 to +7 V maximum; dc coupled; Loading with COINCidence selected is 1 kΩ to +5 V and 1 kΩ to 0 V for ANTIcoincidence; width ≥250 ns; PHA analysis does not require a gate input; minimum gate pulse width for SVA is 1 µs.

- **DEAD TIME** – Rear panel BNC connector which receives an external dead time INPUT. Accepts a negative or positive logic signal, internal jumper, which is ORed with the ADC dead time; negative true amplitude ≤400 mV, positive true amplitude ≥+2.5 V, 0 to +7 V maximum; loading 2.2 kΩ to +5 V. The composite dead time signal may be accessed through pin 6 of the rear panel DATA connector. Internal jumper plug selects the output composite dead time signal polarity, positive true or negative true; shipped in the NEG position; TTL compatible.

OUTPUTS

- **DATA** – Provides 13 binary TTL-compatible output lines and the data transfer commands required for MCA interface; rear panel 34-pin ribbon cable connector. Data lines are negative true. Two input lines are also provided for the Model 8233 Digital Stabilizer correction voltages. Stabilizer Control range; zero: ±3%, gain: ±0.7%.

- **LTC/PUR** – Accepts Reject and Live Time signals from CANBERRA amplifiers equipped with PUR/LTC. It also provides Linear Gate to those units for full interactive operation; rear panel 3-pin Molex connector for use with Model C1514 PUR/LTC interface cable.

  - **REJect** – Receives a positive true logic pulse used to initiate an ADC reject sequence; must occur during the ADC Linear Gate (LG) signal time; amplitude ≥ 2.5, 0 to 7 V maximum; width ≥100 ns; loading 1 kΩ to 0 V. Accessible through pin 2 of the rear panel LTC/PUR connector.

  - **LG** – Provides a negative true logic signal; logic low while the ADC acquires an input pulse, returns to a logic high at the pulse acquisition conclusion. TTL compatible output, 47 Ω series resistor. Accessible through pin 1 of the rear panel LTC/PUR connector.

FRONT PANEL CONTROLS

- **GAIN** – Six-position rotary switch to select full scale resolution of the input signal; selection of 256, 512, 1K, 2K, 4K or 8K channels for a 10 V input pulse or level.

- **RANGE** – Six-position rotary switch to select 256, 512, 1K, 2K, 4K or 8K channels as the upper output address limit.

- **OFFSET** – Six toggle switches to digitally offset the spectrum to the left; subtracts 0 to 8064 channels in binary multiples of 128 channels.

- **LLD** – Screwdriver-adjusted multi-turn potentiometer sets the Lower Level Discriminator for minimum input acceptance voltage; range 0 to +10 V dc. The input threshold tracks the LLD to 500 mV.

- **ULD** – Screwdriver-adjusted multi-turn potentiometer sets the Upper Level Discriminator for maximum input acceptance voltage; range 0 to +10.5 V dc.

- **ZERO** – Screwdriver-adjusted multi-turn potentiometer sets the input analog zero level; adjustment range ±3% of the ADC full scale range.

- **PEAK DETECT** – Toggle switch to select either AUTOmatic or DELAYED initiation of conversion cycle. In AUTOmatic mode, an internal peak detector operates on the input pulse. In DELAYED mode, the conversion begins after a user selectable delay, initiated by the input signal rising through the input threshold setting. An ADJustment potentiometer permits selection of a delay from 2 to 100 µs.

- **COINC/ANTI** – Toggle switch to select either the COINCidence or the ANTIcoincidence gating mode. In the COINCidence mode (ANTIcoincidence) a positive GATE pulse enables (disables) the conversion of the present input. If gating is used, the pulse must be present during the Linear Gate time.

- **PHA/SVA** – Toggle switch to select the Pulse Height Analysis or Sampled Voltage Analysis mode. In PHA, the conversion cycle is initiated by the INPUT pulse. In SVA, the conversion cycle is initiated by a GATE pulse. In either mode, the LLD and ULD acceptance criteria apply. The GATE pulse must be positive in COINC mode or inverted in ANTI mode.

INDICATORS

- **DEAD TIME** – 20 segment LED indicator displays the average dead time of the converter.

PERFORMANCE

- **INTEGRAL NONLINEARITY** – <±0.025% of full scale over the top 99.5% of selected range.

- **DIFFERENTIAL NONLINEARITY** – <±0.9% over the top 99.5% of range including effects from integral nonlinearity.

  NOTE: The upper 1/64 of the address range is not used.

- **GAIN DRIFT** – <±0.005% of full scale/°C.

- **ZERO DRIFT** – <±0.005% of full scale/°C.

- **LONG TERM DRIFT** – <±0.005% of full scale/24 hours at a constant temperature.

- **PEAK SHIFT** – <±0.025 of full scale at rates up to 100 kHz.

- **ADC DEAD TIME** – Linear Gate Time + 1.4 µs.

- **CHANNEL PROFILE** – Typically flat over 90% of channel width.

POWER REQUIREMENTS

+24 V dc – 115 mA	+12 V dc – 325 mA or
–24 V dc – 170 mA	+ 6 V dc – 600 mA

PHYSICAL

- **SIZE** – Standard single width NIM module 3.52 x 22.12 cm (1.35 x 8.71 in.) per DOE/ER-0457T.

- **NET WEIGHT** – 1.04 kg (2.3 lb).

- **SHIPPING WEIGHT** – 2.1 kg (4.6 lb).

ENVIRONMENTAL

- **OPERATING TEMPERATURE** – 0 to 40 °C.

- **OPERATING HUMIDITY** – 0-80% relative, non-condensing. Meets the environmental conditions specified by EN 61010, Installation Category I, Pollution Degree 2.

CABLES

- Cable not supplied; MCA must support 34-pin ADC Standard. Consult factory if required.

- PUR/LTC requires Model C1514 interface cable.