實習題目－4
液晶顯示之計頻器

溫進坤

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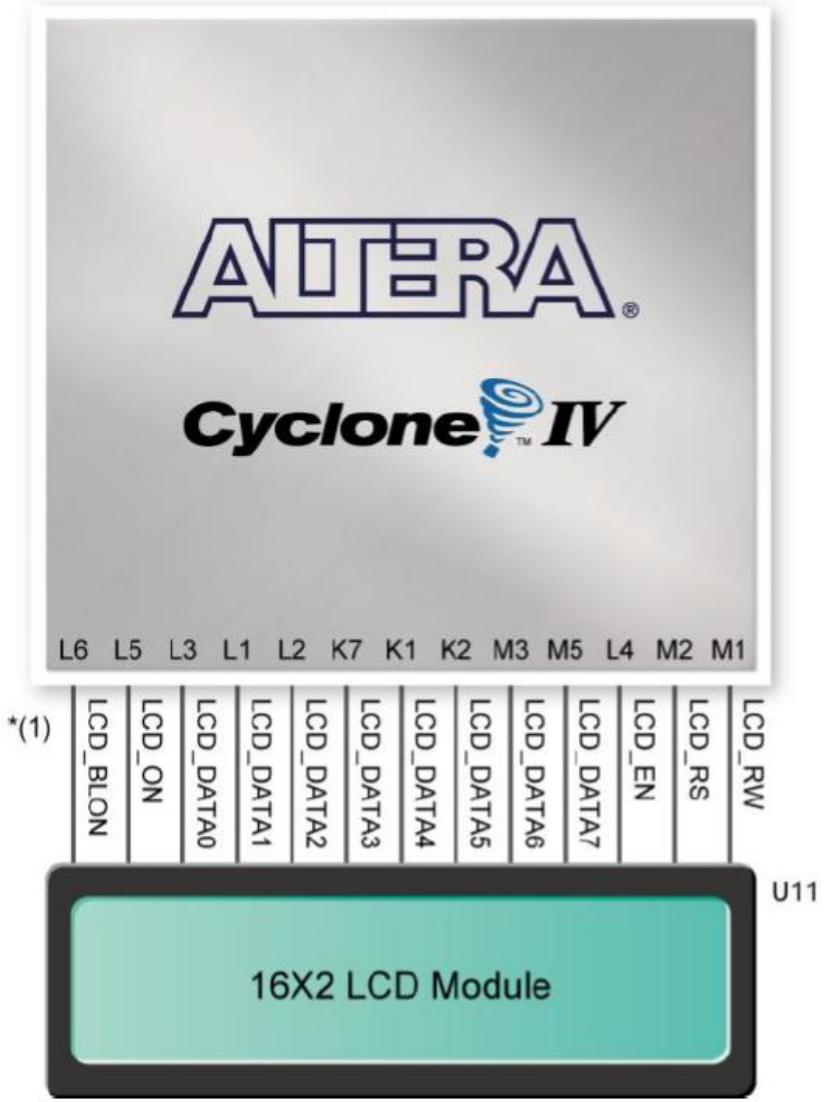
題目功能

1. 電源開機後在液晶顯示器上顯示為00000000Hz。
2. 將每秒計數後的頻率值，顯示在液晶顯示器上。
3. 使用同步式設計，always中不能使用CLOCK_50M或RESET以外的訊號當CLOCK使用。

LCM Connection



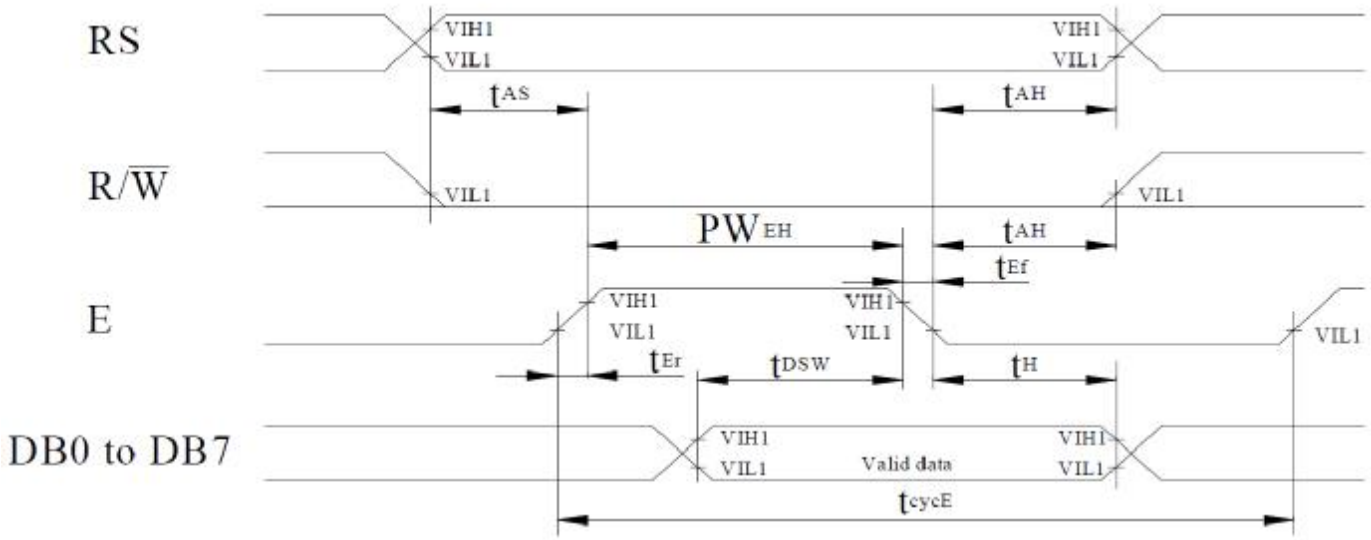
LCM Pin Define

Signal Name	*FPGA Pin No.*	*Description*	*I/O Standard*
LCD_DATA[7]	PIN_M5	LCD Data[7]	3.3V
LCD_DATA[6]	PIN_M3	LCD Data[6]	3.3V
LCD_DATA[5]	PIN_K2	LCD Data[5]	3.3V
LCD_DATA[4]	PIN_K1	LCD Data[4]	3.3V
LCD_DATA[3]	PIN_K7	LCD Data[3]	3.3V
LCD_DATA[2]	PIN_L2	LCD Data[2]	3.3V
LCD_DATA[1]	PIN_L1	LCD Data[1]	3.3V
LCD_DATA[0]	PIN_L3	LCD Data[0]	3.3V
LCD_EN	PIN_L4	LCD Enable	3.3V
LCD_RW	PIN_M1	LCD Read/Write Select, 0 = Write, 1 = Read	3.3V
LCD_RS	PIN_M2	LCD Command/Data Select, 0 = Command, 1 = Data	3.3V
LCD_ON	PIN_L5	LCD Power ON/OFF	3.3V
LCD_BLON	PIN_L6	LCD Back Light ON/OFF	3.3V

LCD_ON : Turn On LCM Power, 1: LCM power on, 0: LCM power off

LCD_BLON : Turn On LCM Backlight, 1:LCM backlight on, 0:LCM backlight off

LCM Control Timing



1:Data,0:Instruction

1:Read,0:Write

1:Enable

Item	Symbol	Min	Typ	Max	Unit
Enable cycle time	t_{cycE}	500	–	–	ns
Enable pulse width (high level)	PW_{EH}	230	–	–	ns
Enable rise/fall time	t_{rr},t_{rf}	–	–	20	ns
Address set-up time (RS, R/W to E)	t_{AS}	40	–	–	ns
Address hold time	t_{AH}	10	–	–	ns
Data set-up time	t_{DSW}	80	–	–	ns
Data hold time	t_{H}	10	–	–	ns

LCM Instruction Table

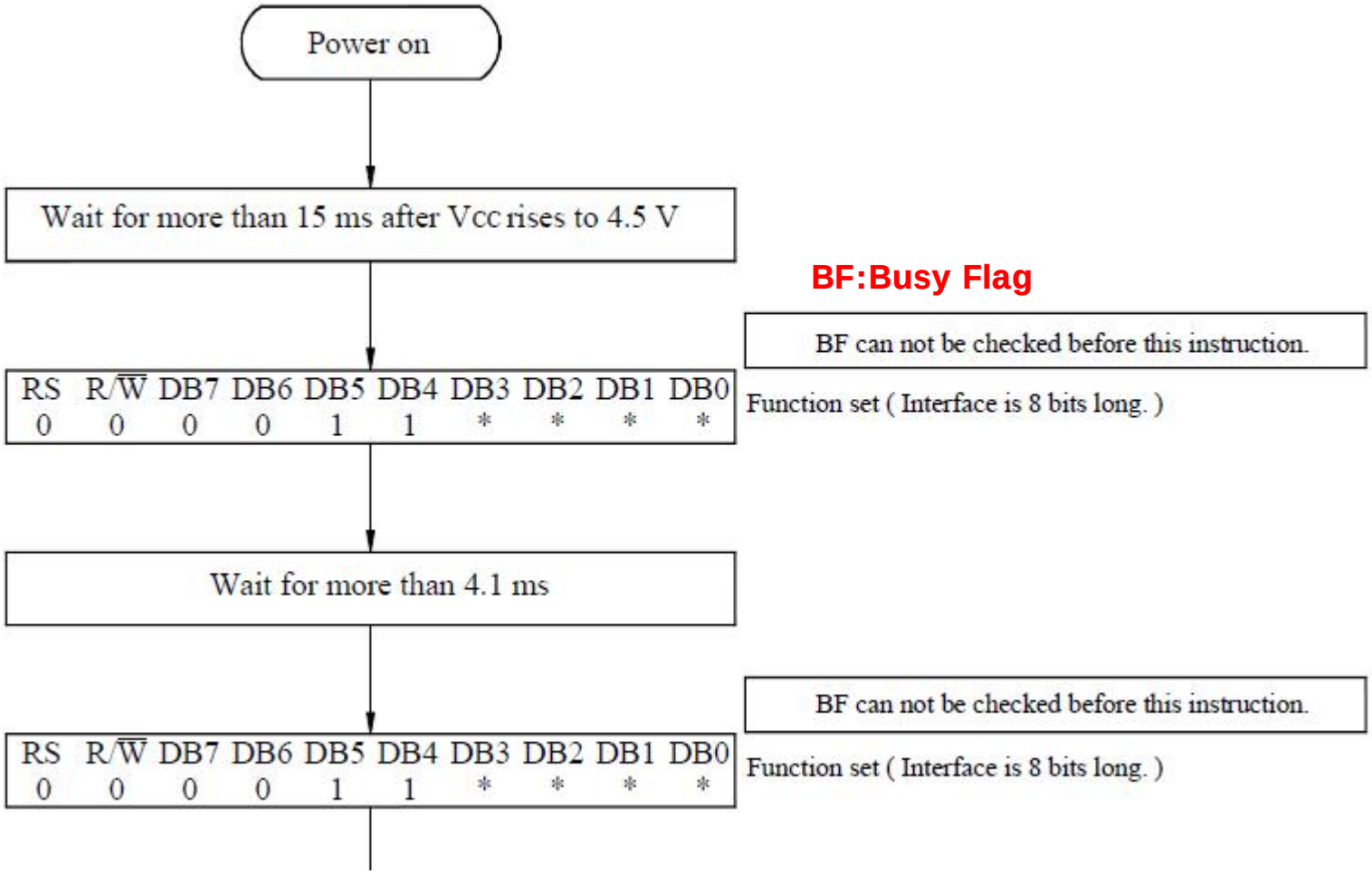
Instruction	Instruction Code										Description	Execution time (fosc=270Khz)
	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
Clear Display	0	0	0	0	0	0	0	0	0	1	Write "00H" to DDRAM and set DDRAM address to "00H" from AC	1.53ms
Return Home	0	0	0	0	0	0	0	0	1	—	Set DDRAM address to "00H" from AC and return cursor to its original position if shifted. The contents of DDRAM are not changed.	1.53ms
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	SH	Assign cursor moving direction and enable the shift of entire display.	39 μs
Display ON/OFF Control	0	0	0	0	0	0	1	D	C	B	Set display (D), cursor (C), and blinking of cursor (B) on/off control bit.	39 μs
Cursor or Display Shift	0	0	0	0	0	1	S/C	R/L	—	—	Set cursor moving and display shift control bit, and the direction, without changing of DDRAM data.	39 μs

I/D:1
SH:0

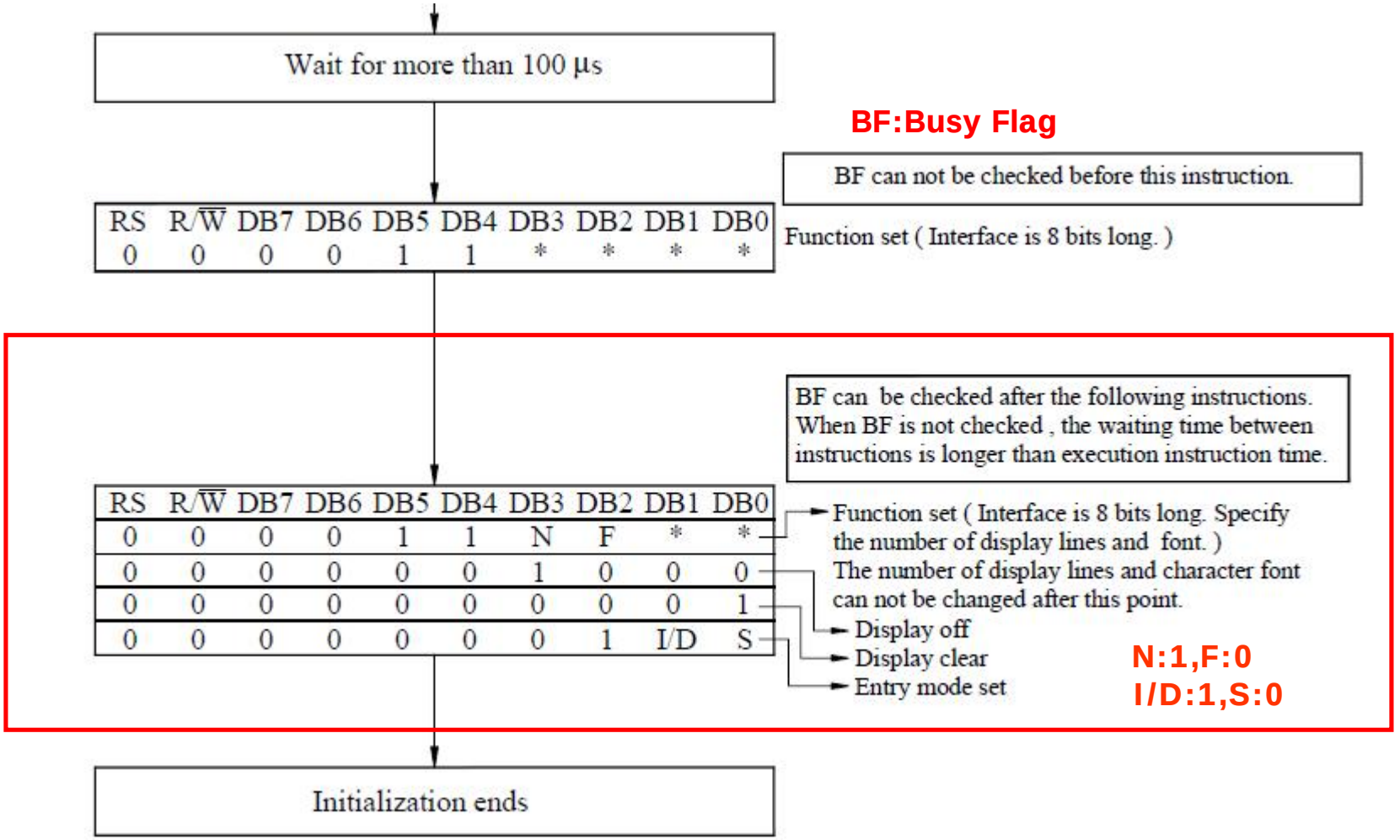
LCM Instruction Table..

Function Set	0	0	0	0	1	DL	N	F	—	—	Set interface data length (DL:8-bit/4-bit), numbers of display line (N:2-line/1-line)and, display font type (F:5× 11 dots/5× 8 dots)	39 μ s
Set CGRAM Address	0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0	Set CGRAM address in address counter.	39 μ s
Set DDRAM Address	0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Set DDRAM address in address counter.	39 μ s
Read Busy Flag and Address	0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Whether during internal operation or not can be known by reading BF. The contents of address counter can also be read.	0 μ s
Write Data to RAM	1	0	D7	D6	D5	D4	D3	D2	D1	D0	Write data into internal RAM (DDRAM/CGRAM).	43 μ s
Read Data from RAM	1	1	D7	D6	D5	D4	D3	D2	D1	D0	Read data from internal RAM (DDRAM/CGRAM).	43 μ s

LCM Initial Flow



LCM Initial Flow..



Test Frequency Input

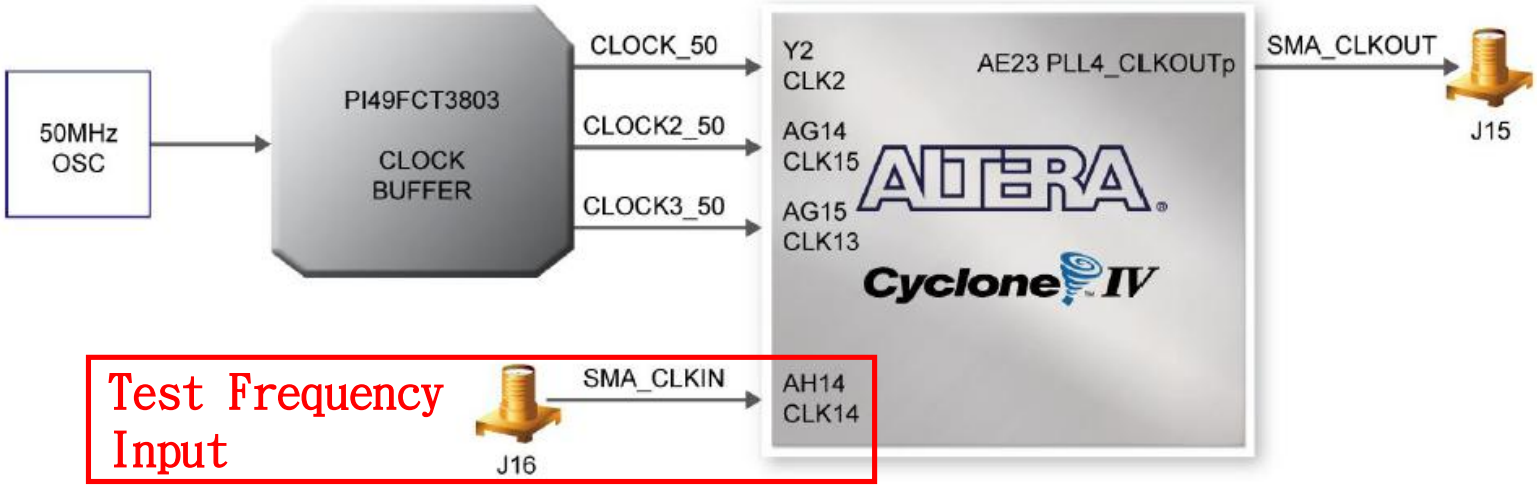
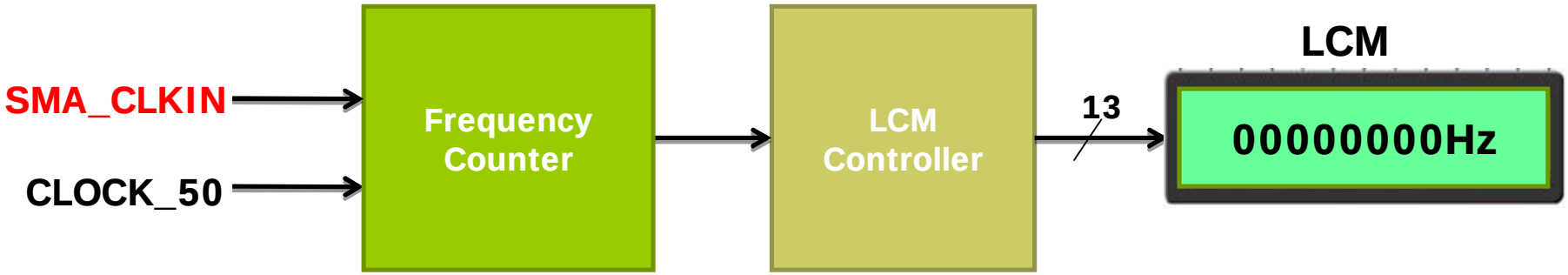


Figure 4-11 Block diagram of the clock distribution

Table 4-5 Pin Assignments for Clock Inputs

Signal Name	*FPGA Pin No.*	*Description*	*I/O Standard*
CLOCK_50	PIN_Y2	50 MHz clock input	3.3V
CLOCK2_50	PIN_AG14	50 MHz clock input	3.3V
CLOCK3_50	PIN_AG15	50 MHz clock input	Depending on JP6
SMA_CLKOUT	PIN_AE23	External (SMA) clock output	Depending on JP6
SMA_CLKIN	PIN_AH14	External (SMA) clock input	3.3V

系統方塊圖


SMA_CLKIN
CLOCK_50
Frequency Counter
LCM Controller
13
LCM
00000000Hz

計分方式

1. 程式完成後請助教確認功能是否正確，並給予完成順序號。
2. 將全部的Verilog程式壓縮後上傳至Moodle[繳交作業]，並在檔名依序寫上實習題目號碼、完成順序號、學號。(檔名:Lab_4_No_xx_學號.zip)
3. 計分標準依完成順序及程式內容給分，若發現程式有互相抄襲狀況，該員分數皆為0分。

參考資料

- **DE2-115_mb_schematic.pdf**
- **DE2_115_pin_assignments.csv**
- **CFAH1602BTMCJP.pdf**