Dust Networks

Eterna LTP5901 / LTP5902
Integration Guide

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About This Guide

This document provides the design guidelines essential for incorporating either an Eterna LTP5901 or LTP5902 module. The document covers design, layout, EMI, and some manufacturing considerations.

Audience

This document is intended for system developers, hardware designers, and layout engineers.

Related Documents

The following related documents are available:

040-0110 Eterna Board Serial Programmer Guide

Conventions and Terminology

This guide uses the following text conventions:

- `Computer type` indicates information that you enter, such as a URL.
- **Bold type** indicates buttons, fields, and menu commands.
- *Italic type* is used to introduce a new term.
- **Note:** Notes provide more detailed information about concepts.
- **Caution:** Cautions advise about actions that might result in loss of data.
- **Warning:** Warnings advise about actions that might cause physical harm to the hardware or your person.

Revision History

Revision	Date	Description
040-0119 rev 1	6/7/2012	Initial version
040-0119 rev 2	7/18/2012	Updated references

1 Design Guidelines

Schematic Design

The LTP5901 and LTP5902 require little external circuitry, as the devices references, decoupling and power supply filtering are integrated. The LTP5901 and LTP5902 will be modularly certified for operation in the United States (FCC), Canada (IC) and the European Union (CE). If further certifications may be necessary, it is essential to provide a method to deliver specific radio test APIs via the API UART interface during testing. Test connections should be included in the schematic if the product does not provide a natural means of delivering the API calls.

During the design phase, it is recommended to include a header to allow for updating of Eterna's software.

The schematic shown in Figure 1 includes the signal connections necessary for the programming header. The part number for the header is provided in Table 1.

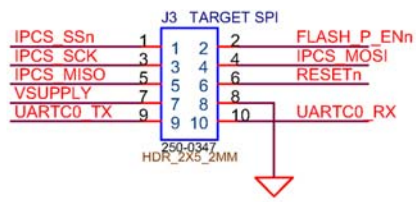

Figure 1 Eterna Example Schematic

Table 1 Programming Header

Reference	Value	Vendor	Vendor P/N
J3	5x2 header	Molex	87831-1020

PCB Layout

Eterna-based designs should adhere to the following layout-sensitive guidelines:

1. The Eterna modules include exposed test points, and pads on the bottom (mounting) side of the PCB. Exposed metal should be avoided in the on the top surface of the mating PCB in the area where the module will be mounted.
2. The LTP5901 includes a chip antenna with layout designed to work over 1 mm thick FR4, as used in the LTP5902. It is recommended to maintain an opening free of FR4 and any conductive material as far as practically possible to maximize the radio performance.
3. The LTP5902 includes a through hole mounted MMCX connector. A sufficient opening in the mating PCB must be provided – see the LTP5902 recommended land pattern later in this document for details.
4. Eterna's radios can be sensitive to EMI generated by DC/DC converters. It is recommended that such inductors are placed a minimum of 2 inches from the radio

and antenna or MMCX connector. If space constraints prevent this degree of separation, inductor selection can reduce the EMI generated. Different core materials and shapes will change the size/ current and price/current relationship of an inductor. Toroid or shielded pot cores in ferrite or permalloy materials are small and don’t radiate much energy but generally cost more than powdered iron core inductors with similar electrical characteristics.

Eterna LTP5901 Recommended Land Pattern (Chip Antenna)

Two common practices for defining land patterns are Non Solder Mask Defined, NSMD, and Solder Mask Defined, SMD. Given the lead pitch of the LTP5901 and that tolerances for metal etch are commonly more precise than solder mask deposition, it is recommended to use NSMD land patterns. The solder mask opening should provide sufficient margin for registration tolerance to avoid solder mask infringing on the pad, typically 60 to 75 um from the edge of the pad and the solder mask.

Land Pattern dimensions are illustrated in Figure 2.

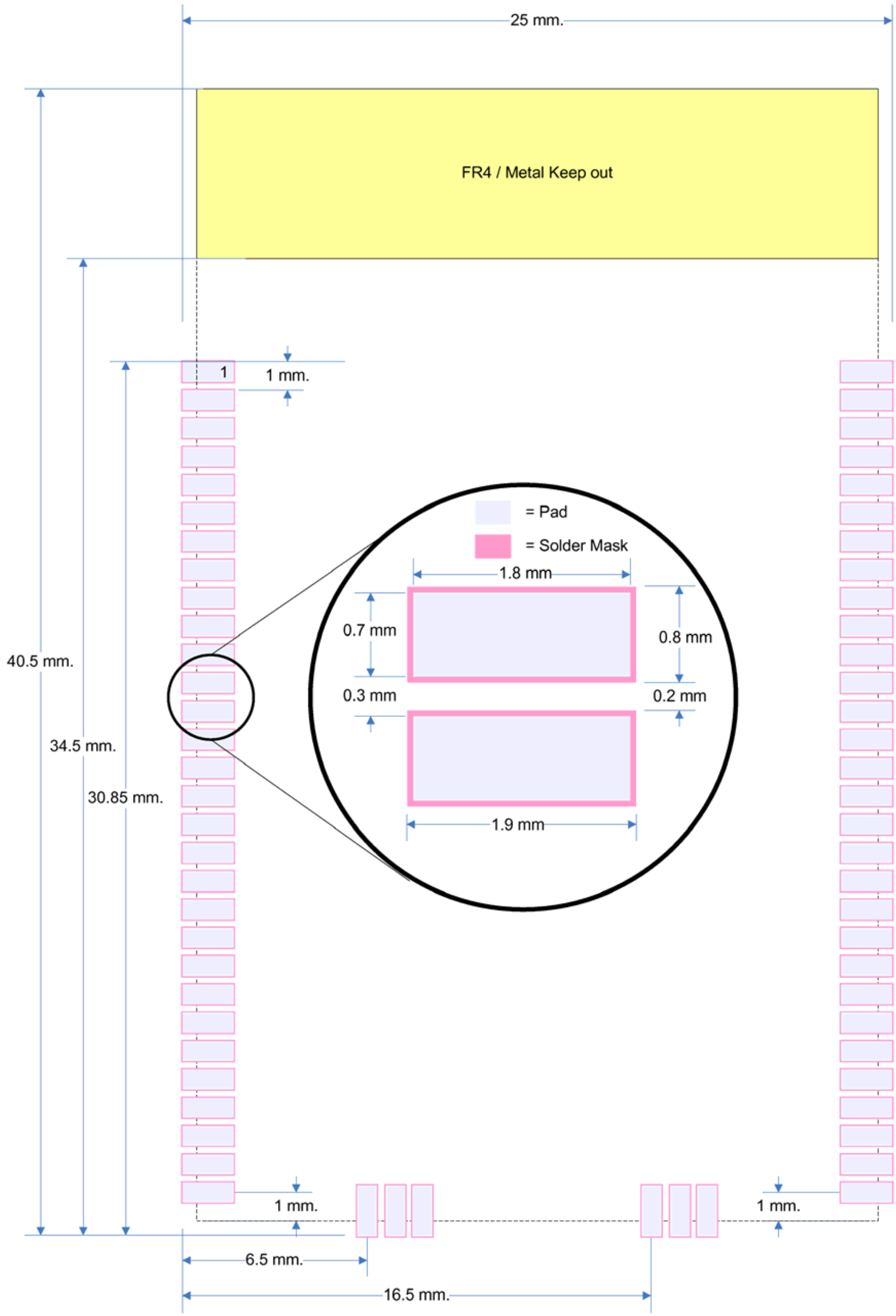

Figure 2 LTP5901 Land Pattern (Chip Antenna)

Eterna LTP5902 Recommended Land Pattern (MMCX)

Two common practices for defining land patterns are Non Solder Mask Defined, NSMD, and Solder Mask Defined, SMD. Given the lead pitch of the LTP5902 and that tolerances for metal etch are commonly more precise than solder mask deposition, it is recommended to use NSMD land patterns. The solder mask opening should provide sufficient margin for registration tolerance to avoid solder mask infringing on the pad, typically 60 to 75 um from the edge of the pad and the solder mask.

Land Pattern dimensions are illustrated in Figure 3.

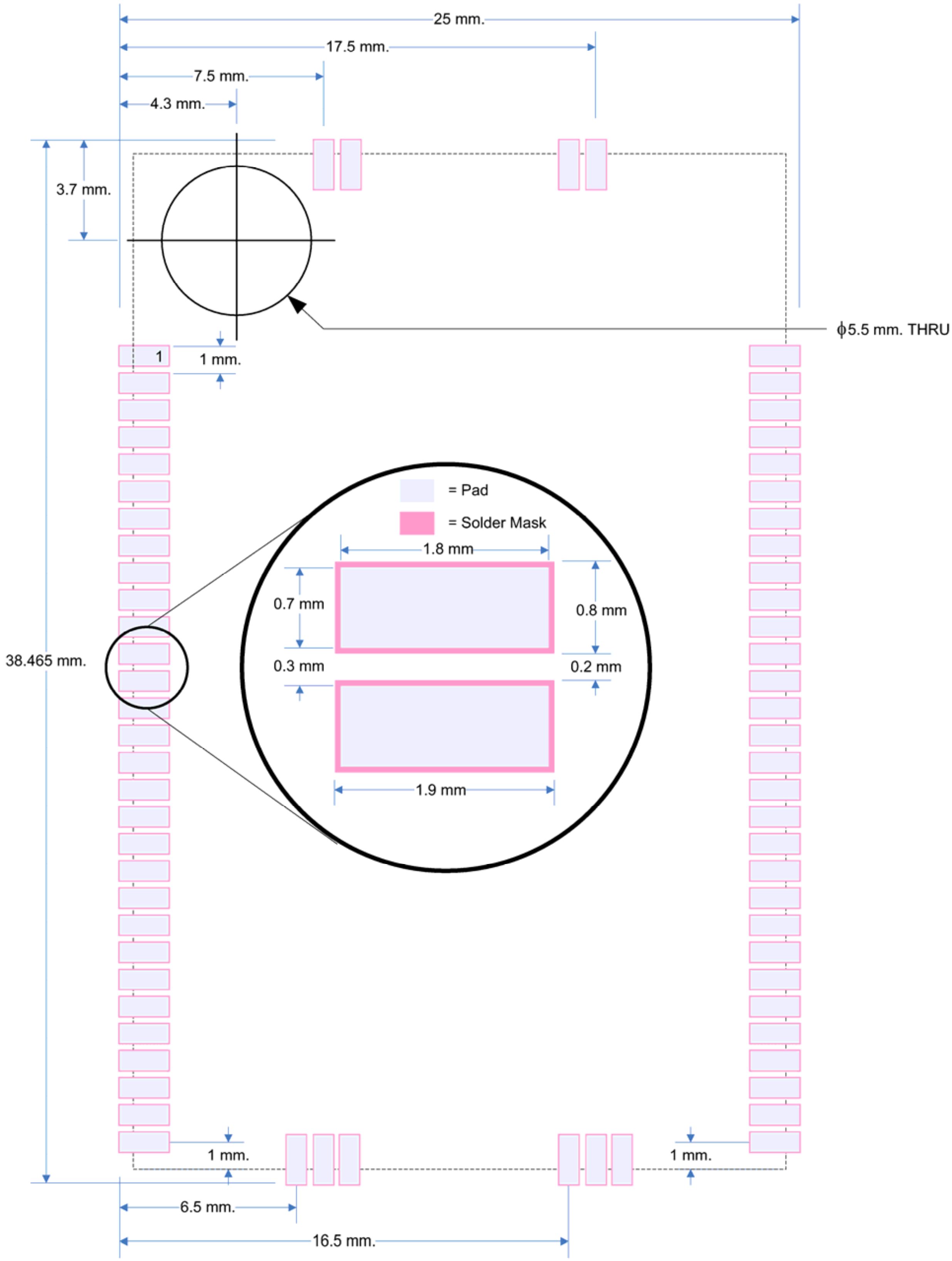

Figure 3 LTP5902 Land Pattern (MMCX)

Antenna ESD Considerations

The antenna pin is a particularly sensitive node for electro-static discharge (ESD) since it must detect small, high-frequency signals. ESD damage may result in decreased receive or transmit performance, or other system failure. Many applications for Eterna have an exposed antenna that provides an entry point for ESD events. Proper consideration of antenna design as well as antenna protection can substantially improve ESD robustness in harsh environments.

A radome (protective covering) made of highly resistive material may be used to prevent direct contact with the antenna and/or dissipate charge. To avoid ESD events caused by triboelectric charging generated by wind passing over the antenna in dry climates, the radome design should consider bulk and surface resistivity as well as the size of the gap between the antenna metal and the interior of the radome.

In general, DC-grounded antennas (the antenna and ground have a DC short) provide superior protection to ESD events. DC-grounded antennas are highly recommended in harsh environments. Additionally, a DC path-to-earth ground should be provided whenever possible to help bleed off accumulated charge from the antenna as well as leak charge from the radome.

While these general guidelines should improve robustness to ESD events, individual implementations may have unique factors that complicate ESD protection.

Supply Design

Due to the heavy duty cycling, Eterna's current consumption can change substantially over a short period. This does not represent an issue for systems with supplies having low source impedance (less than 5 Ohms). Regulated supplies, however, may have difficulty in the sudden changes in current consumption (more than an order of magnitude in less than 1 µs), resulting in transient voltages on the supply co-incident with the higher current consumption of the radio operation. To ensure proper operation of the radio, a supply should be able to ramp from 250 µA to 10 mA in less than 1 µs without generating a transient greater than 200 mV. For systems with regulated supplies, consultation with Linear Technology is strongly recommended.

Eterna can be configured to support current limited supplies. Contact Linear Technology for details.

Voltage Supervision and Reset

Eterna includes a power-on reset to safely set its own state during power up, and includes a brown-out circuit that immediately halts flash erase cycles and interrupts flash write cycles at the next 32-bit boundary, generating an interrupt to the CPU and maintaining state for the CPU to correct should the power supply return to normal operating levels. In the interest in avoiding flash corruption, it is **not** considered best practice to connect the RESETn lead to a voltage supervisor or to asynchronously assert RESETn without previously suspending network and flash activity.

2 Manufacturing Guidelines

Reflow

Given that Eterna modules are assembled using TBD solder compound, careful adherence to J-STD-020 to avoid reflowing the modules during the assembly process is necessary. The solder joint quality of the "castellations" where they contact the mating PCB should meet IPC-A-610 Acceptability of Electronic Assemblies, section 8.2.4 Castellated Terminations.

Solder Paste / Cleaning

"No Clean" soldering paste is strongly recommended, as it does not require cleaning following the soldering process. Cleaning the populated modules is strongly discouraged due to the potential issues that may result. Residuals under the module are difficult to remove with any cleaning process. Cleaning with water can lead to capillary effects where water is absorbed into the gap between the host board and the module, potentially resulting in combination with soldering flux residuals leading to short circuits between neighboring pads. Cleaning with alcohol or a similar organic solvent will likely flood soldering flux residuals under the shield, which is not accessible for post-washing inspection. Ultrasonic cleaning could damage the module permanently.

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