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The BBN TIP: Hardware Manual

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1. OVERVIEW

1.1 Summary

The BBN Terminal Interface Message Processor (TIP) provides a means for connecting up to 63* terminal devices to the ARPA Network. The terminal interface specification conforms to the EIA standard RS232C, which permits direct connection to most data modems. In addition to full duplex, serial data transmission, each of the 64 ports provides 4 program-settable control lines and monitors 6 external status lines; these lines are useful in dealing with modems or other compatible I/O devices. Data format is Teletype compatible, that is, character oriented with start and stop bits. The TIP handles all routine operations of timing and sequencing. All line parameters, such as speed and character size, are program settable.

1.2 General Design Description

The BBN TIP is composed of a 316 Interface Message Processor (IMP) and a BBN Multi-Line Controller (MLC). The MLC occupies channels 14, 15 and 16 on the H316 High-Speed DMC (HSDMC). On an IMP, channel 14 normally accommodates the receive half of a second Host interface, and channels 15 and 16 are normally spare. A TIP, however, normally has only two 50 Kb modems and either no Host or one Host interface; consequently, there should be no conflict with the performance of its IMP functions insofar as hardware

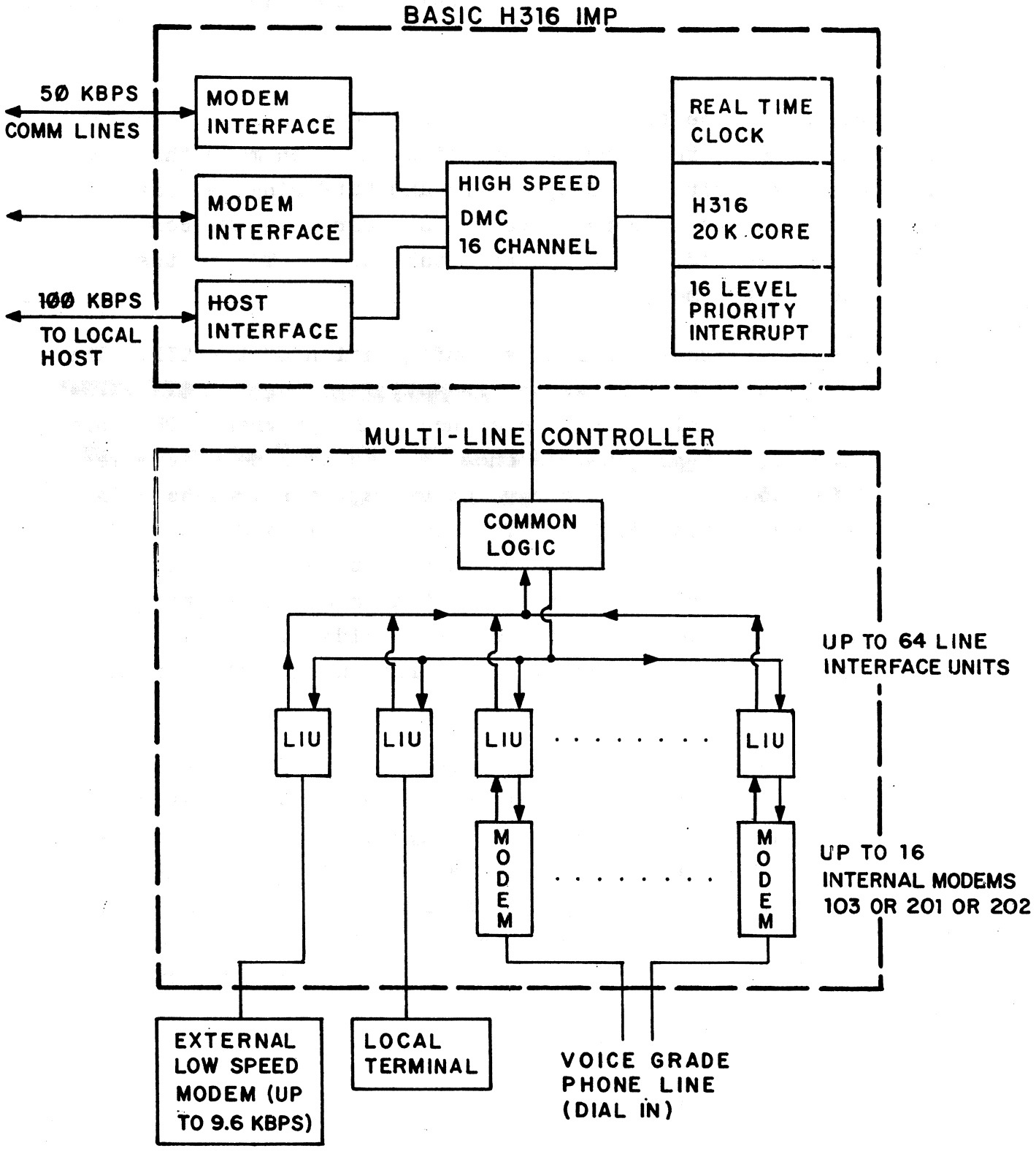
*There are 64 hardware lines but line Ø is logically reserved by the program for special use.

is concerned. At the same time, the added computational requirements brought on by the terminal-handling function mean that, to accommodate the additional programming and buffering, an extra eight thousand words of core above the standard 316 IMP configuration are needed, bringing the total for the TIP to twenty thousand words of memory.

Figure 1-1 shows the hardware configuration of the TIP. The upper part of the figure shows the essentially standard 316 IMP contained in a TIP which runs the standard IMP program. This program includes a test for the presence of a Multi-Line Controller. If an MLC is attached, the program activates a terminal-handling program which controls the MLC. The standard IMP and its associated software are described in BBN Report 1877 and will not be dealt with further here. This report does not describe the TIP software in any detail; software is considered on only the most fundamental level necessary to understand the interaction between program and hardware.

The lower portion of Figure 1-1 shows the BBN Multi-Line Controller. The MLC provides interfaces for up to sixty-four full duplex connections. These lines may be clocked either externally to the TIP, in which case they are called *synchronous* in TIP parlance, or internally by the TIP, called *asynchronous*. Any of these connections or *ports* (as they will be referred to hereafter) may transmit and receive up to 19.2 Kbps when operating externally clocked. The bit rates for the internal clocks range from 75 baud to 2400 baud and are shown in Table 1-1.

All of the circuitry specific to a single port is contained on a plug-in module called a Line Interface Unit or LIU. Although the input and the output for a given port are usually assigned



BBN TIP HARDWARE CONFIGURATION
FIGURE 1-1

	RATES
Ø	ILLEGAL
1	75
2	110
3	134
4	150
5	300
6	600
7	1200
10	1800
11	2400
12	4800 (OUTPUT ONLY)
13	9600 (OUTPUT ONLY)
14	19200 (OUTPUT ONLY)
15	ILLEGAL
16	ILLEGAL
17	SYNCHRONOUS

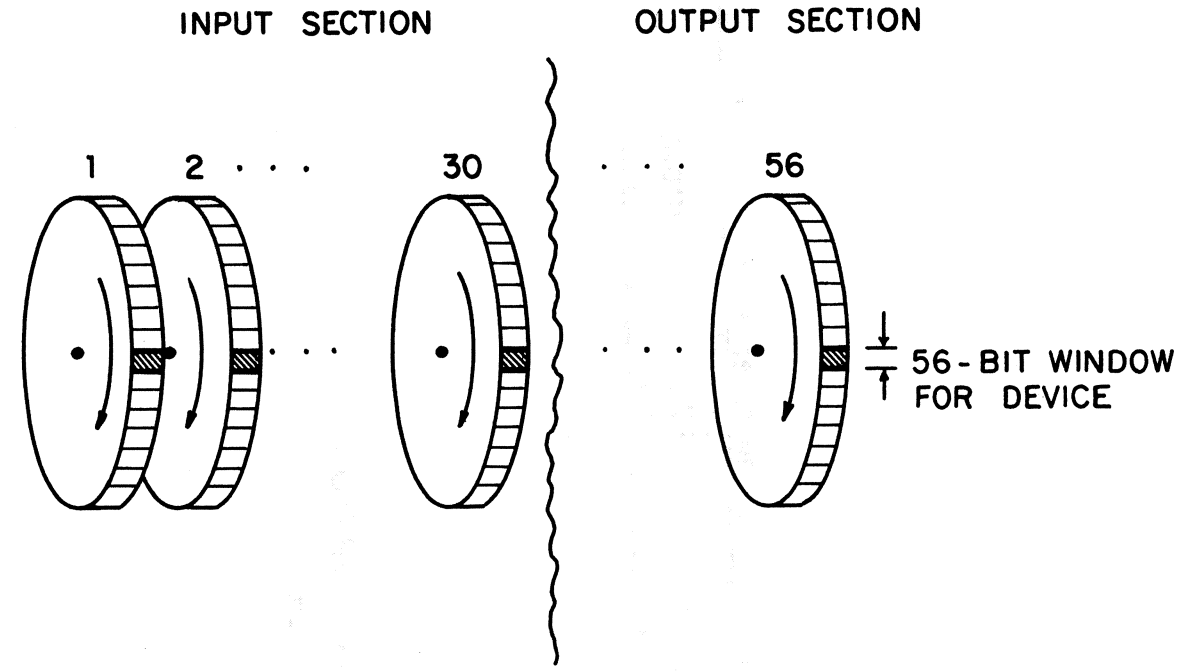
MLC CLOCK RATES

Table 1-1

to the same device, they may go to completely separate devices such as a card reader and a line printer. All such parameters as bit rate and character size are individually settable under program control for each port and are independent for the input and the output of a given port.

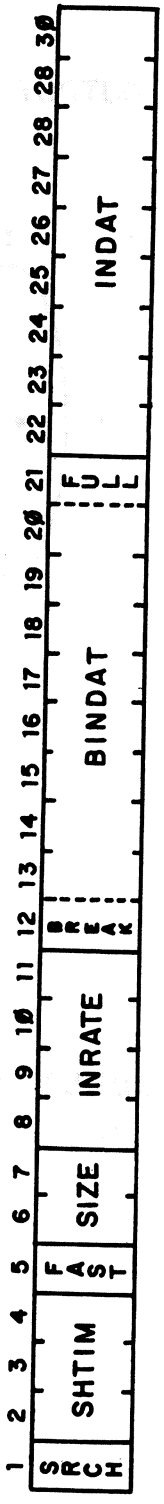
In addition to circuitry on the LIU, each port uses logic which is shared by all lines. This is called the common logic. The common logic contains the DMC interfaces, the timing circuitry, and a 74-bit by 64-word memory. Each of the 64 device ports is assigned a unique memory location called the STATEWORD for that line. The STATEWORD records the instantaneous state of data and control transmission on a line. Part of the memory is realized as a serial, pseudo-drum memory built from circulating shift registers. This 56-bit portion is shown schematically in Figure 1-2. The remaining 18 bits of the STATEWORD are stored on a per-line basis on the individual LIUs. The pseudo-drum rotates once per 51.2 μsec which permits a complete revolution per bit at 19.2 kilobits per second. Thus the MLC handles one bit per revolution at 19.2 Kbps, one bit per 2 revolutions at 9.6 Kbps and so forth.

Figure 1-3 shows the bit assignment for the input portion of the STATEWORD. The TIP program must set the input rate, character size, and fast bit to the proper value. The fast bit indicates a high speed line, which is given priority on input. Initially the Input Data Shifter, INDAT, is preset to all "1s". Input data is shifted into the proper entry position of INDAT, start bit first, followed by Least Significant data bit and so on. When the start bit, which is logically a "Ø", is detected entering



STATEWORD PSEUDODRUM MEMORY

FIGURE 1-2



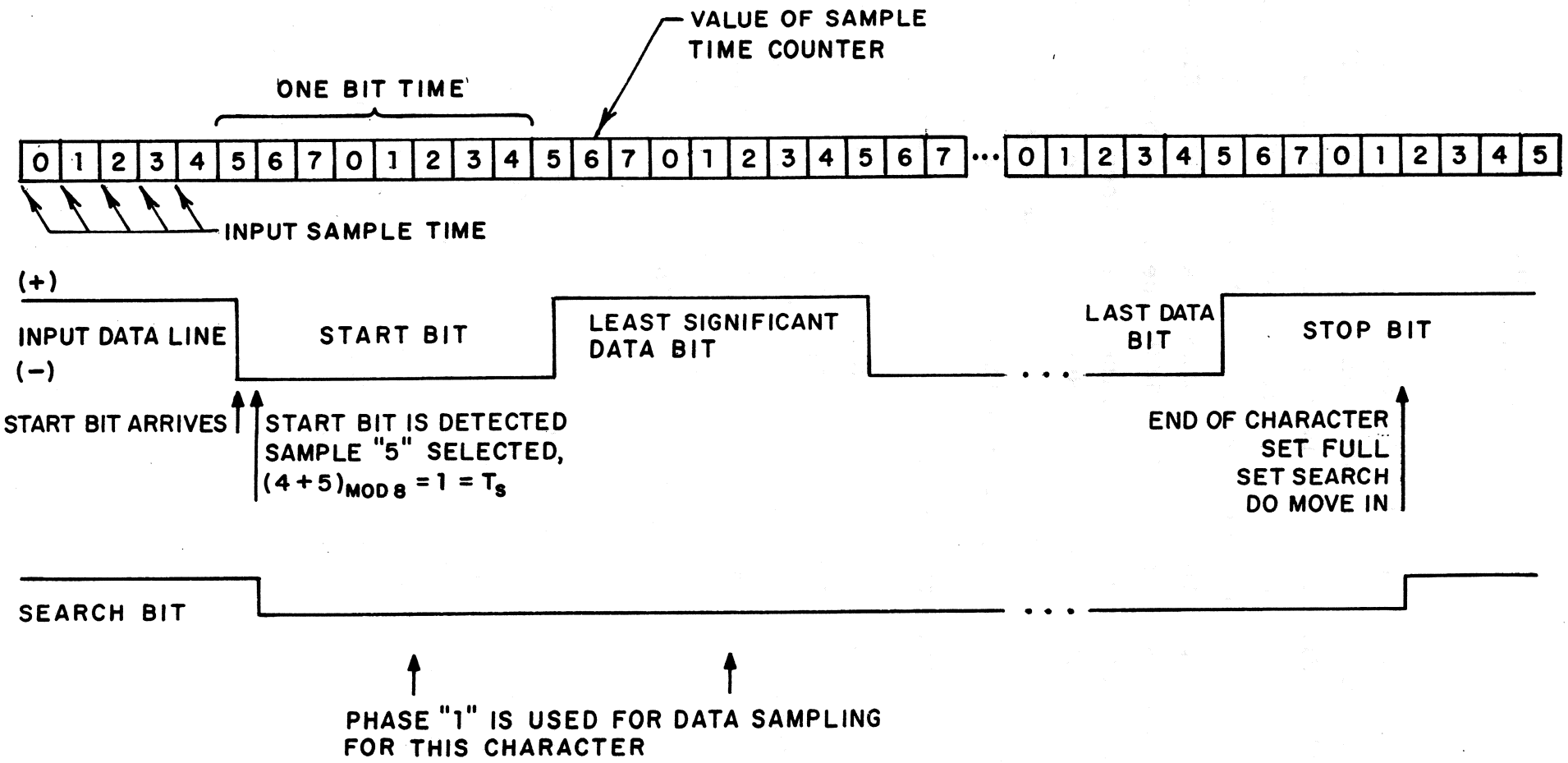
STATEWORD INPUT PORTION
FIGURE 1-3

the LSB (Least Significant Bit) of INDAT, this indicates that an entire character has been shifted in and the contents of INDAT are transferred to BINDAT (Input Data Buffer) and FULL is set. FULL indicates a character which is ready for input to memory. The contents of BINDAT are appended to the line number of this STATEWORD and are input to the 316 memory via the DMC. Simultaneously with the setting of FULL, SRCH (the Search bit) is set to "1". Whenever SRCH is a "1" the line is examined for a start bit. When a start bit is detected, SRCH is reset to "Ø" and a bit sampling time is computed and stored in SHTIM, the sample time field. Sample time (T_s) is computed as follows.

$$T_s = (\text{Time of detecting start bit} + 4 \text{ units}) \bmod 8$$

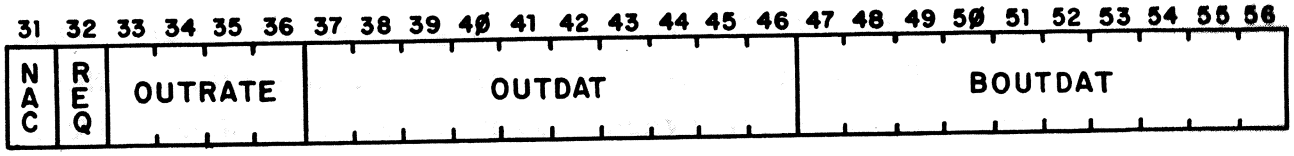
where a unit is 1/8 of a bit time at the selected rate. Figure 1-4 shows how T_s is selected. This sample time is used only during one character; i.e., it is recomputed for each new character that arrives. At the time when a character is transferred from INDAT to BINDAT, the input line is sampled once again and this value is placed in the BREAK bit. If the line is broken, this bit will be a one.

The bit assignment for part of the output is shown in Figure 1-5. Data are loaded from the DMC into BOUTDAT (Output Data Buffer). When OUTDAT (Output Data Shifter) is empty, the contents of BOUTDAT are moved to OUTDAT and bits are shifted out at the rate determined by OUTRATE. When a character is moved from BOUTDAT to OUTDAT, the NAC (Need a Character) bit is set and REQ (Referred Request for Character) may be set. If the MLC is unable immediately to report a request for the next character because the DMC channel is busy, REQ is set. When the DMC becomes available it puts in a request from any line whose REQ bit is set, and



SELECTION OF DATA SAMPLING TIME

FIGURE 1-4



STATEWORD OUTPUT PORTION
FIGURE 1-5

clears that REQ bit. This process is crucial to an understanding of character output. It is described in detail in the "Output" portion of Section 1.4, on p. 24. Note that the handling of output characters and the reporting of requests are handled by independent DMC channels.

A portion of the circuitry for each line is not contained in the central control logic. This external circuitry is located on the Line Interface Unit. The LIU contains circuits which generate signals which may not be time multiplexed, i.e., turned on and off as the pseudo-drum rotates. Such signals are the output data line and modem control lines. The LIU contains a portion of the STATEWORD with bits assigned as in Figure 1-6. OUTFLOP and SOUTFLOP are the output data synchronizers. NAB and SNAB are the output clock synchronizers. MODEM CONTROL OUT provides control signals for an I/O device or an optional modem. SIF is the input data synchronizer and GAB and SGAB are the input clock synchronizers. XPCH may be set by program control to cross-patch a line. MODEM STATUS IN permits the program to read in 6 bits of status from the I/O device or the modem.

1.3 MLC Communications

1.3.1 On the Terminal Side

The format for all data which will be used as input for a given port of the MLC must be either five, six, seven or eight-bit characters. Each character must also be preceded by a start bit and followed by a stop bit. Details of this format, specifying voltage levels of the start and stop bits and of the logic ones and zeros, are treated in Appendix A. Essentially, characters must be compatible with standard Teletype format. The