

Compiler for P3: A Language to Specify Protocol-Independent Packet Parsers (*Draft*)

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1 Introduction

This document presents a domain-specific language P3 for reconfigurable Protocol-independent Packet Parsers.

For the requirement to facilitate the implementation of a high-security network, we design the language from the perspective of high trustworthiness, including the formal definition of type system and operational semantics of the language and its trusted compiler architecture. Based on the full understanding of the basic requirements of the reconfigurable hardware, from the view of hardware-software co-design, we finally defined the core characteristics of P3 language and its trusted compiler architecture called P3C. As the reconfigurable packet parser is an important part of SDN and programmable data plane, implementing the trusted compiler architecture of P3C will be of great significance to the security of SDN.

To build trustworthy compilers, one approach is to specify the source, target, intermediate languages, and the compilation algorithms formally in an interactive proof assistant such as Coq [1, 2], and then mechanically prove a semantic preserving relation between the source and target. CompCert [7, 6, 4], a formally verified compiler from a large subset of C language Clight [3] to assembly code for several machines, is one of the most successful efforts in this way. The proof can be mechanically checked, yielding the highest level of assurance we can hope to achieve[9].

Translation validation [13] is another approach to certify compilers. There have been many efforts in using the translation validation approach for synchronous languages such as Signal [13, 12, 11, 10]. This approach is also used to verify the translation from Simulink to C [14].

Fig.1 shows the architecture of the P3C compiler. In the project 2017ZX01030-301-003, we are required to implement the P3C compiler. However, our research include the verification of the compiler. Referring to the dotted lines in Fig.1, the design of the compiler concerned the verification on the *parsing*, the *type*

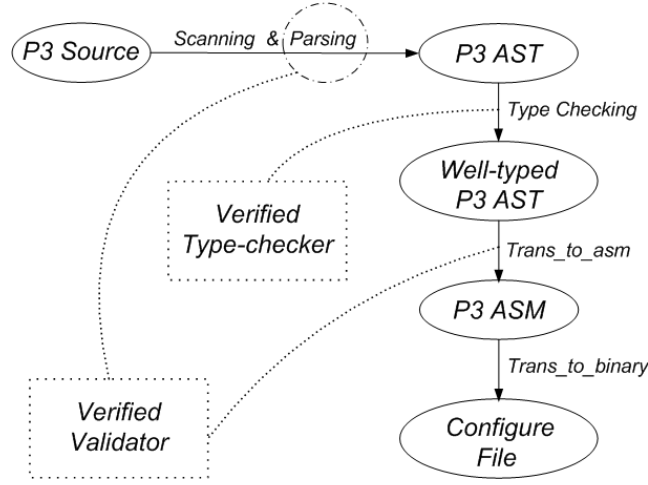


Figure 1: The compiler architecture of P3C

checking and the translation from the P3 abstract syntax tree (*AST*) to the P3 assembly (*ASM*).

The rest of the document is organized as follows. In Section 2, we give the syntax of P3, and the informal interpretation of a P3 specification by examples. In Section 3, we present the syntax of a special P3 assembly language, and the format of a target configuration file. In Section 4, the definition of the P3 AST, and the implementation and verification of the parsing, in the P3C compiler, are described. The definition of type system for P3 AST and the type checking in the P3C compiler are presented in Section 5. In Section 6, we specify the abstract syntax of the P3 assembly, and describe the translation from the P3 AST to the P3 assembly and the translation from the P3 assembly to the configuration file. In Section 7, we define the operational semantics of the P3 AST, the operational semantics of the P3 assembly, and then discuss the verification of the translation from the P3 AST to the P3 assembly. The document is concluded in Section 8.

2 The source language : P3

2.1 Syntax of P3

$\langle \text{parser_spec} \rangle ::= \langle \text{parameters} \rangle \{ \langle \text{decl} \rangle \}$

$\langle \text{parameters} \rangle ::= \langle \text{layer_reg_len} \rangle \langle \text{cell_reg_len} \rangle \langle \text{protocol_set} \rangle \langle \text{layer_set} \rangle$

$\langle \text{layer_reg_len} \rangle ::= \text{lreglen} \text{ '}' \text{ Integer bytes '}'$

$\langle \text{cell_reg_len} \rangle ::= \text{creglen} \text{ '}' \text{ Integer bytes '}'$

$\langle \text{protocol_set} \rangle ::= \text{pset '}' \{ \langle \text{id_list} \rangle \} \text{' ;'}$
 $\langle \text{layer_set} \rangle ::= \text{lset '}' \{ \langle \text{id_list} \rangle \} \text{' ;'}$
 $\langle \text{id_list} \rangle ::= \text{IDENT } \{ \text{' ;' IDENT } \}$
 $\langle \text{decl} \rangle ::= \begin{array}{l} \langle \text{const_decl} \rangle \\ | \langle \text{reg_acc_set} \rangle \\ | \langle \text{protocol_decl} \rangle \\ | \langle \text{layer_action} \rangle \end{array}$
 $\langle \text{const_decl} \rangle ::= \text{const IDENT '=' } \langle \text{expr} \rangle \text{' ;' // } \langle \text{expr} \rangle \text{ must be a constant expression}$
 $\langle \text{const} \rangle ::= \begin{array}{ll} \text{IDENT} & // \text{ constant identifiers} \\ | \text{Integer} & // \text{ integer constants, signed 32 bits} \\ | \text{Hexadecimal} & // \text{ hex constants, such as 0x88a8, 0xFFFFFFFF, 0x89, 0x103} \\ | \text{Bits} & // \text{ binary constants, such as 001001, 100, 0, 1, 1100, 00, 11111} \end{array}$
 $\langle \text{protocol_decl} \rangle ::= \text{protocol } \langle \text{protocol_id} \rangle \text{' } \{ \langle \text{protocol} \rangle \}$
 $\langle \text{protocol_id} \rangle ::= \text{IDENT}$
 $\langle \text{protocol} \rangle ::= \langle \text{fields} \rangle \langle \text{p_stmts} \rangle$
 $\langle \text{fields} \rangle ::= \text{fields '}' \{ \langle \text{field} \rangle \{ \langle \text{field} \rangle \} [\langle \text{option_field} \rangle] \}$
 $\langle \text{field} \rangle ::= \text{IDENT ':' } \langle \text{const} \rangle \text{' ;'}$
 $\langle \text{option_field} \rangle ::= \text{options ':' } \{ \langle \text{option_field} \rangle \}$
 $\langle \text{p_stmts} \rangle ::= \{ \langle \text{p_stmt} \rangle \}$
 $\langle \text{p_stmt} \rangle ::= \begin{array}{l} \langle \text{if_else_p_stmt} \rangle \\ | \text{next_header '=' } \langle \text{protocol_id} \rangle \text{' ;' } \\ | \text{length '=' } \langle \text{const} \rangle \text{' ;' } \\ | \text{bypass '=' } \langle \text{const} \rangle \text{' ;' } \\ | \langle \text{action_stmt} \rangle \end{array}$
 $\langle \text{if_else_p_stmt} \rangle ::= \text{if '}' (\langle \text{expr} \rangle \text{' ' } \langle \text{p_stmts} \rangle \{ \text{elseif '}' (} \langle \text{expr} \rangle \text{' ' } \langle \text{p_stmts} \rangle \{ } \\ [\text{else } \langle \text{p_stmts} \rangle] \text{endif}$
 $\langle \text{layer_action} \rangle ::= \langle \text{layer_id} \rangle \text{' } \{ \langle \text{local_reg_decl} \rangle \langle \text{l_decls} \rangle \langle \text{l_actions} \rangle \}$
 $\langle \text{layer_id} \rangle ::= \text{IDENT}$
 $\langle \text{l_decls} \rangle ::= \{ \langle \text{l_decl} \rangle \}$
 $\langle \text{l_decl} \rangle ::= \langle \text{protocol_id} \rangle \langle \text{id_list} \rangle \text{' ;'}$

```

⟨local_reg_decl⟩ ::= [ ⟨cella_regs⟩ ] [ ⟨cellb0_regs⟩ ] [ ⟨cellb1_regs⟩ ]

⟨cella_regs⟩ ::= ARegisters '{' { ⟨reg_acc_set⟩ } '}'

⟨cellb0_regs⟩ ::= B0Registers '{' { ⟨reg_acc_set⟩ } '}'

⟨cellb1_regs⟩ ::= B1Registers '{' { ⟨reg_acc_set⟩ } '}'

⟨l_actions⟩ ::= [ ⟨cella_actions⟩ ] [ ⟨cellb0_actions⟩ ] [ ⟨cellb1_actions⟩ ]

⟨cella_actions⟩ ::= cellA '{' { ⟨l_stmt⟩ } '}'

⟨cellb0_actions⟩ ::= cellB0 '{' { ⟨l_stmt⟩ } '}'

⟨cellb1_actions⟩ ::= cellB1 '{' { ⟨l_stmt⟩ } '}'

⟨l_stmt⟩ ::= ⟨if_else_l_stmt⟩
           | next_header '=' ⟨protocol_id⟩ ';'
           | length '=' ⟨expr⟩ ';'
           | bypass '=' ⟨const⟩ ';'
           | ⟨action_stmt⟩

⟨l_stmts⟩ ::= { ⟨l_stmt⟩ }

⟨if_else_l_stmt⟩ ::= if '(' ⟨expr⟩ ')' ⟨l_stmts⟩ { elseif '(' ⟨expr⟩ ')' ⟨l_stmts⟩ }
                  [ else ⟨l_stmts⟩ ] endif

⟨expr⟩ ::= ⟨atom⟩           //atom expressions
          | ⟨unop⟩ ⟨expr⟩    //unary expressions
          | ⟨expr⟩ ⟨binop⟩ ⟨expr⟩ //binary expressions
          | ⟨expr⟩ '.' IDENT //access to a field in a protocol
          | ⟨expr⟩ '[' ⟨expr⟩ ']' //access to a bit of a field or register
          | ⟨expr⟩ '[' ⟨expr⟩ ':' ⟨expr⟩ ']' //access to a section of a field or register
          | '(' ⟨expr⟩ ')'
          | IDENT '.' length

⟨atom⟩ ::= ⟨const⟩           //const expressions
          | IDENT           //all kinds of access name , ex., field or register access name

⟨unop⟩ ::= int           //convert hexadecimal or binary numbers to integers(signed 32 bits)
          | not           //logical negation
          | '~'           //bit-wise negation

⟨binop⟩ ::= '+'           //addition
          | '-'           //subtraction
          | '*'           //multiplication
          | '/'           //division integer
          | '%'           //remainder
          | '&&'           //logical and
          | '||'          //logical or
          | '&'           //bit-wise and
          | '|'           //bit-wise or

```

'^'	//bit-wise exclusive or
'=='	//equality between any type of values
'<>'	//inequality between any type of values
'<'	//lower on numerics
'>'	//greater on numerics
'<='	//lower or equal on numerics
'>='	//greater or equal on numerics
'<<'	//shift left
'>>'	//shift right
'++'	//concatenation of 2 binary bits' or 2 hexadecimal digits'
hexes	//convert a binary number or an integer to a hexadecimal number
bits	//convert an integer or a hexadecimal number to a binary number

$\langle action_stmt \rangle ::= \mathbf{action} \text{ '=' } \{ \langle instructions \rangle \}$
 $\quad \quad \quad | \langle instruction \rangle$

$\langle instructions \rangle ::= \{ \langle instruction \rangle \}$

$\langle instruction \rangle ::= \langle set \rangle$
 $\quad \quad \quad | \langle mov \rangle$
 $\quad \quad \quad | \langle lg \rangle$
 $\quad \quad \quad | \langle eq \rangle$

$\langle set \rangle ::= \mathbf{set} \langle tgt_reg_acc_name \rangle \text{ ',' } \langle expr \rangle \text{ ';' }$

$\langle mov \rangle ::= \mathbf{mov} \langle mov_reg_acc_name \rangle \text{ ',' } \langle expr \rangle \text{ ';' }$

$\langle lg \rangle ::= \mathbf{lg} \langle tgt_reg_acc_name \rangle \text{ ',' } \langle expr \rangle \text{ ',' } \langle expr \rangle \text{ ';' }$

$\langle eq \rangle ::= \mathbf{eq} \langle tgt_reg_acc_name \rangle \text{ ',' } \langle expr \rangle \text{ ',' } \langle expr \rangle \text{ ';' }$

$\langle reg_acc_set \rangle ::= \langle reg_acc_name \rangle \text{ '=' } \mathbf{IRF} \text{ '[' } \langle expr \rangle \text{ ':' } \langle expr \rangle \text{ ']' ';' }$
 $\quad \quad \quad | \langle reg_acc_name \rangle \text{ '=' } \mathbf{IRF} \text{ '[' } \langle expr \rangle \text{ ']' ';' }$

$\langle tgt_reg_acc_name \rangle ::= \langle reg_acc_name \rangle$
 $\quad \quad \quad | \langle tgt_reg_acc_name \rangle \text{ '[' } \langle expr \rangle \text{ ':' } \langle expr \rangle \text{ ']' }$
 $\quad \quad \quad | \langle tgt_reg_acc_name \rangle \text{ '[' } \langle expr \rangle \text{ ']' }$

$\langle mov_reg_acc_name \rangle ::= \langle tgt_reg_acc_name \rangle$
 $\quad \quad \quad | \langle mov_reg_acc_name \rangle \text{ '++' } \langle tgt_reg_acc_name \rangle$

$\langle reg_acc_name \rangle ::= IDENT$

2.2 Example: A P3 specification

An example of a P3 specification is shown in Fig.2, Fig.3, Fig.4, Fig.5 and Fig.6.

In Fig.2, some global declarations are given, including the length of the global IRF working register set by *lreglen*, the length of the cell IRF register set by *creglen*, a set of protocol identifiers (ethernet, ieee802-1qTag, ipv4, and etc.), a set of layer action identifiers (l2, l2s, l3, l3s, l4, listed in order-dependence), a

```

lreglen = 72 bytes;
creglen = 24 bytes;

pset = {
    ethernet,
    ieee802-1qTag,
    ipv4,
    mpls,
    ieee802-1OuterTag,
    lldp,
    trill,
    qcn,
    igmp,
    ospf,
    pim,
    tcp,
    udp
};

lset = {
    l2,
    l2s,
    l3,
    l3s,
    l4
};

const global_IRF_len = 64;

IRF_gp_reg0_2b = IRF[global_IRF_len+1:global_IRF_len];
IRF_gp_reg1_2b = IRF[global_IRF_len+3:global_IRF_len+2];
}

```

Figure 2: Example of global declarations in P3

global constant declaration identified by *global_IRF_len* and the global register declarations identified by *IRF_gp_reg0_2b* and *IRF_gp_reg1_2b*.

In Fig.3, the layer-action identified *l2* is specified, including the declarations of protocol instances (an *ethernet* instance *eth*, an *ieee802-1qTag* instance *vlan* and an *ieee802-1OuterTag* instance *qinq*), the declarations of registers and guarded actions in the cell A and cell B0.

In Fig.4 are other two layer-action specifications identified by *l2s* and *l3*. Here, the *l2s* layer-action specification is empty. In the *l3* layer-action specification, an *ipv4* protocol instance *v4* as declared, and the declarations of registers and guarded actions respectively in the cell A, cell B0 and cell B1.

Fig.5 and Fig.6 present several examples of protocol specification, which are identified by *ethernet*, *ieee802-1qTag*, *ieee802-1OuterTag*, *mpls* and *ipv4* respectively. They all include the specification for fields, the offset length set by *len* and the guarded actions.

The components of the example above will be used in the following sections.

3 The target language

The target of the P3C compiler is a hardware configuration file consisting of several special tables, whose syntax is referred to the sub-section 3.2.

```

12 {
    ARegisters {
        IRF_l2_send_to_cpu_8b = IRF[15:8];
        IRF_tag_type_2b = IRF[23:16];
        IRF_pkt_type_3b = IRF[31:24];
        IRF_l2_protocol_flag_type_8b = IRF[39:32];

        IRF_outer_vlan_high = IRF[199:192];
        IRF_outer_vlan_low = IRF[207:200];
        IRF_inner_vlan_high = IRF[215:208];
        IRF_inner_vlan_low = IRF[223:216];
    }

    B0Registers {
        IRF_l2_type = IRF[7:0];
    }

    ethernet eth;
    ieee802-1qTag vlan;
    ieee802-10OuterTag qinq;

    cellA {
        if ((eth.etherType == 0x8100) && (vlan.etherType == 0x0800))
            length = length(eth) + length(vlan);
            next_header = ipv4;
            bypass = 1;
            action = {
                mov IRF_outer_vlan_high ++ IRF_outer_vlan_low, vlan.pcp
            ++ vlan.cfi ++ vlan.vid;
                set IRF_tag_type_2b, 1;
                set IRF_pkt_type_3b, 0;
            }
        elseif ((eth.etherType == 0x88a8 || eth.etherType == 0x9200 || eth
        .etherType == 0x9300) && (qinq.ethertype_o == 0x8100) && (qinq.
        etherType_i == 0x0800))
            length = length(eth) + length(qinq);
            next_header = ipv4;
            bypass = 1;
            action = {
                mov IRF_outer_vlan_high ++ IRF_outer_vlan_low, qinq.pcp_o
            ++ qinq.cfi_o ++ qinq.vid_o;
                mov IRF_inner_vlan_high ++ IRF_inner_vlan_low, qinq.pcp_i
            ++ qinq.cfi_i ++ qinq.vid_i;
                set IRF_tag_type_2b, 2;
                set IRF_pkt_type_3b, 0;
            }
        elseif (eth.etherType == 0x0800)
            length = length(eth);
            next_header = ipv4;
            bypass = 1;
            action = {
                set IRF_tag_type_2b, 0;
                set IRF_pkt_type_3b, 0;
            }
        elseif (eth.etherType == 0x88CC)
            length = length(eth);
            next_header = ll dp;
            bypass = 2;
            action = {
                set IRF_l2_protocol_flag_type_8b, 66;
            }
        else
            bypass = 2;
            action = {
                set IRF_l2_send_to_cpu_8b, 1;
            }
        endif
    }

    cellB0 {
        if (eth.dmac == 0xFFFFFFFFFFFF)
            set IRF_l2_type, 3;
        elseif (eth.dmac[40] == 1)7
            set IRF_l2_type, 2;
        else
            set IRF_l2_type, 1;
        endif
    }
}
}

```

Figure 3: Example of a layer action specification

```

12s {
}
13{
    ARegisters {
        IRF_l3_send_to_cpu_8b = IRF[7:0];
        IRF_l3_encode = IRF[15:8];
        IRF_l3_type = IRF[23:16];
        IRF_l3_protocol_flag_type_8b = IRF[31:24];

        IRF_TOS_8b = IRF[199:192];
        IRF_ttl_8b = IRF[207:200];

        IRF_TTL_EXP = IRF[391:384];
    }

    B0Registers {
        IRF_DIP_LB_MUL = IRF[7:0];
        IRF_IPV4_IP_SPECIAL = IRF[15:8];
        IRF_IPV4_SIP_LB = IRF[23:16];
    }

    B1Registers {
        IRF_IP_FRAG_STATUS = IRF[7:0];
    }

    ipv4 v4;

    cellA {
        mov IRF_TOS_8b, v4.diffserv;
        mov IRF_ttl_8b, v4.ttl;
        lg IRF_TTL_EXP, 2, v4.ttl;
    }

    cellB0 {
        if (v4.srcAddr == 0x00000000)
            set IRF_IPV4_IP_SPECIAL, 1;
        elseif (v4.srcAddr[31:24] == 0x7f)
            set IRF_IPV4_SIP_LB, 1;
        endif

        if (v4.dstAddr == 0xffffffff)
            set IRF_IPV4_IP_SPECIAL, 1;
        elseif (v4.dstAddr[31:24] == 0x7f)
            set IRF_DIP_LB_MUL, 1;
        elseif (v4.dstAddr[31:8] == 0xe0000000)
            set IRF_DIP_LB_MUL, 2;
        elseif (v4.dstAddr[31:28] == 0xe)
            set IRF_DIP_LB_MUL, 4;
        endif
    }

    cellB1 {
        if (v4.flagOffset == 0)
            if (v4.flags == 0)
                set IRF_IP_FRAG_STATUS, 3;
            else
                set IRF_IP_FRAG_STATUS, 1;
            endif
        endif
    }
}
}

```

Figure 4: Examples of other layer action specifications


```

protocol ethernet {
    fields = {
        dmac : 48;
        smac : 48;
        etherType : 16;
    }
    length = 14;
}

protocol ieee802-1qTag {
    fields = {
        pcp : 3;
        cfi : 1;
        vid : 12;
        etherType : 16;
    }
    length = 4;
}

protocol ieee802-10OuterTag {
    fields = {
        pcp_o : 3;
        cfi_o : 1;
        vid_o : 12;
        etherType_o : 16;
        pcp_i : 3;
        cfi_i : 1;
        vid_i : 12;
        etherType_i : 16;
    }
    length = 8;
}

protocol mpls {
    fields = {
        lable : 20;
        tc : 3;
        s : 1;
        ttl : 8;
    }
    length = 4;
    if (s == 0)
        next_header = mpls;
    endif
    action = {
    }
}
}

```

Figure 5: Some protocol specifications in P3

```

protocol ipv4 {
  fields = {
    version : 4;
    ihl : 4;
    diffserv : 8;
    totalLen : 16;
    identifaciton : 16;
    flags : 3;
    fragOffset : 13;
    ttl : 8;
    theProtocol : 8;
    hdrChecksum : 16;
    srcAddr : 32;
    dstAddr : 32;
    options : *;
  }

  if (ihl == 5)
    length = 20;
    action = {
      set IRF_l3_type[3], 0;
    }
  elseif (ihl == 6)
    length = 24;
    action = {
      set IRF_l3_type[3], 1;
    }
  elseif (ihl == 7)
    length = 28;
    action = {
      set IRF_l3_type[3], 1;
    }
  else
    action = {
      set IRF_l3_cpu_code_8b, 2;
    }
  endif

  if (theProtocol == 2)
    next_header = igmp;
    bypass = 2;
    action = {
      set IRF_l3_encode, 3;
      set IRF_l3_type[1:0], 0;
      set IRF_l3_protocol_flag_type_8b, 33;
    }
  elseif (theProtocol == 4)
    next_header = ipv4;
    bypass = 0;
    action = {
      set IRF_l3_encode, 7;
      set IRF_l3_type[1:0], 1;
    }
  elseif (theProtocol == 6)
    next_header = tcp;
    bypass = 1;
    action = {
      set IRF_l3_encode, 1;
      set IRF_l3_type[1:0], 2;
    }
  elseif (theProtocol == 0x11)
    next_header = udp;
    bypass = 1;
    action = {
      set IRF_l3_encode, 0;
      set IRF_l3_type[1:0], 2;
    }
  else
    set IRF_l3_send_to_cpu_1b, 1;
  endif
}
}

```

Figure 6: Another protocol specification in P3

To facilitate the co-design of software and hardware, a P3 assembly (ASM) intermediate representation is designed to be generated before the configuration file is produced, referring to the sub-section 3.1 for its syntax and the sub-section 6.1.1 for the associate abstract syntax. In the subsection The P3 assembly is very close to the configuration file in format. In the P3C compiler, we only verify the translations other than the translation from the P3 assembly to the configuration file. The sub-section 6.1.2 includes some examples of the P3 assembly.

3.1 Syntax of P3 assembly

```

<parser_asm> ::= <const_decl> <register_decl> { <layer_block> }

<const_decl> ::= const IDENT '=' Integer ';'          //integer constants, signed 32 bits

<layer_block> ::= <layer_id> ':'
                  { <Pins> }
                  <cella_pb>
                  <cella_pc_cur>
                  <cella_pc_nxt>
                  <cellb0_pb>
                  <cellb0_pc_cur>
                  <cellb1_pb>
                  <cellb1_pc_cur>

<layer_id> ::= IDENT

<Pins> ::= 'Pins' '(' <ins_name> ',' <ins_size> ')'

<cella_pb> ::= 'Abegin' { <cella_pb_item> } 'Aend'

<cella_pc_cur> ::= 'ACbegin' { <cella_pc_cur_item> } 'ACend'

<cella_pc_nxt> ::= 'ANbegin' { <cella_pc_nxt_item> } 'ANend'

<cellb0_pb> ::= 'B0begin' { <cellb0_pb_item> } 'B0end'

<cellb0_pc_cur> ::= 'B0Cbegin' { <cellb0_pc_cur_item> } 'B0Cend'

<cellb1_pb> ::= 'B1begin' { <cellb1_pb_item> } 'B1end'

<cellb1_pc_cur> ::= 'B1Cbegin' { <cellb1_pc_cur_item> } 'B1Cend'

<cella_pb_item> ::= <hdr_id> ',' '{' <cond> { ',' <cond> } '}' ',' <sub_id> ',' <nxt_id>
                  ',' <bypas>

<cella_pc_cur_item> ::= <sub_id> ',' '{' <cmd> { ',' <cmd> } '}' ',' <lyr_offset>

<cella_pc_nxt_item> ::= <nxt_id> ',' '{' <cella_nxt> '}' ',' '{' <cellb0_nxt> '}' ',' '{'
                  <cellb1_nxt> '}'

```

$\langle cellb0_pb_item \rangle ::= \langle hdr_id \rangle \text{ ', ' } \{ \langle cond \rangle \text{ { ', ' } } \langle cond \rangle \} \text{ ' } \text{ ', ' } \langle sub_id \rangle$
 $\langle cellb0_pc_cur_item \rangle ::= \langle sub_id \rangle \text{ ', ' } \{ \langle cmd \rangle \text{ { ', ' } } \langle cmd \rangle \} \text{ ' }$
 $\langle cellb1_pb_item \rangle ::= \langle hdr_id \rangle \text{ ', ' } \{ \langle cond \rangle \text{ { ', ' } } \langle cond \rangle \} \text{ ' } \text{ ', ' } \langle sub_id \rangle$
 $\langle cellb1_pc_cur_item \rangle ::= \langle sub_id \rangle \text{ ', ' } \{ \langle cmd \rangle \text{ { ', ' } } \langle cmd \rangle \} \text{ ' }$

 $\langle hdr_id \rangle ::= \langle num \rangle$
 $\langle sub_id \rangle ::= \langle num \rangle$
 $\langle nxt_id \rangle ::= \langle num \rangle$
 $\langle bypas \rangle ::= \langle num \rangle$
 $\langle lyr_offset \rangle ::= \langle num \rangle$
 $\langle cella_nxt \rangle ::= \text{ ' (' } \{ \langle irf_offset \rangle \} \text{ ') ' + ' (' } \{ \langle prot_offset \rangle \} \text{ ') ' }$
 $\langle cellb0_nxt \rangle ::= \text{ ' (' } \{ \langle irf_offset \rangle \} \text{ ') ' + ' (' } \{ \langle prot_offset \rangle \} \text{ ') ' }$
 $\langle cellb1_nxt \rangle ::= \text{ ' (' } \{ \langle irf_offset \rangle \} \text{ ') ' + ' (' } \{ \langle prot_offset \rangle \} \text{ ') ' }$
 $\langle irf_offset \rangle ::= \langle num \rangle$
 $\langle prot_offset \rangle ::= \langle num \rangle$
 $\langle cond \rangle ::= \langle reg_seg \rangle \text{ '== ' } \langle num \rangle$
 $\quad \quad \quad | \langle ins_seg \rangle \text{ '== ' } \langle num \rangle$
 $\langle cmd \rangle ::= \langle set_cmd \rangle$
 $\quad \quad \quad | \langle mov_cmd \rangle$
 $\quad \quad \quad | \langle lg_cmd \rangle$
 $\quad \quad \quad | \langle eq_cmd \rangle$
 $\langle set_cmd \rangle ::= \text{ ' (' set } \langle reg_seg \rangle \text{ ', ' } \langle num \rangle \text{ ') ' }$
 $\langle mov_cmd \rangle ::= \text{ ' (' mov } \langle reg_seg \rangle \text{ ', ' } \langle src_reg \rangle \text{ ') ' }$
 $\langle lg_cmd \rangle ::= \text{ ' (' lg } \langle reg_seg \rangle \text{ ', ' } \langle src_reg \rangle \text{ ', ' } \langle src_reg \rangle \text{ ') ' }$
 $\langle eq_cmd \rangle ::= \text{ ' (' eq } \langle reg_seg \rangle \text{ ', ' } \langle src_reg \rangle \text{ ', ' } \langle src_reg \rangle \text{ ') ' }$
 $\langle src_reg \rangle ::= \text{ ' (' IRF ', ' } \langle reg_offset \rangle \text{ ', ' } \langle reg_size \rangle \text{ ') ' }$
 $\quad \quad \quad | \langle num \rangle$
 $\langle reg_seg \rangle ::= \text{ ' (' IRF ', ' } \langle reg_offset \rangle \text{ ', ' } \langle seg_size \rangle \text{ ') ' }$
 $\langle ins_seg \rangle ::= \text{ ' (' } \langle ins_name \rangle \text{ ', ' } \langle ins_offset \rangle \text{ ', ' } \langle seg_size \rangle \text{ ') ' }$

$\langle reg_offset \rangle ::= \langle num \rangle$
 $\langle reg_size \rangle ::= \langle num \rangle$
 $\langle seg_size \rangle ::= \langle num \rangle$
 $\langle ins_size \rangle ::= \langle num \rangle$
 $\langle num \rangle ::= Integer \quad // \text{integer constants, signed 32 bits}$
 $\quad \quad \quad | Hexadecimal \quad // \text{hex constants, such as 0x88a8, 0xFFFFFFFF, 0x89, 0x103}$

3.2 The configuration file format

$\langle configuration \rangle ::= \{ \langle layer_config \rangle \}$
 $\langle layer_con \rangle ::= \langle layer_id \rangle \text{' ' } \langle pb_lut \rangle \langle pc_cur_lut \rangle \langle pc_nxt_lut \rangle$
 $\langle layer_con \rangle ::= \langle layer_id \rangle \text{' '}$
 $\quad \quad \quad \langle cella_pb_con \rangle$
 $\quad \quad \quad \langle cella_pc_cur_con \rangle$
 $\quad \quad \quad \langle cella_pc_nxt_con \rangle$
 $\quad \quad \quad \langle cellb0_pb_con \rangle$
 $\quad \quad \quad \langle cellb0_pc_cur_con \rangle$
 $\quad \quad \quad \langle cellb1_pb_con \rangle$
 $\quad \quad \quad \langle cellb1_pc_cur_con \rangle$
 $\langle layer_id \rangle ::= IDENT$
 $\langle cella_pb_con \rangle ::= CellA \text{ PB } \{ \langle cella_pb_con_item \rangle \}$
 $\langle cella_pc_cur_con \rangle ::= CellA \text{ PC CUR } \{ \langle cella_pc_cur_con_item \rangle \}$
 $\langle cella_pc_nxt_con \rangle ::= CellA \text{ PC NXT } \{ \langle cella_pc_nxt_con_item \rangle \}$
 $\langle cellb0_pb_con \rangle ::= CellB0 \text{ PB } \{ \langle cellb0_pb_con_item \rangle \}$
 $\langle cellb0_pc_cur_con \rangle ::= CellB0 \text{ PC CUR } \{ \langle cellb0_pc_cur_con_item \rangle \}$
 $\langle cellb1_pb_con \rangle ::= CellB1 \text{ PB } \{ \langle cellb1_pb_con_item \rangle \}$
 $\langle cellb1_pc_cur_con \rangle ::= CellB1 \text{ PC CUR } \{ \langle cellb1_pc_cur_con_item \rangle \}$
 $\langle cella_pb_con_item \rangle ::= \dots$
 $\langle cella_pc_cur_con_item \rangle ::= \dots$
 $\langle cella_pc_nxt_con_item \rangle ::= \dots$
 $\langle cellb0_pb_con_item \rangle ::= \dots$
 $\langle cellb0_pc_cur_con_item \rangle ::= \dots$

$\langle cellb1_pb_con_item \rangle ::= \dots$

$\langle cellb1_pc_cur_con_item \rangle ::= \dots$

3.3 Examples of the P3 assembly

In this subsection, we show some examples of the P3 assembly corresponding to the example of P3 specification in Section 2.2.

Fig.7 shows the P3 ASM corresponding to the layer action L2 in Fig.3, where three protocol instances *eth*, *vlan* and *qinq* are declared.

The P3 ASM for a layer action should have 7 tables, three tables for the Cell A, and two tables for the Cell B0 and Cell B1 respectively. In Fig.7, we omit the tables for Cell B1 since no table-driven actions specified in this cell in Fig.3.

The three tables of Cell A are *cella_pb*, *cella_pc_cur* and *cella_pc_nxt*. In the table *cella_pb*, the attributes for the next protocol identifier (*next_id*) and the bypass value are set. Besides, a table looking-up operation is specified by a combination of *guard-condition* and *jump-to(sub_id)*, such as the *guard-condition* (*eth*, 96, 16) == 0x88a8, (*qinq*, 16, 16) == 0x8100, (*qinq*, 48, 16) == 0x0800, the conjunction of the atomic conditions (propositions), and *jump-to* the 0x2 labeled actions' set in *cella_pc_cur* table.

In the *cella_pc_cur* table, 0x2 labeled actions' set includes the following commands:

- `mov IRF_outer_vlan_high, IRF_outer_vlan_low, qinq.pcp_o,qinq.cfi_o,qinq.vid_o;`
- `mov IRF_inner_vlan_high, IRF_inner_vlan_low, qinq.pcp_i,qinq.cfi_i,qinq.vid_i;`
- `set IRF_tag_type_2b, 2;set IRF_pkt_type_3b, 0;`

Besides, in the *cella_pc_cur* table, the attribute for the next-layer offset (*lyr_offset*) is set.

In the table *cella_pc_nxt*, some fields of a protocol are masked for the usage in the later layers, partitioned by the different cells. For example in the first line of the *cella_pc_nxt* table in Fig.7, the masked fields of the protocol *ipv4* are (0 9) for the cell A, (0xc 0xd 0xe 0xf 0x10 0x11 0x12 0x13) for the cell B0, and (6 7) for the cell B1. From the Fig.4, we know that an *ipv4* instance *v4* is declared in the layer action *l3s*. The fields *ihl* and *theProtocol* are used in the cell A, the fields *srcAddr* and *dstAddr* are used in the cell B0, and the fields *flagOffset* and *flags* are used in the cell B1. Referring to the offsets of these fields in the *ipv4* protocol in Fig.6, the fields *ihl* and *theProtocol* are masked by (0 9) corresponding to the 1st byte and the 10th byte in *ipv4*. Similarly, the fields *srcAddr* and *dstAddr* are masked by (0xc 0xd 0xe 0xf 0x10 0x11 0x12 0x13), and the fields *flagOffset* and *flags* are masked by (6 7).

In Fig.7, the tables *cellb0_pb* and *cellb0_pc_cur* are the same in structure with *cella_pb* and *cella_pc_cur* except for without the information to set the next protocol identifier, the bypass value and the next-layer offset.

Fig.8 shows the P3 ASM extracts corresponding to the layer action L3 in Fig.4, where the protocol instances *p4* is declared.

```

//L2header
//Ethernet II:DMAC(6B)+SMAC(6B)+Type(2B)
//VLAN(18B) :DMAC(6B)+SMAC(6B)+Type(2B)+TAG(2B:PRI/3b+CFI/1b+VID/12b)+
Length/Type(2B)
//Qinq(22B) :DMAC(6B)+SMAC(6B)+EType(2B)+TAG(2B:PRI/3b+CFI/1b+VID/12b)+
EType(2B)+TAG(2B:PRI/3b+CFI/1b+VID/12b)+LEN/ETType(2B)

l2:

Pins (eth, 112) // size: 8*14
Pins (vlan, 32) // size: 8*4
Pins (qinq, 64) // size: 8*8

Abegin

//cella_pb(407bit*32)
//hdr_id(7)+mask(24*8b)+value(24*8b)+sub_id(7)+nxt_id(7)+bypass(2:
mainbypass(1)+subbypass(1))

0x1,{(eth, 96, 16) == 0x8100, (vlan, 16, 16) == 0x0800}, 0x1, 0x3, 1//eth+
vlan+ipv4
0x1, {(eth, 96, 16) == 0x88a8, (qinq, 16, 16) == 0x8100, (qinq, 48, 16) ==
0x0800},0x2,0x3,1//eth+qinq+ipv4
0x1, {(eth, 96, 16) == 0x9200, (qinq, 16, 16) == 0x8100, (qinq, 48, 16) ==
0x0800},0x2,0x3,1//eth+qinq+ipv4
0x1, {(eth, 96, 16) == 0x9300, (qinq, 16, 16) == 0x8100, (qinq, 48, 16) ==
0x0800},0x2,0x3,1//eth+qinq+ipv4
0x1, {(eth, 96, 16) == 0x0800}, 0x3, 0x3, 1//eth+ipv4
0x1, {(eth, 96, 16) == 0x88cc}, 0x4, 0x6, 2//eth+lldp

Aend

ACbegin

//cella_pc_cur(328bit*32)
//vliw(320:alu(8*24b)+mov(8*8b)+set(8*8b))+lyr_offset(8)
0x1,{(mov (IRF,192,16), (vlan,0,16)),(set (IRF,16,8), 1), (set (IRF,24,8),
0)}, 0x12
0x2,{(mov (IRF,192,16), (vlan,0,16)),(mov (IRF,208,16), (vlan,0,16)),(set
(IRF,16,8), 2), (set (IRF,24,8), 0)}, 0x16
0x3,{(set (IRF,16,8), 0), (set (IRF,24,8), 0)}, 0xc
0x4,{(set (IRF,32,8), 66)}, 0xc

ACend

ANbegin

//cella_pc_nxt(583bit*32)
//nxt_id(7)+pa_offset(3*24*8b:cellA(irf/2+fra/22)+cellB0(irf/2+fra/22)+
cellB1(irf/2+fra/22))

0x3, {( ) + (0 9)}, {( ) + (0xc 0xd 0xe 0xf 0x10 0x11 0x12 0x13)}, {( ) + (6
7)}//ipv4
0x6, {( ) + ( )}, {( ) + ( )}, {( ) + ( )}//lldp

ANend

BObegin

//cellb0_pb(398bit*32)
//hdr_id(7)+mask(24*8b)+value(24*8b)+sub_id(7)

0x1, {(eth, 0, 48) == 0xFFFFFFFFFFFF}, 0x1//eth.dmac == 0xFFFFFFFFFFFF
0x1, {(eth, 40, 1) == 1}, 0x2//eth.dmac[40] == 1

BOend

BOCbegin

//cellb0_pc_cur(320bit*32)
//vliw(320:alu(8*24b)+mov(8*8b)+set(8*8b))
0x2, {(set (IRF,0,8), 3)}//sub_id:01,set IRF_l2_type = 3;
0x2, {(set (IRF,0,8), 2)}//sub_id:02,set IRF_l2_type = 2;

BOCend

```

Figure 7: P3 ASM for the layer action L2 in Fig.3

```

//L3header(IPheader)
//IPv4(20B) :Ver(4bit)+IHL(4bit)+TyoS(8bit)+TtlLen(16bit)+Iden(16bit)+Flg
              (3bit)+FraOffset(13bit)+TimeTOLive(8bit)+Protocol(8bit)+HdrCheSUM
              (16bit)+SAddr(32bit)+DAddr(32bit)
L3:
Pins (v4, 224) // size: 8*28
Abegin
//cella_pb(407bit*32)
//hdr_id(7)+mask(24*8b)+value(24*8b)+sub_id(7)+nxt_id(7)+bypass(2:
              mainbypass(1)+subbypass(1))

Ox3, {(v4, 4, 4) == 5, (v4, 72, 8) == 2}, Ox1, Ox9, 2
.....
Ox3, {(v4, 4, 4) == 7, (v4, 72, 8) == 0x11}, Ox1, Ox11, 1
Aend

ACbegin
//cella_pc_cur(328bit*32)
//vliw(320:alu(8*24b)+mov(8*8b)+set(8*8b))+lyr_offset(8)
Ox1, {(mov (IRF,192,8), (v4,8,8)),(mov (IRF,200,8), (v4,64,8)), (lg (IRF
,384,8), 2, (v4,64,8)), (set (IRF,19,1), 0), (set (IRF,8,8), 3), (
set (IRF,16,2),0), (set (IRF,24,8), 33))}, Ox14
.....
Oxc, {(mov (IRF,192,8), (v4,8,8)),(mov (IRF,200,8), (v4,64,8)), (lg (IRF
,384,8), 2, (v4,64,8)), (set (IRF,19,1), 1), (set (IRF,8,8), 0),
(set (IRF,16,2), 2)}, Ox1c
ACend

ANbegin
//cella_pc_nxt(583bit*32)
//nxt_id(7)+pa_offset(3*24*8b)
Ox9, {( ) + ( )}, {( ) + ( )}, {( ) + ( )} //igmp
Ox3, {( ) + ( )}, {( ) + ( )}, {( ) + ( )} //ipv4
Oxc, {( ) + ( )}, {( ) + ( )}, {( ) + ( )} //tcp
Oxd, {( ) + ( )}, {( ) + ( )}, {( ) + ( )} //udp
ANend

BObegin
//cellb0_pb(398bit*32)
//hdr_id(7)+mask(24*8b)+value(24*8b)+sub_id(7)
Ox3, {(v4, 96, 32) == 0x00000000, (v4,128,32) == 0xffffffff}, Ox1
.....
Ox3, {(v4.srcAddr?,(v4,156,4) == 0xe), 0xe
BOend

BOCbegin
//cellb0_pc_cur(320bit*32)
//vliw(320:alu(8*24b)+mov(8*8b)+set(8*8b))
Ox1, {(set (IRF,8,8),1),?} //sub_id:01,set IRF_IPV4_IP_SPECIAL, 1;set
IRF_IPV4_IP_SPECIAL, 1;
.....
Oxe, {(set (IRF,0,8),4)} //sub_id:0e,set IRF_DIP_LB_MUL, 4;
BOCend

Bibegin
//cellb1_pb(398bit*32)
//hdr_id(7)+mask(24*8b)+value(24*8b)+sub_id(7)
Ox3, {(v4, 51, 13) == 0, (v4,48,3) == 0}, Ox1//v4.flagOffset == 0,v4.flags
== 0
Ox3, {(v4, 51, 13) == 0, (v4,48,3) == 0}, Ox2//v4.flagOffset == 0,v4.
flags != 0
Blend

B1Cbegin
//cellb1_pc_cur(320bit*32)
//vliw(320:alu(8*24b)+mov(8*8b)+set(8*8b))
Ox1, {(set (IRF,0,7),3)} //sub_id:01,set IRF_IP_FRAG_STATUS, 3;
Ox2, {(set (IRF,0,7),1)} //sub_id:02,set IRF_IP_FRAG_STATUS, 1;
B1Cend//

```

Figure 8: P3 ASM for another layer action L3 in Fig.4 (extracts)

It is worth to noting that the table looking-up operations of *cella_pb* in Fig.8 is corresponding to the guarded actions specified for the protocol *ipv4* in Fig.6.

4 Parsing

By scanning and parsing, a P3 source specification such as the example in Section 2.2 is translated into its corresponding P3 AST, referring to Fig.1. The syntax of a P3 AST is presented in the subsection 4.1.

4.1 The P3 Abstract Syntax Tree

```

<parser_spec> ::= Parser ( <layer_reg_len>, <cell_reg_len>, <protocol_set>, <layer_set>,
                          { <decl> } )

<layer_reg_len> ::= Lreglen ( IntConst( Integer ) )

<cell_reg_len> ::= Creglen ( IntConst( Integer ) )

<protocol_set> ::= Pset ( <id_list> )

<layer_set> ::= Lset ( <id_list> )

<id_list> ::= { IDENT }

<decl> ::= ConstDecl ( <const_decl> )
        | RegAccSet ( <reg_acc_set> )
        | <protocol_decl>
        | <layer_action>

<const_decl> ::= ConstDcl( IDENT, <const> )

<const> ::= IDENT           // constant identifiers
        | IntConst( Integer ) //integer constants, signed 32 bits
        | HexConst( Hexadecimal ) //hex constants, such as 0x88a8, 0xFFFFFFFF
        | BitSConst( BITS ) //binary constants, such as 001001, 100, 0, 1

<protocol_decl> ::= ProtocolDecl ( IDENT , <protocol> )

<protocol> ::= Protocol ( <fields> , <p_stmts> )

<fields> ::= ( Fields ( <field> { <field> }, OptionFields ( [ <option_field> ] ) )

<field> ::= ( IDENT , <const> )

<option_field> ::= ( IDENT , 0 )

<p_stmts> ::= { <p_stmt> }

```

$$\begin{aligned}
\langle p_stmt \rangle &::= \langle if_else_p_stmt \rangle \\
&\quad | \textit{NextHeader} (IDENT) \\
&\quad | \textit{Length} (\langle const \rangle) \\
&\quad | \textit{Bypass} (\langle const \rangle) \\
&\quad | \langle action_stmt \rangle \\
\langle if_else_p_stmt \rangle &::= \textit{IfElseP} (\{ \langle if_branch_p \rangle \} , \langle default_branch_p \rangle) \\
\langle if_branch_p \rangle &::= (\langle expr \rangle , \langle p_stmts \rangle) \\
\langle default_branch_p \rangle &::= [\langle p_stmts \rangle] \\
\langle layer_action \rangle &::= \textit{LayerAction} (IDENT , \langle local_reg_decl \rangle , \langle l_decls \rangle , \langle l_actions \rangle) \\
\langle l_decls \rangle &::= \langle local_reg_decl \rangle \{ \langle l_decl \rangle \} \\
\langle l_decl \rangle &::= \textit{ProtocolDef} (IDENT , \langle id_list \rangle) \\
\langle local_reg_decl \rangle &::= \textit{LocalRegs} (\langle cella_regs \rangle , \langle cellb0_regs \rangle , \langle cellb1_regs \rangle) \\
\langle cella_regs \rangle &::= \textit{CellARegs} (\{ \langle reg_acc_set \rangle \}) \\
\langle cellb0_regs \rangle &::= \textit{CellB0Regs} (\{ \langle reg_acc_set \rangle \}) \\
\langle cellb1_regs \rangle &::= \textit{CellB1Regs} (\{ \langle reg_acc_set \rangle \}) \\
\langle l_actions \rangle &::= \textit{LocalActions} (\langle cella_actions \rangle , \langle cellb0_actions \rangle , \langle cellb1_actions \rangle) \\
\langle cella_actions \rangle &::= \textit{CellA} (\{ \langle l_stmt \rangle \}) \\
\langle cellb0_actions \rangle &::= \textit{CellB0} (\{ \langle l_stmt \rangle \}) \\
\langle cellb1_actions \rangle &::= \textit{CellB1} (\{ \langle l_stmt \rangle \}) \\
\langle l_stmt \rangle &::= \langle if_else_l_stmt \rangle \\
&\quad | \textit{NextHeader} (IDENT) \\
&\quad | \textit{Length} (\langle expr \rangle) \\
&\quad | \textit{Bypass} (\langle const \rangle) \\
&\quad | \langle action_stmt \rangle \\
\langle l_stmts \rangle &::= \{ \langle l_stmt \rangle \} \\
\langle if_else_l_stmt \rangle &::= \textit{IfElseL} (\{ \langle if_branch_l \rangle \} , \langle default_branch_l \rangle) \\
\langle if_branch_l \rangle &::= (\langle expr \rangle , \langle l_stmts \rangle) \\
\langle default_branch_l \rangle &::= [\langle l_stmts \rangle]
\end{aligned}$$

```

⟨expr⟩ ::= Eatom(⟨atom⟩)
          | Eunop(⟨unop⟩, ⟨expr⟩)    (* unary operation *)
          | Ebinop(⟨binop⟩, ⟨expr⟩, ⟨expr⟩) (* binary operation *)
          | Efield(⟨expr⟩, IDENT)    (* access to a field in a protocol *)
          | EFieldBit(⟨expr⟩, ⟨expr⟩) (*access to a bit of a field or a register access*)
          | EFieldSection(⟨expr⟩, ⟨expr⟩, ⟨expr⟩)
            (* access to a section of a field or a register access *)
          | ProtLen(IDENT)

⟨atom⟩ ::= Econst(⟨const⟩)           //const expressions
          | IDENT                     //all kinds of access name , ex., field or register access name

⟨unop⟩ ::= Oint                      //convert hexadecimal or binary numbers to integers
          | Onot                      //logical negation
          | Oneg                      //bit-wise negation

⟨binop⟩ ::= Oadd                     // addition '+'
          | Osub                     // subtraction '-'
          | Omul                     // multiplication '*'
          | Odivint                  // division integer '/'
          | Omod                     // remainder '%'
          | Oand                     //logical and '&&'
          | Oor                      //logical or '||'
          | Oband                    //bit-wise and '&'
          | Obor                     //bit-wise or '|'
          | Obeor                    //bit-wise exclusive or '^'
          | Oeq                      // comparison ([=])
          | One                      // comparison ([<>])
          | Olt                      // comparison ([<])
          | Ogt                      // comparison ([>])
          | Ole                      // comparison ([<=])
          | Oge                      // comparison ([>=])
          | Osl                      //shift left '<<'
          | Osr                      //shift right '>>'
          | Obc                      //bits' concatenation '++'
          | Ohexes //convert a binary number or an integer to a hexadecimal number
          | Obits  //convert an integer or a hexadecimal number to a binary number

⟨action_stmt⟩ ::= Action(⟨instructions⟩ )

⟨instructions⟩ ::= { ⟨instruction⟩ }

⟨instruction⟩ ::= Set (⟨tgt_reg_acc_name⟩, ⟨expr⟩)
                  | Mov (⟨mov_reg_acc_name⟩, ⟨expr⟩)
                  | Lg (⟨tgt_reg_acc_name⟩, ⟨expr⟩, ⟨expr⟩)
                  | Eq (⟨tgt_reg_acc_name⟩, ⟨expr⟩, ⟨expr⟩)

⟨reg_acc_set⟩ ::= IRF( IDENT, ⟨expr⟩ , ⟨expr⟩ )
                  | IRF( IDENT, ⟨expr⟩ )

⟨tgt_reg_acc_name⟩ ::= TargetRegAccName( IDENT )
                      | TargetRegAccName ( ⟨tgt_reg_acc_name⟩, ⟨expr⟩ , ⟨expr⟩ )
                      | TargetRegAccName ( ⟨tgt_reg_acc_name⟩, ⟨expr⟩ )

```

$$\langle mov_reg_acc_name \rangle ::= MovRegAccName(\langle tgt_reg_acc_name \rangle) \\ | MovRegAccName(\langle mov_reg_acc_name \rangle, \langle tgt_reg_acc_name \rangle)$$

4.2 Implementation and Verification

In the current version of the compiler, the OCaml code of parsing is generated in Coq by Menhir *Menhir* [8], which has been formally validated and produces proofs of correctness and completeness by the J.-H. Jourdan approach [5] used in CompCert [7, 6, 4].

As examples, we list as follows the printed P3 AST corresponding to Fig.2 and Fig.3, part of the example in Section 2.2.

```

<parser>
  <layer_reg_len>
    <const>
      <int>(72)
  <cell_reg_len>
    <const>
      <int>(24)
  <protocol_set>
    <id>(ethernet)
    <id>(ieee802-1qTag)
    <id>(ipv4)
    <id>(mpls)
    <id>(ieee802-1OuterTag)
    <id>(lldp)
    <id>(trill)
    <id>(qcn)
    <id>(igmp)
    <id>(ospf)
    <id>(pim)
    <id>(tcp)
    <id>(udp)
  <layer_set>
    <id>(l2)
    <id>(l2s)
    <id>(l3)
    <id>(l3s)
    <id>(l4)
  <decl>
    <const_decl>
      <id>(global_IRF_len)
      <const_expr>
        <const>
          <int>(64)
    <decl>
      <reg_acc_set>
        <reg_acc_name>
          <id>(IRF_gp_reg0_2b)
        <binop_expr>
          <binop>(+)
          <const_expr>
            <const>
              <id>(global_IRF_len)
          <const_expr>

```

```

        <const>
        <int>(1)
    <const_expr>
    <const>
    <id>(global_IRF_len)
<decl>
    <reg_acc_set>
    <reg_acc_name>
    <id>(IRF_gp_reg1_2b)
    <binop_expr>
    <binop>(+)
    <const_expr>
    <const>
    <id>(global_IRF_len)
    <const_expr>
    <const>
    <int>(3)
    <binop_expr>
    <binop>(+)
    <const_expr>
    <const>
    <id>(global_IRF_len)
    <const_expr>
    <const>
    <int>(2)
<decl>
    <layer_action>
    <id>(l2)
    <local_reg_decl>
    <cella_regs>
    <reg_acc_set>
    <reg_acc_name>
    <id>(IRF_l2_send_to_cpu_8b)
    <const_expr>
    <const>
    <int>(15)
    <const_expr>
    <const>
    <int>(8)
    <reg_acc_set>
    <reg_acc_name>
    <id>(IRF_tag_type_2b)
    <const_expr>
    <const>
    <int>(23)
    <const_expr>
    <const>
    <int>(16)
    <reg_acc_set>
    <reg_acc_name>
    <id>(IRF_pkt_type_3b)
    <const_expr>
    <const>
    <int>(31)
    <const_expr>
    <const>
    <int>(24)

```

```

<reg_acc_set>
  <reg_acc_name>
    <id>(IRF_l2_protocol_flag_type_8b)
  <const_expr>
    <const>
      <int>(39)
    <const_expr>
      <const>
        <int>(32)
<reg_acc_set>
  <reg_acc_name>
    <id>(IRF_outer_vlan_high)
  <const_expr>
    <const>
      <int>(199)
    <const_expr>
      <const>
        <int>(192)
<reg_acc_set>
  <reg_acc_name>
    <id>(IRF_outer_vlan_low)
  <const_expr>
    <const>
      <int>(207)
    <const_expr>
      <const>
        <int>(200)
<reg_acc_set>
  <reg_acc_name>
    <id>(IRF_inner_vlan_high)
  <const_expr>
    <const>
      <int>(215)
    <const_expr>
      <const>
        <int>(208)
<reg_acc_set>
  <reg_acc_name>
    <id>(IRF_inner_vlan_low)
  <const_expr>
    <const>
      <int>(223)
    <const_expr>
      <const>
        <int>(216)
<cellb0_regs>
  <reg_acc_set>
    <reg_acc_name>
      <id>(IRF_l2_type)
    <const_expr>
      <const>
        <int>(7)
    <const_expr>
      <const>
        <int>(0)
  <cellb1_regs>(None)
<l_decl>

```

```

        <id>(ethernet)
        <id>(eth)
    <l_decl>
        <id>(ieee802-1qTag)
        <id>(vlan)
    <l_decl>
        <id>(ieee802-1OuterTag)
        <id>(qinq)
    <l_actions>
        <cella_actions>
            <l_stmt>
                <if_else_l_stmt>
                    <if_branch_l>
                        <binop_expr>
                            binop(&&)
                            <paren_expr>
                                <binop_expr>
                                    binop(==)
                                    <field_expr>
                                        <const_expr>
                                            <const>
                                                <id>(eth)
                                                <id>(etherType)
                                            <const_expr>
                                                <const>
                                                    <hex>(0x8100)
                                <paren_expr>
                                    <binop_expr>
                                        binop(==)
                                        <field_expr>
                                            <const_expr>
                                                <const>
                                                    <id>(vlan)
                                                    <id>(etherType)
                                            <const_expr>
                                                <const>
                                                    <hex>(0x0800)
                            <l_stmt>
                                <binop_expr>
                                    <binop>(+)
                                    <length_expr>
                                        <id>(eth)
                                    <length_expr>
                                        <id>(vlan)
                        <l_stmt>
                            <id>(ipv4)
                    <l_stmt>
                        <const>
                            <int>(1)
                <l_stmt>
                    <action_stmt>
                        <mov_instruction>
                            <mov_reg_acc_name>
                                <mov_reg_acc_name>
                                    <tgt_reg_acc_name>
                                        <id>(
IRF_outer_vlan_high)

```

```

        <tgt_reg_acc_name>
        <id>(IRF_outer_vlan_low)
    <binop_expr>
    binop(++)
    <binop_expr>
    binop(++)
    <field_expr>
    <const_expr>
    <const>
    <id>(vlan)
    <id>(pcp)
    <field_expr>
    <const_expr>
    <const>
    <id>(vlan)
    <id>(cfi)
    <field_expr>
    <const_expr>
    <const>
    <id>(vlan)
    <id>(vid)
    <seq_instruction>
    <tgt_reg_acc_name>
    <id>(IRF_tag_type_2b)
    <const_expr>
    <const>
    <int>(1)
    <seq_instruction>
    <tgt_reg_acc_name>
    <id>(IRF_pkt_type_3b)
    <const_expr>
    <const>
    <int>(0)
<if_branch_1>
    <binop_expr>
    binop(&&)
    <binop_expr>
    binop(&&)
    <paren_expr>
    <binop_expr>
    binop(||)
    <binop_expr>
    binop(||)
    <binop_expr>
    binop(==)
    <field_expr>
    <const_expr>
    <const>
    <id>(eth)
    <id>(etherType)
    <const_expr>
    <const>
    <hex>(0x88a8)
    <binop_expr>
    binop(==)
    <field_expr>
    <const_expr>

```



```

        <const>
        <id>(eth)
        <id>(etherType)
        <const_expr>
        <const>
        <hex>(0x9200)
    <binop_expr>
    binop(==)
    <field_expr>
    <const_expr>
    <const>
    <id>(eth)
    <id>(etherType)
    <const_expr>
    <const>
    <hex>(0x9300)
<paren_expr>
<binop_expr>
binop(==)
<field_expr>
<const_expr>
<const>
<id>(qinq)
<id>(ethertype_o)
<const_expr>
<const>
<hex>(0x8100)
<paren_expr>
<binop_expr>
binop(==)
<field_expr>
<const_expr>
<const>
<id>(qinq)
<id>(etherType_i)
<const_expr>
<const>
<hex>(0x0800)
<l_stmt>
<binop_expr>
<binop>(+)
<length_expr>
<id>(eth)
<length_expr>
<id>(qinq)
<l_stmt>
<id>(ipv4)
<l_stmt>
<const>
<int>(1)
<l_stmt>
<action_stmt>
<mov_instruction>
<mov_reg_acc_name>
<mov_reg_acc_name>
<tgt_reg_acc_name>
<id>(

```

IRF_outer_vlan_high)

```

    <tgt_reg_acc_name>
    <id>(IRF_outer_vlan_low)
<binop_expr>
  binop(++)
  <binop_expr>
    binop(++)
    <field_expr>
      <const_expr>
        <const>
          <id>(qinq)
        <id>(pcp_o)
      <field_expr>
        <const_expr>
          <const>
            <id>(qinq)
          <id>(cfi_o)
      <field_expr>
        <const_expr>
          <const>
            <id>(qinq)
          <id>(vid_o)
<mov_instruction>
  <mov_reg_acc_name>
  <mov_reg_acc_name>
  <tgt_reg_acc_name>
  <id>(

```

IRF_inner_vlan_high)

```

    <tgt_reg_acc_name>
    <id>(IRF_inner_vlan_low)
<binop_expr>
  binop(++)
  <binop_expr>
    binop(++)
    <field_expr>
      <const_expr>
        <const>
          <id>(qinq)
        <id>(pcp_i)
      <field_expr>
        <const_expr>
          <const>
            <id>(qinq)
          <id>(cfi_i)
      <field_expr>
        <const_expr>
          <const>
            <id>(qinq)
          <id>(vid_i)
<seq_instruction>
  <tgt_reg_acc_name>
  <id>(IRF_tag_type_2b)
  <const_expr>
    <const>
      <int>(2)
<seq_instruction>
  <tgt_reg_acc_name>

```

```

                                <id>(IRF_pkt_type_3b)
                                <const_expr>
                                <const>
                                <int>(0)
<if_branch_1>
  <binop_expr>
    binop(==)
    <field_expr>
      <const_expr>
      <const>
      <id>(eth)
      <id>(etherType)
    <const_expr>
    <const>
    <hex>(0x0800)
  <l_stmt>
    <length_expr>
    <id>(eth)
  <l_stmt>
    <id>(ipv4)
  <l_stmt>
    <const>
    <int>(1)
  <l_stmt>
    <action_stmt>
      <seq_instruction>
        <tgt_reg_acc_name>
        <id>(IRF_tag_type_2b)
        <const_expr>
        <const>
        <int>(0)
      <seq_instruction>
        <tgt_reg_acc_name>
        <id>(IRF_pkt_type_3b)
        <const_expr>
        <const>
        <int>(0)
<if_branch_1>
  <binop_expr>
    binop(==)
    <field_expr>
      <const_expr>
      <const>
      <id>(eth)
      <id>(etherType)
    <const_expr>
    <const>
    <hex>(0x88CC)
  <l_stmt>
    <length_expr>
    <id>(eth)
  <l_stmt>
    <id>(lldp)
  <l_stmt>
    <const>
    <int>(2)
  <l_stmt>

```

```

        <action_stmt>
        <seq_instruction>
        <tgt_reg_acc_name>
        <id>(
IRF_l2_protocol_flag_type_8b)
        <const_expr>
        <const>
        <int>(66)
    <default_branch_1>
    <l_stmt>
    <const>
    <int>(2)
    <l_stmt>
    <action_stmt>
    <seq_instruction>
    <tgt_reg_acc_name>
    <id>(IRF_l2_send_to_cpu_8b)
    <const_expr>
    <const>
    <int>(1)
<cellb0_actions>
<l_stmt>
<if_else_1_stmt>
<if_branch_1>
<binop_expr>
    binop(==)
    <field_expr>
    <const_expr>
    <const>
    <id>(eth)
    <id>(dmac)
    <const_expr>
    <const>
    <hex>(0xFFFFFFFFFFFF)
<l_stmt>
    <action_stmt>
    <seq_instruction>
    <tgt_reg_acc_name>
    <id>(IRF_l2_type)
    <const_expr>
    <const>
    <int>(3)
<if_branch_1>
<binop_expr>
    binop(==)
    <bit_expr>
    <field_expr>
    <const_expr>
    <const>
    <id>(eth)
    <id>(dmac)
    <const_expr>
    <const>
    <int>(40)
    <const_expr>
    <const>
    <int>(1)

```

```

    <l_stmt>
      <action_stmt>
        <seq_instruction>
          <tgt_reg_acc_name>
            <id>(IRF_l2_type)
          <const_expr>
            <const>
              <int>(2)
    <default_branch_l>
    <l_stmt>
      <action_stmt>
        <seq_instruction>
          <tgt_reg_acc_name>
            <id>(IRF_l2_type)
          <const_expr>
            <const>
              <int>(1)
    <cellb1_actions>(None)

```

5 Type Checking

By type checking on the P3 AST, we can guarantee a P3 source specification to be *well-typed*. The type checking is based on the type rules in the type system for P3 AST defined in the subsection 5.1. If the P3 AST can not pass the type checking, the P3 source specification will be refused by the compiler.

5.1 Type system for P3

5.1.1 Type expressions

A basic type expression can be defined by the syntax shown as follows.

<type> ::=	<i>Int</i>	integer type, signed integer up to 32 bits
	<i>Bool</i>	boolean type
	<i>Hexes</i> (<i>n</i>)	hexadecimal type, with <i>n</i> hexadecimal digits
	<i>Bits</i> (<i>n</i>)	binary type, with <i>n</i> binary digits
	<i>RegAcc</i> (<i>k</i> , <i>i</i> , <i>j</i>)	register segment access type, $0 \leq j \leq i < k$, and <i>k</i> is the size of the register <i>IRF</i> in the current context
	<i>FieldAcc</i> (<i>id</i> , <i>k</i> , <i>i</i> , <i>j</i>)	protocol field access type in a cell context, <i>k</i> is the protocol instance length, with $0 \leq i \leq j < k \vee (i = k \wedge j \text{ is undefined})$
	<i>FieldAcc</i> (<i>k</i> , <i>i</i> , <i>j</i>)	protocol field access type in a protocol context, <i>k</i> is the protocol instance length, with $0 \leq i \leq j < k \vee (i = k \wedge j \text{ is undefined})$
	<i>X</i>	type to specify that any instance of the protocol named <i>X</i> has a type <i>X</i>

For a constant expression, we need to compute its value for the validity checking in many places. Hence, we add an associate value to form an additional

basic type, shown as follows.

$$\langle type \rangle ::= (\tau, i) \quad \begin{array}{l} \text{a integer constant type, with the type } \tau \text{ and the} \\ \text{integer value } i, \text{ a signed integer up to 32 bits} \end{array}$$

5.1.2 Typing environment

A typing environment associates type expressions to variables and has the form

$$\mathcal{E} ::= [x_1 : A_1, x_2 : A_2, \dots, x_n : A_n]$$

where $x_i \neq x_j$ for all i and j , satisfying $i \neq j$ and $(1 \leq i, j \leq n)$.

We use \mathcal{C} , \mathcal{R} , \mathcal{L} and \mathcal{P} to denote a global const identifiers' typing environment, a special typing environment (see below), a local typing environment for a layer, and a local typing environment for a protocol respectively. We use \mathcal{L}_A , \mathcal{L}_{B0} and \mathcal{L}_{B1} to denote a particular local typing environment specific to the Cell A, Cell B0, and Cell B1 contexts in the current layer environment \mathcal{L} . In some cases, we use \mathcal{L}_{id} or \mathcal{P}_{id} to denote a particular local typing environment specific to the context of a layer or a protocol identified by id .

We introduce a special typing environment \mathcal{R} , which records the read-only register accesses to the last layer and is dynamically changed between the layers. At the beginning, \mathcal{R} is initialized by the global register declarations, which is available to be read at the first layer declared. Then it is changed when a new layer is just entered, and become the combination of \mathcal{L}_A , \mathcal{L}_{B0} and \mathcal{L}_{B1} in the last layer environment \mathcal{L} .

Finally, to provide more confident consistency, we define some parameters syntactically, including the size of a layer register, the size of a cell register, a protocol set and a layer set syntactically. Accordingly, we introduce special global environments $\mathcal{L}reglen$, $\mathcal{C}reglen$, $\mathcal{P}set$ and $\mathcal{L}set$. For convenience, we use \mathcal{G} to denote the combination of them, that is, $\mathcal{G} = (\mathcal{L}reglen, \mathcal{C}reglen, \mathcal{P}set, \mathcal{L}set)$.

5.1.3 Judgements

- $\mathcal{E} \vdash e : A$, implies that,
under the well-formed typing environment \mathcal{E} , the expression e is well-typed and has the type A . Here, \mathcal{E} can be \emptyset , \mathcal{G} , or \mathcal{C} .
- $\mathcal{E} \vdash \diamond$, means that \mathcal{E} is a well-formed typing environment. Here, \mathcal{E} can be \emptyset , \mathcal{G} , \mathcal{C} , \mathcal{L} , \mathcal{P} , \mathcal{L}_A , \mathcal{L}_{B0} or \mathcal{L}_{B1} .
- $\mathcal{G}, \mathcal{C} \vdash e : A$, implies that,
under the well-formed typing environments \mathcal{G} and \mathcal{C} , the expression e is well-typed and has the type A .
- $\mathcal{G}, \mathcal{C}, \mathcal{R} \vdash e : A$, implies that,
under the well-formed typing environments \mathcal{G} , \mathcal{C} and \mathcal{R} , the expression e is well-typed and has the type A .

- $\mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L} \vdash e : A$, implies that,
under the well-formed typing environments \mathcal{G} , \mathcal{C} , \mathcal{R} and \mathcal{L} , the expression e is well-typed and has the type A .
- $\mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_C \vdash e : A$, implies that,
under the well-formed typing environments \mathcal{G} , \mathcal{C} , \mathcal{R} , \mathcal{L} and \mathcal{L}_C (\mathcal{L}_A , \mathcal{L}_{B0} or \mathcal{L}_{B1}), the expression e is well-typed and has the type A .
- $\mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_A, \mathcal{P} \vdash e : A$, implies that,
under the well-formed typing environments \mathcal{G} , \mathcal{C} , \mathcal{R} , \mathcal{L} , \mathcal{L}_A and \mathcal{P} , the expression e is well-typed and has the type A .
- $\mathcal{S} \vdash D$, implies that,
under the the well-formed typing environment \mathcal{S} , the parser component D is well-typed. Here, \mathcal{S} can be \emptyset , \mathcal{G} , or \mathcal{C} .
- $\mathcal{G}, \mathcal{C} \vdash D$, implies that,
under the well-formed typing environments \mathcal{G} and \mathcal{C} , the parser component D is well-typed.
- $\mathcal{G}, \mathcal{C}, \mathcal{R} \vdash D$, implies that,
under the well-formed typing environments \mathcal{G} , \mathcal{C} and \mathcal{R} , the parser component D is well-typed.
- $\mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L} \vdash D$, implies that
under the well-formed typing environments \mathcal{G} , \mathcal{C} , \mathcal{R} and \mathcal{L} , the parser component D is well-typed.
- $\mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_C \vdash D$, implies that
under the well-formed typing environments \mathcal{G} , \mathcal{C} , \mathcal{R} , \mathcal{L} and \mathcal{L}_C (\mathcal{L}_A , \mathcal{L}_{B0} or \mathcal{L}_{B1}), the parser component D is well-typed.
- $\mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_A, \mathcal{P} \vdash D$, implies that
under the well-formed typing environments \mathcal{G} , \mathcal{C} , \mathcal{R} , \mathcal{L} , \mathcal{L}_A and \mathcal{P} , the parser component D is well-typed.

5.1.4 Typing rules

- Common

$$\frac{}{\emptyset \vdash \diamond} \text{ (C-1)} \qquad \frac{\mathcal{E} \vdash \diamond \quad x : A \in \mathcal{E}}{\mathcal{E} \vdash x : A} \text{ (C-2)}$$

$$\frac{\mathcal{E}' \vdash \diamond \quad x \notin \text{dom}(\mathcal{E}') \quad \mathcal{E} = \mathcal{E}' \cup \{x : A\}}{\mathcal{E} \vdash \diamond} \text{ (C-3)}$$

$$\frac{\mathcal{E}' \vdash e : A \quad y \notin \text{dom}(\mathcal{E}') \quad \mathcal{E} = \mathcal{E}' \cup \{y : A'\}}{\mathcal{E} \vdash e : A} \text{ (C-4)}$$

$$\frac{\mathcal{G} \vdash \diamond \quad \mathcal{C} \vdash e : A}{\mathcal{G}, \mathcal{C} \vdash e : A} \text{ (C-5)} \quad \frac{\mathcal{G} \vdash \diamond \quad \mathcal{C} \vdash \diamond \quad \mathcal{R} \vdash e : A}{\mathcal{G}, \mathcal{C}, \mathcal{R} \vdash e : A} \text{ (C-6)}$$

- Initialization of \mathcal{G} , opened at the beginning of the specification and not to be closed

$$\frac{\mathcal{G} = (\mathcal{L}reglen, \mathcal{C}reglen, \mathcal{P}set, \mathcal{L}set) \quad \mathcal{L}reglen = k \quad k > 0}{\mathcal{G} \vdash Lreglen(k)} \text{ (IG-1)}$$

$$\frac{\mathcal{G} = (\mathcal{L}reglen, \mathcal{C}reglen, \mathcal{P}set, \mathcal{L}set) \quad \mathcal{C}reglen = k \quad k > 0}{\mathcal{G} \vdash Creglen(k)} \text{ (IG-2)}$$

$$\frac{\mathcal{G} = (\mathcal{L}reglen, \mathcal{C}reglen, \mathcal{P}set, \mathcal{L}set) \quad \mathcal{P}set = \{id_1, \dots, id_k\} \quad \forall i, j (1 \leq i, j \leq k \rightarrow id_i \neq id_j)}{\mathcal{G} \vdash Pset(id_1, \dots, id_k)} \text{ (IG-3)}$$

$$\frac{\mathcal{G} = (\mathcal{L}reglen, \mathcal{C}reglen, \mathcal{P}set, \mathcal{L}set) \quad \mathcal{L}set = \{id_1, \dots, id_k\} \quad \forall i, j (1 \leq i, j \leq k \rightarrow id_i \neq id_j)}{\mathcal{G} \vdash Lset(id_1, \dots, id_k)} \text{ (IG-4)}$$

$$\frac{\begin{array}{l} \mathcal{G} = (\mathcal{L}reglen, \mathcal{C}reglen, \mathcal{P}set, \mathcal{L}set) \\ \mathcal{L}reglen = k \quad \mathcal{G} \vdash Lreglen(k) \quad \mathcal{C}reglen = k' \\ \mathcal{G} \vdash Creglen(k') \quad \mathcal{P}set = \{pid_1, \dots, pid_p\} \quad \mathcal{G} \vdash Pset(pid_1, \dots, pid_p) \\ \mathcal{L}set = \{lid_1, \dots, lid_l\} \quad \mathcal{G} \vdash Lset(lid_1, \dots, lid_l) \end{array}}{\mathcal{G} \vdash \diamond} \text{ (IG-5)}$$

- Initialization of \mathcal{C} , opened at the beginning of the specification and not to be closed

$$\frac{\mathcal{C}' \vdash c : (\tau, n) \quad id \notin dom(\mathcal{C}') \quad \mathcal{C} = \mathcal{C}' \cup \{id : (\tau, n)\}}{\mathcal{C} \vdash ConstDcl(id, c)} \text{ (IC-1)}$$

$$\frac{\text{val}(i) \text{ is a signed integer up to 32 bits}}{\emptyset \vdash \text{IntConst}(i) : (\text{Int}, \text{val}(i))} \text{ (IC-2)}$$

$$\frac{\text{val}(i) \text{ is the decimal result from a hexadecimal number } i \text{ (with } n \text{ hexadecimal digits)}}{\emptyset \vdash \text{HexConst}(i) : (\text{Hexes}(n), \text{val}(i))} \text{ (IC-3)}$$

$$\frac{\text{val}(bs) \text{ is the non negtive integer from a binary bit string } bs \text{ with the length } n}{\emptyset \vdash \text{BitSConst}(bs) : (\text{Bits}(n), \text{val}(bs))} \text{ (IC-4)}$$

- Initialization of \mathcal{R} , initialized at the beginning of the specification (Rules IR-1 and IR-2) and each time at the leaving of a layer context (Rule IR-3), and opened at the beginning of a layer context.

$$\frac{\begin{array}{c} \mathcal{G} \vdash \text{Lreglen}(n) \quad \mathcal{G}, \mathcal{C} \vdash e_1 : (\text{Int}, n_1) \\ \mathcal{G}, \mathcal{C} \vdash e_2 : (\text{Int}, n_2) \quad 0 \leq n_2 \leq n_1 < n \quad id \notin \text{dom}(\mathcal{R}') \\ \forall id' \in \text{dom}(\mathcal{R}'). (\mathcal{G}, \mathcal{C}, \mathcal{R}' \vdash id' : \text{RegAcc}(n, n'_1, n'_2) \rightarrow n'_1 < n_2 \vee n_1 < n'_2) \\ \mathcal{R} = \mathcal{R}' \cup \{id : \text{RegAcc}(n, n_1, n_2)\} \end{array}}{\mathcal{G}, \mathcal{C}, \mathcal{R} \vdash \text{IRF}(id, e_1, e_2)} \text{ (IR-1)}$$

$$\frac{\begin{array}{c} \mathcal{G} \vdash \text{Lreglen}(n) \quad \mathcal{G}, \mathcal{C} \vdash e : (\text{Int}, k) \quad 0 \leq k < n \quad id \notin \text{dom}(\mathcal{R}') \\ \forall id' \in \text{dom}(\mathcal{R}'). (\mathcal{G}, \mathcal{C}, \mathcal{R}' \vdash id' : \text{RegAcc}(n, n'_1, n'_2) \rightarrow n'_1 < k \vee k < n'_2) \\ \mathcal{R} = \mathcal{R}' \cup \{id : \text{RegAcc}(n, k, k)\} \end{array}}{\mathcal{G}, \mathcal{C}, \mathcal{R} \vdash \text{IRF}(id, e)} \text{ (IR-2)}$$

$$\frac{\begin{array}{c} \mathcal{G} \vdash \text{Lreglen}(n) \quad \mathcal{G} \vdash \text{Creglen}(k) \quad n = 3 * k \\ \mathcal{R} = \{id : \text{RegAcc}(n, 2 * k + n_1, 2 * k + n_2) \mid id : \text{RegAcc}(k, n_1, n_2) \in \mathcal{L}_A\} \\ \cup \{id : \text{RegAcc}(n, k + n_1, k + n_2) \mid id : \text{RegAcc}(k, n_1, n_2) \in \mathcal{L}_{B0}\} \\ \cup \{id : \text{RegAcc}(n, n_1, n_2) \mid id : \text{RegAcc}(k, n_1, n_2) \in \mathcal{L}_{B1}\} \end{array}}{\mathcal{R} \vdash \diamond} \text{ (IR-3)}$$

- Initialization of \mathcal{L} , opened at the beginning and closed at the end of a LayerAction specification

$$\frac{\begin{array}{c} \mathcal{G}, \mathcal{C}, \mathcal{R} \vdash \text{ProtocolDecl}(pid, protocol) \\ \mathcal{L}' \vdash \diamond \quad id_i \notin \text{dom}(\mathcal{L}'), 1 \leq i \leq k \quad \mathcal{L} = \mathcal{L}' \cup \{id_i : pid \mid 1 \leq i \leq k\} \end{array}}{\mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L} \vdash \text{ProtocolDef}(pid, (id_1, \dots, id_k))} \text{ (IL)}$$

- Initialization of \mathcal{L}_A at the CellA Registers specification, opened at the beginning and closed at the end of a Cell A specification

$$\begin{array}{c}
\mathcal{G} \vdash \text{Creglen}(n) \\
\mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_A' \vdash e_1 : (Int, n_1) \quad \mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_A' \vdash e_2 : (Int, n_2) \\
0 \leq n_2 \leq n_1 < n \quad id \notin \text{dom}(\mathcal{L}_A') \cup \text{dom}(\mathcal{R}) \\
\forall id' \in \text{dom}(\mathcal{L}_A'). (\mathcal{L}_A' \vdash id' : \text{RegAcc}(n, n_1', n_2') \rightarrow n_1' < n_2 \vee n_1 < n_2') \\
\forall id' \in \text{dom}(\mathcal{R}). (\mathcal{R} \vdash id' : \text{RegAcc}(n, n_1', n_2') \rightarrow n_1' < 2 * n + n_2 \vee 2 * n + n_1 < n_2') \\
\mathcal{L}_A = \mathcal{L}_A' \cup \{id : \text{RegAcc}(n, n_1, n_2)\} \\
\hline
\mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_A \vdash \text{IRF}(id, e_1, e_2) \quad (\text{ILA-1})
\end{array}$$

$$\begin{array}{c}
\mathcal{G} \vdash \text{Creglen}(n) \\
\mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_A' \vdash e : (Int, k) \quad 0 \leq k < n \quad id \notin \text{dom}(\mathcal{L}_A') \cup \text{dom}(\mathcal{R}) \\
\forall id' \in \text{dom}(\mathcal{L}_A'). (\mathcal{L}_A' \vdash id' : \text{RegAcc}(n, n_1', n_2') \rightarrow n_1' < k \vee k < n_2') \\
\forall id' \in \text{dom}(\mathcal{R}). (\mathcal{R} \vdash id' : \text{RegAcc}(n, n_1', n_2') \rightarrow n_1' < 2 * n + k \vee 2 * n + k < n_2') \\
\mathcal{L}_A = \mathcal{L}_A' \cup \{id : \text{RegAcc}(n, k, k)\} \\
\hline
\mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_A \vdash \text{IRF}(id, e) \quad (\text{ILA-2})
\end{array}$$

- Initialization of \mathcal{L}_{B0} at the CellB0 Registers specification, opened at the beginning and closed at the end of a Cell B0 specification

$$\begin{array}{c}
\mathcal{G} \vdash \text{Creglen}(n) \\
\mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}'_{B0} \vdash e_1 : (Int, n_1) \quad \mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}'_{B0} \vdash e_2 : (Int, n_2) \\
0 \leq n_2 \leq n_1 < n \quad id \notin \text{dom}(\mathcal{L}'_{B0}) \cup \text{dom}(\mathcal{R}) \\
\forall id' \in \text{dom}(\mathcal{L}'_{B0}). (\mathcal{L}'_{B0} \vdash id' : \text{RegAcc}(n, n_1', n_2') \rightarrow n_1' < n_2 \vee n_1 < n_2') \\
\forall id' \in \text{dom}(\mathcal{R}). (\mathcal{R} \vdash id' : \text{RegAcc}(n, n_1', n_2') \rightarrow n_1' < n + n_2 \vee n + n_1 < n_2') \\
\mathcal{L}_{B0} = \mathcal{L}'_{B0} \cup \{id : \text{RegAcc}(n, n_1, n_2)\} \\
\hline
\mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_{B0} \vdash \text{IRF}(id, e_1, e_2) \quad (\text{ILB0-1})
\end{array}$$

$$\begin{array}{c}
\mathcal{G} \vdash \text{Creglen}(n) \\
\mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}'_{B0} \vdash e : (Int, k) \quad 0 \leq k < n \quad id \notin \text{dom}(\mathcal{L}'_{B0}) \cup \text{dom}(\mathcal{R}) \\
\forall id' \in \text{dom}(\mathcal{L}'_{B0}). (\mathcal{L}'_{B0} \vdash id' : \text{RegAcc}(n, n_1', n_2') \rightarrow n_1' < k \vee k < n_2') \\
\forall id' \in \text{dom}(\mathcal{R}). (\mathcal{R} \vdash id' : \text{RegAcc}(n, n_1', n_2') \rightarrow n_1' < n + k \vee n + k < n_2') \\
\mathcal{L}_{B0} = \mathcal{L}'_{B0} \cup \{id : \text{RegAcc}(n, k, k)\} \\
\hline
\mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_{B0} \vdash \text{IRF}(id, e) \quad (\text{ILB0-2})
\end{array}$$

- Initialization of \mathcal{L}_{B1} at the CellB1 Registers specification, opened at the beginning and closed at the end of a Cell B1 specification

$$\begin{array}{c}
\mathcal{G} \vdash \text{Creglen}(n) \\
\mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}'_{B1} \vdash e_1 : (Int, n_1) \quad \mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}'_{B1} \vdash e_2 : (Int, n_2) \\
0 \leq n_2 \leq n_1 < n \quad id \notin \text{dom}(\mathcal{L}'_{B1}) \cup \text{dom}(\mathcal{R}) \\
\forall id' \in \text{dom}(\mathcal{L}'_{B1}). (\mathcal{L}'_{B1} \vdash id' : \text{RegAcc}(n, n'_1, n'_2) \rightarrow n'_1 < n_2 \vee n_1 < n'_2) \\
\forall id' \in \text{dom}(\mathcal{R}). (\mathcal{R} \vdash id' : \text{RegAcc}(n, n'_1, n'_2) \rightarrow n'_1 < n_2 \vee n_1 < n'_2) \\
\mathcal{L}_{B1} = \mathcal{L}'_{B1} \cup \{id : \text{RegAcc}(n, n_1, n_2)\} \\
\hline
\mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_{B1} \vdash \text{IRF}(id, e_1, e_2) \quad (\text{ILB1-1})
\end{array}$$

$$\begin{array}{c}
\mathcal{G} \vdash \text{Creglen}(n) \\
\mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}'_{B1} \vdash e : (Int, k) \quad 0 \leq k < n \quad id \notin \text{dom}(\mathcal{L}'_{B1}) \cup \text{dom}(\mathcal{R}) \\
\forall id' \in \text{dom}(\mathcal{L}'_{B1}). (\mathcal{L}'_{B1} \vdash id' : \text{RegAcc}(n, n'_1, n'_2) \rightarrow n'_1 < k \vee k < n'_2) \\
\forall id' \in \text{dom}(\mathcal{R}). (\mathcal{R} \vdash id' : \text{RegAcc}(n, n'_1, n'_2) \rightarrow n'_1 < k \vee k < n'_2) \\
\mathcal{L}_{B1} = \mathcal{L}'_{B1} \cup \{id : \text{RegAcc}(n, k, k)\} \\
\hline
\mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_{B1} \vdash \text{IRF}(id, e) \quad (\text{ILB1-2})
\end{array}$$

- Initialization of \mathcal{P} , opened at each time of the instantiation of a Protocol specification and closed at the end of that instantiation.

$$\begin{array}{c}
fids = ((fid_1 : c_1), \dots, (fid_k : c_k)) \\
ofid = (ofid : 0) \quad \forall i : 1 \leq i \leq k. (\emptyset \vdash c_i : (Int, n_i)) \\
n = n_1 + n_2 + \dots + n_k \quad \forall i (1 \leq i \leq k \rightarrow n_i > 0) \\
\forall i, j (1 \leq i < j \leq k \rightarrow fid_i \neq fid_j) \quad \forall i. (1 \leq i \leq k \rightarrow fid_i \neq ofid) \\
\mathcal{G} \vdash \diamond \quad \mathcal{C} \vdash \diamond \quad \mathcal{R} \vdash \diamond \quad \mathcal{L} \vdash \diamond \quad \mathcal{L}_A \vdash \diamond \\
\mathcal{P}' \vdash \diamond \quad \forall i (1 \leq i \leq k \rightarrow fid_i \notin \text{dom}(\mathcal{P}')) \quad ofid \notin \text{dom}(\mathcal{P}') \\
\mathcal{P} = \mathcal{P}' \cup \{fid_i : \text{FieldAcc}(n, n_1 + \dots + n_{i-1}, n_1 + \dots + n_i - 1) \mid 1 \leq i \leq k\} \\
\cup \{ofid : \text{FieldAcc}(n, n, null)\} \\
\hline
\mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_A, \mathcal{P} \vdash (\text{Fields}(fids), \text{OptionFields}(ofid)) \quad (\text{IP-1})
\end{array}$$

- Expressions

$$\frac{\mathcal{C} \vdash \diamond \quad \mathcal{R} \vdash \diamond \quad \frac{\mathcal{C} \vdash c : (\tau, n) \quad \mathcal{G} \vdash \diamond}{\mathcal{L} \vdash \diamond} \quad \mathcal{L}_C \vdash \diamond \quad \mathcal{L}_C \text{ is } \mathcal{L}_A, \mathcal{L}_{B0} \text{ or } \mathcal{L}_{B1}}{\mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_C \vdash Econst(c) : (\tau, n)} \text{ CE-1}$$

$$\frac{\mathcal{G} \vdash \diamond \quad \mathcal{C} \vdash \diamond \quad \mathcal{R} \vdash \diamond \quad \frac{\mathcal{C} \vdash c : (\tau, n)}{\mathcal{L} \vdash \diamond} \quad \mathcal{L}_A \vdash \diamond \quad \mathcal{P} \vdash \diamond}{\mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_A, \mathcal{P} \vdash Econst(c) : (\tau, n)} \text{ CE-2}$$

$$\frac{\mathcal{C} \vdash c : (\tau, n) \quad \mathcal{G} \vdash \diamond}{\mathcal{G}, \mathcal{C} \vdash Econst(c) : (\tau, n)} \text{ CE-3}$$

$$\frac{\mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_C \vdash e : (\tau, m) \quad n = trans_to_int(\tau, m) \quad \mathcal{L}_C \text{ is } \mathcal{L}_A, \mathcal{L}_{B0} \text{ or } \mathcal{L}_{B1}}{\mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_C \vdash Eunop(Oint, e) : (Int, n)} \text{ OINT-1}$$

$$\frac{\mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_A, \mathcal{P} \vdash e : (\tau, m) \quad n = trans_to_int(\tau, m)}{\mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_A, \mathcal{P} \vdash Eunop(Oint, e) : (Int, n)} \text{ OINT-2}$$

$$\frac{\mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_C \vdash e : Bool \quad \mathcal{L}_C \text{ is } \mathcal{L}_A, \mathcal{L}_{B0} \text{ or } \mathcal{L}_{B1}}{\mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_C \vdash Eunop(Onot, e) : Bool} \text{ ONOT-1}$$

$$\frac{\mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_A, \mathcal{P} \vdash e : Bool}{\mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_A, \mathcal{P} \vdash Eunop(Onot, e) : Bool} \text{ ONOT-2}$$

$$\frac{\mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_C \vdash e : (Bits(n), bs) \quad bs' = bit_wise_negation(bs) \quad \mathcal{L}_C \text{ is } \mathcal{L}_A, \mathcal{L}_{B0} \text{ or } \mathcal{L}_{B1}}{\mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_C \vdash Eunop(Oneg, e) : (Bits(n), bs')} \text{ ONEG-1}$$

$$\frac{\mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_A, \mathcal{P} \vdash e : (Bits(n), bs) \quad bs' = bit_wise_negation(bs)}{\mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_A, \mathcal{P} \vdash Eunop(Oneg, e) : (Bits(n), bs')} \text{ ONEG-2}$$

$$\begin{array}{c}
\mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_C \vdash e_1 : (\tau_1, m_1) \quad \mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_C \vdash e_2 : (\tau_2, m_2) \\
binop \in \{Oadd, Osub, Omul, Odivint, Omod\} \\
n = do_binop(binop, trans_to_int(\tau_1, m_1), trans_to_int(\tau_2, m_2)) \\
\mathcal{L}_C \text{ is } \mathcal{L}_A, \mathcal{L}_{B0} \text{ or } \mathcal{L}_{B1} \\
\hline
\mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_C \vdash Ebinop(binop, e_1, e_2) : (Int, n)
\end{array} \text{ BOPA-1}$$

$$\begin{array}{c}
\mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_A, \mathcal{P} \vdash e_1 : (\tau_1, m_1) \quad \mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_A, \mathcal{P} \vdash e_2 : (\tau_2, m_2) \\
binop \in \{Oadd, Osub, Omul, Odivint, Omod\} \\
n = do_binop(binop, trans_to_int(\tau_1, m_1), trans_to_int(\tau_2, m_2)) \\
\hline
\mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_A, \mathcal{P} \vdash Ebinop(binop, e_1, e_2) : (Int, n)
\end{array} \text{ BOPA-2}$$

$$\begin{array}{c}
\mathcal{G}, \mathcal{C} \vdash e_1 : (\tau_1, m_1) \\
\mathcal{G}, \mathcal{C} \vdash e_2 : (\tau_2, m_2) \quad binop \in \{Oadd, Osub, Omul, Odivint, Omod\} \\
n = do_binop(binop, trans_to_int(\tau_1, m_1), trans_to_int(\tau_2, m_2)) \\
\hline
\mathcal{G}, \mathcal{C} \vdash Ebinop(binop, e_1, e_2) : (Int, n)
\end{array} \text{ BOPA-3}$$

$$\begin{array}{c}
\mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_C \vdash e_1 : Bool \quad \mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_C \vdash e_2 : Bool \\
binop \in \{Oand, Oor\} \quad \mathcal{L}_C \text{ is } \mathcal{L}_A, \mathcal{L}_{B0} \text{ or } \mathcal{L}_{B1} \\
\hline
\mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_C \vdash Ebinop(binop, e_1, e_2) : Bool
\end{array} \text{ BOPL-1}$$

$$\begin{array}{c}
\mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_A, \mathcal{P} \vdash e_1 : Bool \\
\mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_A, \mathcal{P} \vdash e_2 : Bool \quad binop \in \{Oand, Oor\} \\
\hline
\mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_A, \mathcal{P} \vdash Ebinop(binop, e_1, e_2) : Bool
\end{array} \text{ BOPL-2}$$

$$\begin{array}{c}
\mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_C \vdash e_1 : (Bits(n), bs_1) \\
\mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_C \vdash e_2 : (Bits(n), bs_2) \quad binop \in \{Oband, Obor, Obeor\} \\
bs = bit_wise_operation(binop, bs_1, bs_2) \quad \mathcal{L}_C \text{ is } \mathcal{L}_A, \mathcal{L}_{B0} \text{ or } \mathcal{L}_{B1} \\
\hline
\mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_C \vdash Ebinop(binop, e_1, e_2) : (Bits(n), bs)
\end{array} \text{ BOPB-1}$$

$$\begin{array}{c}
\mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_A, \mathcal{P} \vdash e_1 : (Bits(n), bs_1) \\
\mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_A, \mathcal{P} \vdash e_2 : (Bits(n), bs_2) \quad binop \in \{Oband, Obor, Obeor\} \\
bs = bit_wise_operation(binop, bs_1, bs_2) \\
\hline
\mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_A, \mathcal{P} \vdash Ebinop(binop, e_1, e_2) : (Bits(n), bs)
\end{array} \text{ BOPB-2}$$

$$\frac{\mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_C \vdash e_1 : \tau \quad \mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_C \vdash e_2 : \tau \quad \text{binop} \in \{Oeq, One, Olt, Ogt, Ole, Oge\} \quad \mathcal{L}_C \text{ is } \mathcal{L}_A, \mathcal{L}_{B0} \text{ or } \mathcal{L}_{B1}}{\mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_C \vdash Ebinop(binop, e_1, e_2) : Bool} \text{BOPR-1}$$

$$\frac{\mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_A, \mathcal{P} \vdash e_1 : \tau \quad \mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_A, \mathcal{P} \vdash e_2 : \tau \quad \text{binop} \in \{Oeq, One, Olt, Ogt, Ole, Oge\}}{\mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_A, \mathcal{P} \vdash Ebinop(binop, e_1, e_2) : Bool} \text{BOPR-2}$$

$$\frac{\mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_C \vdash e_1 : \tau \quad \mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_C \vdash e_2 : Int \quad \text{binop} \in \{Osl, Osr\} \quad \mathcal{L}_C \text{ is } \mathcal{L}_A, \mathcal{L}_{B0} \text{ or } \mathcal{L}_{B1}}{\mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_C \vdash Ebinop(binop, e_1, e_2) : \tau} \text{BOPS-1}$$

$$\frac{\mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_A, \mathcal{P} \vdash e_1 : \tau \quad \mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_A, \mathcal{P} \vdash e_2 : Int \quad \text{binop} \in \{Osl, Osr\}}{\mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_A, \mathcal{P} \vdash Ebinop(binop, e_1, e_2) : \tau} \text{BOPS-2}$$

$$\frac{\mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_C \vdash e_1 : Bits(n_1) \quad \mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_C \vdash e_2 : Bits(n_2) \quad n = n_1 + n_2 \quad \mathcal{L}_C \text{ is } \mathcal{L}_A, \mathcal{L}_{B0} \text{ or } \mathcal{L}_{B1}}{\mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_C \vdash Ebinop(Obc, e_1, e_2) : Bits(n)} \text{BOPC-1}$$

$$\frac{\mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_A, \mathcal{P} \vdash e_1 : Bits(n_1) \quad \mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_A, \mathcal{P} \vdash e_2 : Bits(n_2) \quad n = n_1 + n_2}{\mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_A, \mathcal{P} \vdash Ebinop(Obc, e_1, e_2) : Bits(n)} \text{BOPC-1'}$$

$$\frac{\mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_C \vdash e_1 : Hexes(n_1) \quad \mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_C \vdash e_2 : Hexes(n_2) \quad n = n_1 + n_2 \quad \mathcal{L}_C \text{ is } \mathcal{L}_A, \mathcal{L}_{B0} \text{ or } \mathcal{L}_{B1}}{\mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_C \vdash Ebinop(Obc, e_1, e_2) : Hexes(n)} \text{BOPC-2}$$

$$\frac{\mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_A, \mathcal{P} \vdash e_1 : Hexes(n_1) \quad \mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_A, \mathcal{P} \vdash e_2 : Hexes(n_2) \quad n = n_1 + n_2}{\mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_A, \mathcal{P} \vdash Ebinop(Obc, e_1, e_2) : Hexes(n)} \text{BOPC-2'}$$

$$\frac{\begin{array}{l} \mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_C \vdash e_1 : \text{RegAcc}(k, n_1, n_2) \\ \mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_C \vdash e_2 : \text{RegAcc}(k, m_1, m_2) \quad n_2 = m_1 + 1 \\ 0 \leq m_2 \leq m_1 < n_2 \leq n_1 < k \quad \mathcal{L}_C \text{ is } \mathcal{L}_A, \mathcal{L}_{B0} \text{ or } \mathcal{L}_{B1} \end{array}}{\mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_C \vdash \text{Ebinop}(\text{Obc}, e_1, e_2) : \text{RegAcc}(k, n_1, m_2)} \text{BOPC-3}$$

$$\frac{\begin{array}{l} \mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_A, \mathcal{P} \vdash e_1 : \text{RegAcc}(k, n_1, n_2) \\ \mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_A, \mathcal{P} \vdash e_2 : \text{RegAcc}(k, m_1, m_2) \\ n_2 = m_1 + 1 \quad 0 \leq m_2 \leq m_1 < n_2 \leq n_1 < k \end{array}}{\mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_A, \mathcal{P} \vdash \text{Ebinop}(\text{Obc}, e_1, e_2) : \text{RegAcc}(k, n_1, m_2)} \text{BOPC-3'}$$

$$\frac{\begin{array}{l} \mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_C \vdash e_1 : \text{FieldAcc}(\text{id}, k, n_1, n_2) \\ \mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_C \vdash e_2 : \text{FieldAcc}(\text{id}, k, m_1, m_2) \quad m_1 = n_2 + 1 \\ 0 \leq n_1 \leq n_2 < m_1 \leq m_2 < k \quad \mathcal{L}_C \text{ is } \mathcal{L}_A, \mathcal{L}_{B0} \text{ or } \mathcal{L}_{B1} \end{array}}{\mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_C \vdash \text{Ebinop}(\text{Obc}, e_1, e_2) : \text{FieldAcc}(\text{id}, k, n_1, m_2)} \text{BOPC-4}$$

$$\frac{\begin{array}{l} \mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_A, \mathcal{P} \vdash e_1 : \text{FieldAcc}(k, n_1, n_2) \\ \mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_A, \mathcal{P} \vdash e_2 : \text{FieldAcc}(k, m_1, m_2) \\ m_1 = n_2 + 1 \quad 0 \leq n_1 \leq n_2 < m_1 \leq m_2 < k \end{array}}{\mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_A, \mathcal{P} \vdash \text{Ebinop}(\text{Obc}, e_1, e_2) : \text{FieldAcc}(k, n_1, m_2)} \text{BOPC-4'}$$

$$\frac{\begin{array}{l} \mathcal{G}, \mathcal{C}, \mathcal{L}, \mathcal{L}_C \vdash e_1 : (\tau, m) \quad \mathcal{G}, \mathcal{C}, \mathcal{L}, \mathcal{L}_C \vdash e_2 : (\text{Int}, n) \\ n \geq \text{num_of_digits}(\text{trans_to_hex}(\tau, m)) \quad \mathcal{L}_C \text{ is } \mathcal{L}_A, \mathcal{L}_{B0} \text{ or } \mathcal{L}_{B1} \end{array}}{\mathcal{G}, \mathcal{C}, \mathcal{L}, \mathcal{L}_C \vdash \text{Ebinop}(\text{Ohexes}, e_1, e_2) : \text{Hexes}(n)} \text{BOPH-1}$$

$$\frac{\begin{array}{l} \mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_A, \mathcal{P} \vdash e_1 : (\tau, m) \quad \mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_A, \mathcal{P} \vdash e_2 : (\text{Int}, n) \\ n \geq \text{num_of_digits}(\text{trans_to_hex}(\tau, m)) \end{array}}{\mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_A, \mathcal{P} \vdash \text{Ebinop}(\text{Ohexes}, e_1, e_2) : \text{Hexes}(n)} \text{BOPH-2}$$

$$\frac{\begin{array}{l} \mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_C \vdash e_1 : (\tau, m) \quad \mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_C \vdash e_2 : (\text{Int}, n) \\ n \geq \text{num_of_bits}(\text{trans_to_binary_number}(\tau, m)) \\ \mathcal{L}_C \text{ is } \mathcal{L}_A, \mathcal{L}_{B0} \text{ or } \mathcal{L}_{B1} \end{array}}{\mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_C \vdash \text{Ebinop}(\text{Obits}, e_1, e_2) : \text{Bits}(n)} \text{BOPBT-1}$$

$$\frac{\begin{array}{l} \mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_A, \mathcal{P} \vdash e_1 : (\tau, m) \quad \mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_A, \mathcal{P} \vdash e_2 : (\text{Int}, n) \\ n \geq \text{num_of_bits}(\text{trans_to_binary_number}(\tau, m)) \end{array}}{\mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_A, \mathcal{P} \vdash \text{Ebinop}(\text{Obits}, e_1, e_2) : \text{Bits}(n)} \text{BOPBT-2}$$

$$\begin{array}{c}
\mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L} \vdash id : pid \\
\mathcal{G}, \mathcal{C}, \mathcal{R} \vdash ProtocolDecl(pid, Protocol(Fields(flds), OptionFields(oflds)), \dots) \\
\quad flds = ((fid_1 : c_1), \dots, (fid_k : c_k)) \\
\quad ofld = (ofld : null) \quad \forall i : 1 \leq i \leq k. (\emptyset \vdash c_i : (Int, n_i)) \\
\quad n = n_1 + n_2 + \dots + n_k \quad \exists i. fid = fid_i \quad \mathcal{L}_C \text{ is } \mathcal{L}_A, \mathcal{L}_{B0} \text{ or } \mathcal{L}_{B1} \\
\hline
\mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_C \vdash Efield(id, fid) : FieldAcc(id, n, n_1 + \dots + n_{i-1}, n_1 + \dots + n_i - 1) \quad \text{EFIELD}
\end{array}$$

$$\begin{array}{c}
\mathcal{G} \vdash Creglen(n) \\
\mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_C \vdash e_1 : RegAcc(n, n_1, n_2) \quad \mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_C \vdash e_2 : (Int, n') \\
0 \leq n_2 \leq n_1 < n \quad 0 \leq n' \leq n_1 - n_2 \quad \mathcal{L}_C \text{ is } \mathcal{L}_A, \mathcal{L}_{B0} \text{ or } \mathcal{L}_{B1} \\
\hline
\mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_C \vdash EFieldBit(e_1, e_2) : RegAcc(n, n_2 + n', n_2 + n') \quad \text{FB-1}
\end{array}$$

$$\begin{array}{c}
\mathcal{G} \vdash Creglen(n) \quad \mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_A, \mathcal{P} \vdash e_1 : RegAcc(n, n_1, n_2) \\
\mathcal{G}, \mathcal{C}, \mathcal{G}, \mathcal{R}, \mathcal{L}, \mathcal{L}_A, \mathcal{P} \vdash e_2 : (Int, n') \\
0 \leq n_2 \leq n_1 < n \quad 0 \leq n' \leq n_1 - n_2 \\
\hline
\mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_A, \mathcal{P} \vdash EFieldBit(e_1, e_2) : RegAcc(n, n_2 + n', n_2 + n') \quad \text{FB-1}'
\end{array}$$

$$\begin{array}{c}
\mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_C \vdash e_1 : FieldAcc(id, n, n_1, n_2) \\
\mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_C \vdash e_2 : (Int, n') \\
0 \leq n_1 \leq n_2 < n \quad 0 \leq n' \leq n_2 - n_1 \quad \mathcal{L}_C \text{ is } \mathcal{L}_A, \mathcal{L}_{B0} \text{ or } \mathcal{L}_{B1} \\
\hline
\mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_C \vdash EFieldBit(e_1, e_2) : FieldAcc(id, n, n_1 + n', n_1 + n') \quad \text{FB-2}
\end{array}$$

$$\begin{array}{c}
\mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_A, \mathcal{P} \vdash e_1 : FieldAcc(n, n_1, n_2) \\
\mathcal{G}, \mathcal{C}, \mathcal{G}, \mathcal{R}, \mathcal{L}, \mathcal{L}_A, \mathcal{P} \vdash e_2 : (Int, n') \\
0 \leq n_1 \leq n_2 < n \quad 0 \leq n' \leq n_2 - n_1 \\
\hline
\mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_A, \mathcal{P} \vdash EFieldBit(e_1, e_2) : FieldAcc(n, n_1 + n', n_1 + n') \quad \text{FB-2}'
\end{array}$$

$$\frac{\begin{array}{c} \mathcal{G} \vdash \text{Creglen}(n) \quad \mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_C \vdash e_1 : \text{RegAcc}(n, n_1, n_2) \\ \mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_C \vdash e_2 : (\text{Int}, n') \quad \mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_C \vdash e_3 : (\text{Int}, n'') \\ 0 \leq n_2 \leq n_1 < n \quad 0 \leq n'' \leq n' \leq n_1 - n_2 \quad \mathcal{L}_C \text{ is } \mathcal{L}_A, \mathcal{L}_{B0} \text{ or } \mathcal{L}_{B1} \end{array}}{\mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_C \vdash \text{EFieldSection}(e_1, e_2, e_3) : \text{RegAcc}(n, n_2 + n'', n_2 + n')} \text{FS-1}$$

$$\frac{\begin{array}{c} \mathcal{G} \vdash \text{Creglen}(n) \quad \mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_A, \mathcal{P} \vdash e_1 : \text{RegAcc}(n, n_1, n_2) \\ \mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_A, \mathcal{P} \vdash e_2 : (\text{Int}, n') \quad \mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_A, \mathcal{P} \vdash e_3 : (\text{Int}, n'') \\ 0 \leq n_2 \leq n_1 < n \quad 0 \leq n'' \leq n' \leq n_1 - n_2 \end{array}}{\mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_A, \mathcal{P} \vdash \text{EFieldSection}(e_1, e_2, e_3) : \text{RegAcc}(n, n_2 + n'', n_2 + n')} \text{FS-1'}$$

$$\frac{\begin{array}{c} \mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_C \vdash e_1 : \text{FieldAcc}(\text{id}, n, n_1, n_2) \\ \mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_C \vdash e_2 : (\text{Int}, n') \quad \mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_C \vdash e_3 : (\text{Int}, n'') \\ 0 \leq n_1 \leq n_2 < n \quad 0 \leq n'' \leq n' \leq n_2 - n_1 \quad \mathcal{L}_C \text{ is } \mathcal{L}_A, \mathcal{L}_{B0} \text{ or } \mathcal{L}_{B1} \end{array}}{\mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_C \vdash \text{EFieldSection}(e_1, e_2, e_3) : \text{FieldAcc}(\text{id}, n, n_1 + n'', n_1 + n')} \text{FS-2}$$

$$\frac{\begin{array}{c} \mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_A, \mathcal{P} \vdash e_1 : \text{FieldAcc}(n, n_1, n_2) \\ \mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_A, \mathcal{P} \vdash e_2 : (\text{Int}, n') \quad \mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_A, \mathcal{P} \vdash e_3 : (\text{Int}, n'') \\ 0 \leq n_1 \leq n_2 < n \quad 0 \leq n'' \leq n' \leq n_2 - n_1 \end{array}}{\mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_A, \mathcal{P} \vdash \text{EFieldSection}(e_1, e_2, e_3) : \text{FieldAcc}(n, n_1 + n'', n_1 + n')} \text{FS-2'}$$

$$\frac{\mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L} \vdash \text{id} : \text{pid} \quad \mathcal{G}, \mathcal{C}, \mathcal{R} \vdash \text{ProtocolDecl}(\text{pid}, \text{protocol})}{\mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L} \vdash \text{ProtLen}(\text{id}) : \text{Int}} (\text{PLEN})$$

- Instructions

$$\begin{array}{c}
\mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_C \vdash ra : \text{RegAcc}(n', n_1, n_2) \\
\mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_C \vdash e : (\tau, m) \quad \text{trans_to_bits_type}(\tau, m) = (\text{Bits}(n), m) \\
n = n_1 - n_2 + 1 \quad \mathcal{L}_C \text{ is } \mathcal{L}_A, \mathcal{L}_{B0} \text{ or } \mathcal{L}_{B1} \\
\hline
\mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_C \vdash \text{Set}(ra, e) \quad \text{SET-1}
\end{array}$$

$$\begin{array}{c}
\mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_A, \mathcal{P} \vdash ra : \text{RegAcc}(n', n_1, n_2) \\
\mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_A, \mathcal{P} \vdash e : (\tau, m) \\
\text{trans_to_bits}(\tau, m) = (\text{Bits}(n), m) \quad n = n_1 - n_2 + 1 \\
\hline
\mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_A, \mathcal{P} \vdash \text{Set}(ra, e) \quad \text{SET-2}
\end{array}$$

$$\begin{array}{c}
\mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_C \vdash mra : \text{RegAcc}(n', n_1, n_2) \\
m = n_1 - n_2 + 1 \quad \mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_C \vdash e : \tau \\
\tau = \text{Bits}(m) \vee \tau = \text{RegAcc}(n_r, r', r'') \vee \tau = \text{FieldAcc}(id, n_f, f', f'') \\
m = r' - r'' + 1 = f'' - f' + 1 \quad \mathcal{L}_C \text{ is } \mathcal{L}_A, \mathcal{L}_{B0} \text{ or } \mathcal{L}_{B1} \\
\hline
\mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_C \vdash \text{Mov}(mra, e) \quad \text{MOV-1}
\end{array}$$

$$\begin{array}{c}
\mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_A, \mathcal{P} \vdash mra : \text{RegAcc}(n', n_1, n_2) \\
m = n_1 - n_2 + 1 \quad \mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_A, \mathcal{P} \vdash e : \tau \\
\tau = \text{Bits}(m) \vee \tau = \text{RegAcc}(n_r, r', r'') \vee \tau = \text{FieldAcc}(id, n_f, f', f'') \\
m = r' - r'' + 1 = f'' - f' + 1 \\
\hline
\mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_A, \mathcal{P} \vdash \text{Mov}(mra, e) \quad \text{MOV-2}
\end{array}$$

$$\begin{array}{c}
\mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_C \vdash ra : \text{RegAcc}(n', n_1, n_2) \quad \mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_C \vdash e : (\tau, m) \\
\mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_C \vdash e' : (\tau', m') \quad \mathcal{L}_C \text{ is } \mathcal{L}_A, \mathcal{L}_{B0} \text{ or } \mathcal{L}_{B1} \\
\hline
\mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_C \vdash \text{Eq}(ra, e, e') \quad \text{EQ-1}
\end{array}$$

$$\begin{array}{c}
\mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_A, \mathcal{P} \vdash ra : \text{RegAcc}(n', n_1, n_2) \\
\mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_A, \mathcal{P} \vdash e : (\tau, m) \quad \mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_A, \mathcal{P} \vdash e' : (\tau', m') \\
\hline
\mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_A, \mathcal{P} \vdash \text{Eq}(ra, e, e') \quad \text{EQ-2}
\end{array}$$

$$\begin{array}{c}
\mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_C \vdash ra : \text{RegAcc}(n', n_1, n_2) \quad \mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_C \vdash e : (\tau, m) \\
\mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_C \vdash e' : (\tau', m') \quad \mathcal{L}_C \text{ is } \mathcal{L}_A, \mathcal{L}_{B0} \text{ or } \mathcal{L}_{B1} \\
\hline
\mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_C \vdash \text{Lg}(ra, e, e') \quad \text{LG-1}
\end{array}$$

$$\begin{array}{c}
\mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_A, \mathcal{P} \vdash ra : \text{RegAcc}(n', n_1, n_2) \\
\mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_A, \mathcal{P} \vdash e : (\tau, m) \quad \mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_A, \mathcal{P} \vdash e' : (\tau', m') \\
\hline
\mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_A, \mathcal{P} \vdash \text{Lg}(ra, e, e') \quad \text{LG-2}
\end{array}$$

- Access of registers in instructions

$$\frac{\mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_C \vdash id : \text{RegAcc}(n, n_1, n_2) \quad \mathcal{L}_C \text{ is } \mathcal{L}_A, \mathcal{L}_{B0} \text{ or } \mathcal{L}_{B1}}{\mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_C \vdash \text{TargetRegAccName}(id) : \text{RegAcc}(n, n_1, n_2)} \text{TREGACC-1}$$

$$\frac{\mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_A, \mathcal{P} \vdash id : \text{RegAcc}(n, n_1, n_2)}{\mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_A, \mathcal{P} \vdash \text{TargetRegAccName}(id) : \text{RegAcc}(n, n_1, n_2)} \text{TREGACC-1'}$$

$$\frac{\begin{array}{c} \mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_C \vdash \text{tran} : \text{RegAcc}(n, m_1, m_2) \\ \mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_C \vdash e_1 : (\text{Int}, k_1) \\ \mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_C \vdash e_2 : (\text{Int}, k_2) \quad 0 \leq k_2 \leq k_1 \leq m_1 - m_2 \\ n_1 = m_2 + k_1 \quad n_2 = m_2 + k_2 \quad \mathcal{L}_C \text{ is } \mathcal{L}_A, \mathcal{L}_{B0} \text{ or } \mathcal{L}_{B1} \end{array}}{\mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_C \vdash \text{TargetRegAccName}(\text{tran}, e_1, e_2) : \text{RegAcc}(n, n_1, n_2)} \text{TREGACC-2}$$

$$\frac{\begin{array}{c} \mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_A, \mathcal{P} \vdash \text{tran} : \text{RegAcc}(n, m_1, m_2) \\ \mathcal{G}, \mathcal{C}, \mathcal{L}, \mathcal{L}_C \vdash e_1 : (\text{Int}, k_1) \quad \mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_C \vdash e_2 : (\text{Int}, k_2) \\ 0 \leq k_2 \leq k_1 \leq m_1 - m_2 \quad n_1 = m_2 + k_1 \quad n_2 = m_2 + k_2 \end{array}}{\mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_A, \mathcal{P} \vdash \text{TargetRegAccName}(\text{tran}, e_1, e_2) : \text{RegAcc}(n, n_1, n_2)} \text{TREGACC-2'}$$

$$\frac{\begin{array}{c} \mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_C \vdash \text{tran} : \text{RegAcc}(n, m_1, m_2) \quad \mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_C \vdash e : (\text{Int}, k) \\ 0 \leq k \leq m_1 - m_2 \quad m = m_2 + k \quad \mathcal{L}_C \text{ is } \mathcal{L}_A, \mathcal{L}_{B0} \text{ or } \mathcal{L}_{B1} \end{array}}{\mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_C \vdash \text{TargetRegAccName}(\text{tran}, e) : \text{RegAcc}(n, m, m)} \text{TREGACC-3}$$

$$\frac{\begin{array}{c} \mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_A, \mathcal{P} \vdash \text{tran} : \text{RegAcc}(n, m_1, m_2) \\ \mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_C \vdash e : (\text{Int}, k) \quad 0 \leq k \leq m_1 - m_2 \quad m = m_2 + k \end{array}}{\mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_A, \mathcal{P} \vdash \text{TargetRegAccName}(\text{tran}, e) : \text{RegAcc}(n, m, m)} \text{TREGACC-3'}$$

$$\frac{\mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_C \vdash \text{tra} : \text{RegAcc}(n, m_1, m_2) \quad \mathcal{L}_C \text{ is } \mathcal{L}_A, \mathcal{L}_{B0} \text{ or } \mathcal{L}_{B1}}{\mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_C \vdash \text{MovRegAccName}(\text{tra}) : \text{RegAcc}(n, m_1, m_2)} \text{MREGACC-1}$$

$$\frac{\mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_A, \mathcal{P} \vdash \text{tra} : \text{RegAcc}(n, m_1, m_2)}{\mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_A, \mathcal{P} \vdash \text{MovRegAccName}(\text{tra}) : \text{RegAcc}(n, m_1, m_2)} \text{MREGACC-1'}$$

$$\begin{array}{c}
\mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_C \vdash mra : \text{RegAcc}(n, m_1, m_2) \\
\mathcal{G}, \mathcal{C}, \mathcal{L}, \mathcal{L}, \mathcal{L}_C \vdash tra : \text{RegAcc}(n, n_1, n_2) \\
m_2 = n_1 + 1 \quad \mathcal{L}_C \text{ is } \mathcal{L}_A, \mathcal{L}_{B0} \text{ or } \mathcal{L}_{B1} \\
\hline
\mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_C \vdash \text{MovRegAccName}(mra, tra) : \text{RegAcc}(n, m_1, n_2) \quad \text{MREGACC-2}
\end{array}$$

$$\begin{array}{c}
\mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_A, \mathcal{P} \vdash mra : \text{RegAcc}(n, m_1, m_2) \\
\mathcal{G}, \mathcal{C}, \mathcal{L}, \mathcal{L}_A, \mathcal{P} \vdash tra : \text{RegAcc}(n, n_1, n_2) \quad m_2 = n_1 + 1 \\
\hline
\mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_A, \mathcal{P} \vdash \text{MovRegAccName}(mra, tra) : \text{RegAcc}(n, m_1, n_2) \quad \text{MREGACC-2'}
\end{array}$$

- Action statement

$$\begin{array}{c}
\forall i : 1 \leq i \leq k. \mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_C \vdash ins_i \quad \mathcal{L}_C \text{ is } \mathcal{L}_A, \mathcal{L}_{B0} \text{ or } \mathcal{L}_{B1} \\
\hline
\mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_C \vdash \text{Action}(ins_1, \dots, ins_k) \quad \text{AS-1}
\end{array}$$

$$\begin{array}{c}
\forall i : 1 \leq i \leq k. \mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_A, \mathcal{P} \vdash ins_i \\
\hline
\mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_A, \mathcal{P} \vdash \text{Action}(ins_1, \dots, ins_k) \quad \text{AS-2}
\end{array}$$

- Bypass statement

$$\begin{array}{c}
\mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_A \vdash c : (\text{Int}, n) \quad n = 0 \vee n = 1 \vee n = 2 \\
\hline
\mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_A \vdash \text{Bypass}(c) \quad \text{BYP-1}
\end{array}$$

$$\begin{array}{c}
\mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_A, \mathcal{P} \vdash c : (\text{Int}, n) \quad n = 0 \vee n = 1 \vee n = 2 \\
\hline
\mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_A, \mathcal{P} \vdash \text{Bypass}(c) \quad \text{BYP-2}
\end{array}$$

- NextHeader statement

$$\begin{array}{c}
\mathcal{G} \vdash \text{Pset}(id_1, \dots, id_k) \quad id \in \{id_1, \dots, id_k\} \\
\mathcal{G} \vdash \diamond \quad \mathcal{C} \vdash \diamond \quad \mathcal{R} \vdash \diamond \quad \mathcal{L} \vdash \diamond \quad \mathcal{L}_A \vdash \diamond \\
\hline
\mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_A \vdash \text{NextHeader}(id) \quad \text{NEXTHEADER-1}
\end{array}$$

$$\begin{array}{c}
\mathcal{G} \vdash \text{Pset}(id_1, \dots, id_k) \quad id \in \{id_1, \dots, id_k\} \\
\mathcal{G} \vdash \diamond \quad \mathcal{C} \vdash \diamond \quad \mathcal{R} \vdash \diamond \quad \mathcal{L} \vdash \diamond \quad \mathcal{L}_A \vdash \diamond \quad \mathcal{P} \vdash \diamond \\
\hline
\mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_A, \mathcal{P} \vdash \text{NextHeader}(id) \quad \text{NEXTHEADER-2}
\end{array}$$

- Length statement

$$\begin{array}{c}
\mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_A \vdash e : (\text{Int}, n) \\
\hline
\mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_A \vdash \text{Length}(e) \quad \text{LENGTH-1}
\end{array}
\quad
\begin{array}{c}
\mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_A, \mathcal{P} \vdash e : (\text{Int}, n) \\
\hline
\mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_A, \mathcal{P} \vdash \text{Length}(e) \quad \text{LENGTH-2}
\end{array}$$

- Layer statement

$$\begin{array}{c}
\forall i : 1 \leq i \leq n. (ls_i = Action(ins_1, \dots, ins_k) \rightarrow \mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_C \vdash Action(ins_1, \dots, ins_k)) \\
\forall i : 1 \leq i \leq n. (ls_i = Bypass(c) \rightarrow \mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_A \vdash Bypass(c)) \\
\forall i : 1 \leq i \leq n. (ls_i = NextHeader(id) \rightarrow \mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_A \vdash NextHeader(id)) \\
\forall i : 1 \leq i \leq n. (ls_i = Length(e) \rightarrow \mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_A \vdash Length(e)) \\
\forall i : 1 \leq i \leq n. (ls_i = IfElseL(if_l_list, d_l) \rightarrow \mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_C \vdash IfElseL(if_l_list, d_l)) \\
\mathcal{L}_C \text{ is } \mathcal{L}_A, \mathcal{L}_{B0} \text{ or } \mathcal{L}_{B1} \\
\hline
\mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_C \vdash (ls_1, \dots, ls_n) \quad \text{LSL}
\end{array}$$

$$\begin{array}{c}
if_l_list = ((e_1, l_stmts_1), \dots, (e_k, l_stmts_k)) \\
d_l = l_stmts \quad \forall i : 1 \leq i \leq k. \mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_C \vdash e_k : Bool \\
\forall i : 1 \leq i \leq k. \mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_C \vdash l_stmts_i \\
\mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_C \vdash d_l \quad \mathcal{L}_C \text{ is } \mathcal{L}_A, \mathcal{L}_{B0} \text{ or } \mathcal{L}_{B1} \\
\hline
\mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_C \vdash IfElseL(if_l_list, d_l) \quad \text{IFEL}
\end{array}$$

- Layer local actions

$$\begin{array}{c}
caas = CellA(ca_l_s_list) \\
cb0as = CellB0(cb0_l_s_list) \quad cb1as = CellB1(cb1_l_s_list) \\
\mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_C \vdash ca_l_s_list \quad \mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_C \vdash cb0_l_s_list \\
\mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_C \vdash cb1_l_s_list \quad \mathcal{L}_C \text{ is } \mathcal{L}_A, \mathcal{L}_{B0} \text{ or } \mathcal{L}_{B1} \\
\hline
\mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_C \vdash LocalActions(caas, cb0as, cb1as) \quad \text{LLA}
\end{array}$$

- Layer local register declarations

$$\begin{array}{c}
cars = CellARegs(ca_ra_ss_list) \\
cb0rs = CellB0Regs(cb0_ra_ss_list) \\
cb1rs = CellB1Regs(cb1_ra_ss_list) \\
\forall ras \in ca_ra_ss_list. \mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L} \vdash ras \\
\forall ras \in cb0_ra_ss_list. \mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L} \vdash ras \\
\forall ras \in cb1_ra_ss_list. \mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L} \vdash ras \\
\hline
\mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L} \vdash LocalRegs(cars, cb0rs, cb1rs) \quad \text{LLRD}
\end{array}$$

- Layer action

$$\begin{array}{c}
\mathcal{G} \vdash Lset(id_1, \dots, id_k) \quad id \in \{id_1, \dots, id_k\} \quad \mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}_{id} \vdash lvs \\
\mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}_{id} \vdash lrd \quad \mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}_{id} \vdash ld \quad \mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}_{id} \vdash las \\
\hline
\mathcal{G}, \mathcal{C}, \mathcal{R} \vdash LayerAction(id, lvs, lrd, ld, las) \quad \text{LA}
\end{array}$$

- Protocol statement

$$\begin{array}{c}
\forall i : 1 \leq i \leq n. (ps_i = \text{Action}(ins_1, \dots, ins_k) \rightarrow \mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_A, \mathcal{P} \vdash \text{Action}(ins_1, \dots, ins_k)) \\
\forall i : 1 \leq i \leq n. (ps_i = \text{IfElseP}(if_p_list, d_p \rightarrow \mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_A, \mathcal{P} \vdash \text{IfElseP}(if_p_list, d_p)) \\
\quad \forall i : 1 \leq i \leq n. (ps_i = \text{NextHeader}(id) \rightarrow \mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_A, \mathcal{P} \vdash \text{NextHeader}(id)) \\
\quad \forall i : 1 \leq i \leq n. (ps_i = \text{Bypass}(c) \rightarrow \mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_A, \mathcal{P} \vdash \text{Bypass}(c)) \\
\quad \forall i : 1 \leq i \leq n. (ps_i = \text{Length}(e) \rightarrow \mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_A, \mathcal{P} \vdash \text{Length}(e)) \\
\hline
\mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_A, \mathcal{P} \vdash (ps_1, \dots, ps_n) \quad \text{PSL}
\end{array}$$

$$\begin{array}{c}
if_p_list = ((e_1, p_stmts_1), \dots, (e_k, p_stmts_k)) \\
d_p = p_stmts \quad \forall i : 1 \leq i \leq k. \mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_A, \mathcal{P} \vdash e_k : \text{Bool} \\
\quad \forall i : 1 \leq i \leq k. \mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_A, \mathcal{P} \vdash p_stmts_i \\
\quad \mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_A, \mathcal{P} \vdash p_stmts \\
\hline
\mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_A, \mathcal{P} \vdash \text{IfElseL}(if_p_list, d_p) \quad \text{IFEP}
\end{array}$$

$$\begin{array}{c}
\mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_A, \mathcal{P} \vdash (\text{Fields}(flds), \text{OptionFields}(oflds)) \\
flds = ((fld_1 : c_1), \dots, (fld_k : c_k)) \\
\emptyset \vdash c_1 : (\text{Int}, n_1), \dots, \emptyset \vdash c_k : (\text{Int}, n_k) \\
\emptyset \vdash e : (\text{Int}, n) \quad n * 8 \geq n_1 + \dots + n_k \\
\hline
\mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_A, \mathcal{P} \vdash \text{Length}(e) \quad \text{LENGTH-P}
\end{array}$$

- Protocol declaration

$$\begin{array}{c}
\mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_A, \mathcal{P} \vdash fields \\
p_stmts = (ps_1, \dots, ps_m) \quad \forall i : 1 \leq i \leq m. \mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_A, \mathcal{P} \vdash ps_i \\
\hline
\mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_A, \mathcal{P} \vdash \text{Protocol}(fields, p_stmts) \quad \text{PROTOCOL}
\end{array}$$

$$\begin{array}{c}
\mathcal{G} \vdash \text{Pset}(id_1, \dots, id_k) \\
id \in \{id_1, \dots, id_k\} \quad \mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_A, \mathcal{P}_{id} \vdash p \\
\hline
\mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}, \mathcal{L}_A \vdash \text{ProtocolDecl}(id, p) \quad \text{PD}
\end{array}$$

- Global declarations

$$\frac{\begin{array}{c} \mathcal{G} \vdash Lset(id_1, \dots, id_k) \\ \forall lid \in \{id_1, \dots, id_k\}. (ProtocolDef(id, \dots) \text{ is declared at the layer } lid \rightarrow \\ \mathcal{G}, \mathcal{C}, \mathcal{R}, \mathcal{L}_{lid}, \mathcal{L}_A \vdash ProtocolDecl(id, p)) \end{array}}{\mathcal{G}, \mathcal{C}, \mathcal{R} \vdash ProtocolDecl(id, p)} \text{PDG}$$

$$\frac{\begin{array}{c} \forall i : 1 \leq i \leq n. (decl_i = ConstDecl(consdcl) \rightarrow \mathcal{C} \vdash consdcl) \\ \forall i : 1 \leq i \leq n. (decl_i = RegAccSet(regacc) \rightarrow \mathcal{G}, \mathcal{C}, \mathcal{R} \vdash regacc) \\ \forall i : 1 \leq i \leq n. (decl_i = ProtocolDecl(pdcl) \rightarrow \mathcal{G}, \mathcal{C}, \mathcal{R} \vdash pdcl) \\ \forall i : 1 \leq i \leq n. (decl_i = LayerAction(lact) \rightarrow \mathcal{G}, \mathcal{C}, \mathcal{R} \vdash lact) \\ \mathcal{G} \vdash Lset(id_1, \dots, id_k) \\ \forall lid \in \{id_1, \dots, id_k\}. LayerAction(id, lvs, lrd, ld, las) \text{ is declared in the same order} \end{array}}{\mathcal{G}, \mathcal{C}, \mathcal{R} \vdash (decl_1, \dots, decl_n)} \text{GDECL}$$

- Parser Specification

$$\frac{\begin{array}{c} \mathcal{G} \vdash l_reg_len \\ \mathcal{G} \vdash c_reg_len \quad \mathcal{G} \vdash p_set \quad \mathcal{G} \vdash l_set \quad \mathcal{G}, \mathcal{C}, \mathcal{R} \vdash decls \end{array}}{\emptyset \vdash Parser(l_reg_len, c_reg_len, p_set, l_set, decls)} \text{PSPEC}$$

5.2 Implementation and Verification

The implementation of the type checking is in Coq first and then extracted into the OCaml code. Based on the typing rules in the subsection 5.1, we define:

- $wt(p)$: p is well-typed P3 AST

To verify the correctness of the type checking program *type_checker*, we will prove two properties as follows:

- *Soundness*. $\forall p, \exists p'. type_checker(p) = OK(p') \rightarrow wt(p')$
- *Completeness*. $\forall p, \exists p'. wt(p) \rightarrow type_checker(p) = OK(p')$

6 Translations

Referring to Fig.1, we have two steps of the translations in the compiler: from a P3 AST to its P3 assembly, and from the P3 assembly to the configuration File.

6.1 Translation of AST to the P3 Assembly

The subsection 6.1.1 gives the abstract syntax of the P3 assembly generated from a P3 AST.

6.1.1 Abstract Syntax of the P3 assembly

$\langle \text{parser_asm} \rangle ::= \langle \text{layer_reg_len} \rangle \langle \text{cell_reg_len} \rangle \{ \langle \text{layer_block} \rangle \}$

$\langle \text{layer_reg_len} \rangle ::= \text{Lreglen} (\langle \text{num} \rangle)$

$\langle \text{cell_reg_len} \rangle ::= \text{Creglen} (\langle \text{num} \rangle)$

$\langle \text{layer_block} \rangle ::= \text{LayerBlock} (\langle \text{layer_id} \rangle, \langle \text{pins} \rangle, \langle \text{cella} \rangle, \langle \text{cellb0} \rangle, \langle \text{cellb1} \rangle)$

$\langle \text{layer_id} \rangle ::= \text{IDENT}$

$\langle \text{pins} \rangle ::= \{ \text{Pins} (\langle \text{ins_name} \rangle, \langle \text{ins_size} \rangle) \}$

$\langle \text{cella} \rangle ::= \text{CellA} (\langle \text{cella_pb} \rangle, \langle \text{cella_pc_cur} \rangle, \langle \text{cella_pc_nxt} \rangle)$

$\langle \text{cellb0} \rangle ::= \text{CellB0} (\langle \text{cellb0_pb} \rangle, \langle \text{cellb0_pc_cur} \rangle)$

$\langle \text{cellb1} \rangle ::= \text{CellB0} (\langle \text{cellb1_pb} \rangle, \langle \text{cellb1_pc_cur} \rangle)$

$\langle \text{cella_pb} \rangle ::= \text{Apb} (\{ \langle \text{cella_pb_item} \rangle \})$

$\langle \text{cella_pc_cur} \rangle ::= \text{ApcCur} (\{ \langle \text{cella_pc_cur_item} \rangle \})$

$\langle \text{cella_pc_nxt} \rangle ::= \text{ApcNxt} (\{ \langle \text{cella_pc_nxt_item} \rangle \})$

$\langle \text{cellb0_pb} \rangle ::= \text{B0pb} (\{ \langle \text{cellb0_pb_item} \rangle \})$

$\langle \text{cellb0_pc_cur} \rangle ::= \text{B0pcCur} (\{ \langle \text{cellb0_pc_cur_item} \rangle \})$

$\langle \text{cellb1_pb} \rangle ::= \text{B1pb} (\{ \langle \text{cellb1_pb_item} \rangle \})$

$\langle \text{cellb1_pc_cur} \rangle ::= \text{B1pcCur} (\{ \langle \text{cellb1_pc_cur_item} \rangle \})$

$\langle \text{cella_pb_item} \rangle ::= (\langle \text{hdr_id} \rangle, \langle \text{cond_list} \rangle, \langle \text{sub_id} \rangle, \langle \text{nxt_id} \rangle, \langle \text{bypas} \rangle)$

$\langle \text{cella_pc_cur_item} \rangle ::= (\langle \text{sub_id} \rangle, \langle \text{cmd_list} \rangle, \langle \text{lyr_offset} \rangle)$

$\langle \text{cella_pc_nxt_item} \rangle ::= (\langle \text{nxt_id} \rangle, \langle \text{cella_nxt} \rangle, \langle \text{cellb0_nxt} \rangle, \langle \text{cellb1_nxt} \rangle)$

$\langle \text{cellb0_pb_item} \rangle ::= (\langle \text{hdr_id} \rangle, \langle \text{cond_list} \rangle, \langle \text{sub_id} \rangle)$

$\langle \text{cellb0_pc_cur_item} \rangle ::= (\langle \text{sub_id} \rangle, \langle \text{cmd_list} \rangle)$

$$\begin{aligned}
\langle cellb1_pb_item \rangle &::= (\langle hdr_id \rangle, \langle cond_list \rangle, \langle sub_id \rangle) \\
\langle cellb1_pc_cur_item \rangle &::= (\langle sub_id \rangle, \langle cmd_list \rangle) \\
\langle cond_list \rangle &::= Conds(\langle cond \rangle \{, \langle cond \rangle \}) \\
\langle cmd_list \rangle &::= Cmds(\langle cmd \rangle \{, \langle cmd \rangle \}) \\
\\
\langle hdr_id \rangle &::= HdrID(\langle num \rangle) \\
\langle sub_id \rangle &::= SubID(\langle num \rangle) \\
\langle nxt_id \rangle &::= NxtID(\langle num \rangle) \\
\langle bypas \rangle &::= Bypas(\langle num \rangle) \\
\langle lyr_offset \rangle &::= LyrOffset(\langle num \rangle) \\
\langle cella_nxt \rangle &::= CellANxt(\langle irf_offsets \rangle, \langle prot_offsets \rangle) \\
\langle cellb0_nxt \rangle &::= CellB0Nxt(\langle irf_offsets \rangle, \langle prot_offsets \rangle) \\
\langle cellb1_nxt \rangle &::= CellB1Nxt(\langle irf_offsets \rangle, \langle prot_offsets \rangle) \\
\langle irf_offsets \rangle &::= IRFOffset(\langle num \rangle \{, \langle num \rangle \}) \\
\langle prot_offsets \rangle &::= ProtOffset(\langle num \rangle \{, \langle num \rangle \}) \\
\langle cond \rangle &::= (\langle reg_seg \rangle, \langle num \rangle) \quad | \quad (\langle ins_seg \rangle, \langle num \rangle) \\
\langle cmd \rangle &::= \begin{array}{l} \langle set_cmd \rangle \\ | \\ \langle mov_cmd \rangle \\ | \\ \langle lg_cmd \rangle \\ | \\ \langle eq_cmd \rangle \end{array} \\
\langle set_cmd \rangle &::= Set(\langle reg_seg \rangle, \langle num \rangle) \\
\langle mov_cmd \rangle &::= Mov(\langle reg_seg \rangle, \langle src_reg \rangle) \\
\langle lg_cmd \rangle &::= Lg(\langle reg_seg \rangle, \langle src_reg \rangle, \langle src_reg \rangle) \\
\langle eq_cmd \rangle &::= Eq(\langle reg_seg \rangle, \langle src_reg \rangle, \langle src_reg \rangle) \\
\langle src_reg \rangle &::= (\mathbf{IRF}, \langle reg_offset \rangle, \langle reg_size \rangle) \\
&\quad | \langle num \rangle \\
\langle reg_seg \rangle &::= (\mathbf{IRF}, \langle reg_offset \rangle, \langle seg_size \rangle) \\
\langle ins_seg \rangle &::= (\langle ins_name \rangle, \langle ins_offset \rangle, \langle seg_size \rangle)
\end{aligned}$$

7.2.1 Values and Memory model for Registers and Fields

The semantic values and the memory model used in the semantics definition can be inferred from the semantic environment in the subsection 7.2.2. To save the space, we omit to present them separately.

7.2.2 Semantic environment

Global	ge	$::= (\gamma, \sigma, \delta)$	divide global environment into three parts
	γ	$::= (lr, cr, ps, ls, \iota, \rho)$	several basic settings of a $P3$ specification
	σ	$::= id \rightarrow val$	map a constant identifier to val
	δ	$::= raid \rightarrow regacc(n, i, j, bv)$	map a register-access identifier to a segment $(i..j)$ of a register IRF sized n , with the binary value bv
	lr	$::= lreglen(k)$	the $Lreglen$ value set to k
	cr	$::= creglen(k)$	the $Creglen$ value set to k
	ps	$::= pset(id, \dots, id)$	the set of protocol identifiers
	ls	$::= lset(id, \dots, id)$	the set of layer identifiers
	ι	$::= lid \rightarrow ldef$	map a layer identifier to a layer definition
	ρ	$::= pid \rightarrow pdef$	map a protocol identifier to a protocol definition
Layer	le	$::= (\xi_\iota, nh, len, bp)$	divide layer local environment into four parts
	ξ_ι	$::= id \rightarrow (k, (fid \rightarrow (n, bv)))$	map a protocol instance identifier to the length of the protocol (k) and a function that maps a field identifier to a binary value bv sized n
	nh	$::= nexthead(pid)$	the $NextHeader$ set to the protocol identified by pid
Cell	len	$::= length(k)$	the $Length$ bound to an integer
	bp	$::= bypass(k)$	the $Bypass$ bound to an integer
	ce	$::= \delta_A \mid \delta_{B0} \mid \delta_{B1}$	divide cell local environment into three branches
	δ_A	$::= raid \rightarrow regacc(n, i, j, bv)$	map a register-access identifier to a segment $(i..j)$ of a register IRF sized n , with the binary value bv
	δ_{B0}	$::= raid \rightarrow regacc(n, i, j, bv)$	map a register-access identifier to a segment $(i..j)$ of a register IRF sized n , with the binary value bv
	δ_{B1}	$::= raid \rightarrow regacc(n, i, j, bv)$	map a register-access identifier to a segment $(i..j)$ of a register IRF sized n , with the binary value bv
Protocol	ξ_ρ	$::= fid \rightarrow fdacc(id, n, i, j, bv)$	map a field identifier to a segment $(i..j)$ of a protocol instance identified id sized no less than n , with the binary value bv
Identifier	$raid, lid, pid, fid$	$::= id$	

Figure 10: Semantic Environments

The semantic environment maps variables to the values and memory for registers and fields, and has the form

$$\mathcal{E} ::= [x_1 : v_1, x_2 : v_2, \dots, x_n : v_n]$$

where $x_i \neq x_j$ for all i and j , satisfying $i \neq j$ and $(1 \leq i, j \leq n)$.

Figure 10 show all the semantic environments we use to define the semantics. In some cases, we use the subscript *id* to denote a particular local semantic environment specific to the context of a protocol or a layer identified by *id*.

7.2.3 Judgements

The judgements used in the semantics definition can be inferred from the semantic rules in the subsection 7.2.4. To save the space, we omit to present them separately.

7.2.4 Semantic rules

- Initialization of γ , opened at the beginning of the specification and not to be closed, where $\gamma = (lr, cr, ps, ls, \iota, \rho)$

SLR-Initialization of *lr* :

$$\frac{\gamma = (lr, cr, ps, ls, \iota, \rho) \quad \vdash IntConst(k) \Rightarrow val(k) \quad lr = null \quad lr' = lreglen(val(k)) \quad \gamma' = (lr', cr, ps, ls, \iota, \rho)}{\vdash (\gamma, Lreglen(IntConst(k))) \Rightarrow \gamma'} \text{ SLR}$$

SCR-Initialization of *cr* :

$$\frac{\gamma = (lr, cr, ps, ls, \iota, \rho) \quad \vdash IntConst(k) \Rightarrow val(k) \quad cr = null \quad cr' = lreglen(val(k)) \quad \gamma' = (lr, cr', ps, ls, \iota, \rho)}{\vdash (\gamma, Creglen(IntConst(k))) \Rightarrow \gamma'} \text{ SCR}$$

SPS-Initialization of *ps* :

$$\frac{\gamma = (lr, cr, ps, ls, \iota, \rho) \quad ps = null \quad ps' = pset(id_1, \dots, id_k) \quad \gamma' = (lr, cr, ps', ls, \iota, \rho)}{\vdash (\gamma, Pset(id_1, \dots, id_k)) \Rightarrow \gamma'} \text{ SPS}$$

SLS-Initialization of *ls* :

$$\frac{\gamma = (lr, cr, ps, ls, \iota, \rho) \quad ls = null \quad ls' = pset(id_1, \dots, id_k) \quad \gamma' = (lr, cr, ps, ls', \iota, \rho)}{\vdash (\gamma, Lset(id_1, \dots, id_k)) \Rightarrow \gamma'} \text{ SLS}$$

SLA-Initialization of ι :

$$\frac{\gamma = (lr, cr, ps, ls, \iota, \rho) \quad ldef = get_layer_def(lvs, lrd, ld, las) \quad id \notin dom(\iota) \quad \iota' = \iota \cup \{id : ldef\} \quad \gamma' = (lr, cr, ps, ls, \iota', \rho)}{\vdash (\gamma, LayerAction(id, lvs, lrd, ld, las)) \Rightarrow \gamma'} \text{SLA}$$

SPD-Initialization of ρ :

$$\frac{\gamma = (lr, cr, ps, ls, \iota, \rho) \quad pdef = get_protocol_def(p) \quad id \notin dom(\rho) \quad \rho' = \rho \cup \{id : pdef\} \quad \gamma' = (lr, cr, ps, ls, \iota, \rho')}{\vdash (\gamma, ProtocolDecl(id, p)) \Rightarrow \gamma'} \text{SPD}$$

- Initialization of σ , opened at the beginning of the specification and not to be closed

$$\frac{\vdash c \Rightarrow v \quad id \notin dom(\sigma) \quad ge = (\gamma, \sigma, \delta) \quad \sigma' = \sigma \cup \{id : v\} \quad ge' = (\gamma, \sigma', \delta)}{\vdash (ge, ConstDcl(id, c)) \Rightarrow ge'} \text{(SIC-1)}$$

$$\frac{val(i) \text{ is a signed integer up to 32 bits}}{\vdash IntConst(i) \Rightarrow val(i)} \text{(SIC-2)}$$

$$\frac{val(i) \text{ is a number } i \text{ with hexadecimal digits}}{\vdash HexConst(i) \Rightarrow val(i)} \text{(SIC-3)}$$

$$\frac{val(bs) \text{ is the binary bit string of } bs}{\vdash BitSConst(bs) \Rightarrow val(bs)} \text{(IC-4)}$$

- Initialization of δ , initialized at the beginning of the specification and changed each time at the leaving of a layer context (Rule SIR-3).

$$\begin{array}{c}
ge = (\gamma, \sigma, \delta) \quad ge \vdash e_1 \Rightarrow n_1 \quad ge \vdash e_2 \Rightarrow n_2 \\
\gamma = (lreglen(n), cr, ps, ls, \iota, \rho) \quad 0 \leq n_2 \leq n_1 < n \quad id \notin dom(\delta) \\
\forall id' \in dom(\delta). (\delta \vdash id' \Rightarrow regacc(n, n'_1, n'_2, base_layer_bv_{id'}) \rightarrow n'_1 < n_2 \vee n_1 < n'_2) \\
\delta' = \delta \cup \{id : regacc(n, n_1, n_2, base_layer_bv_{id})\} \quad ge' = (\gamma, \sigma, \delta') \\
\hline
\vdash (ge, IRF(id, e_1, e_2)) \Rightarrow ge' \quad (SIR-1)
\end{array}$$

$$\begin{array}{c}
ge = (\gamma, \sigma, \delta) \quad ge \vdash e \Rightarrow k \\
\gamma = (lreglen(n), cr, ps, ls, \iota, \rho) \quad 0 \leq k < n \quad id \notin dom(\delta) \\
\forall id' \in dom(\delta). (\delta \vdash id' \Rightarrow regacc(n, n'_1, n'_2, base_layer_bv_{id'}) \rightarrow n'_1 < k \vee k < n'_2) \\
\delta' = \delta \cup \{id : regacc(n, k, k, base_layer_bv_{id})\} \quad ge' = (\gamma, \sigma, \delta') \\
\hline
\vdash (ge, IRF(id, e)) \Rightarrow ge' \quad (SIR-2)
\end{array}$$

$$\begin{array}{c}
ge = (\gamma, \sigma, \delta) \quad \gamma = (lreglen(n), creglen(k), ps, ls, \iota, \rho) \\
n = 3 * k \quad le = (\xi_\iota, nextheader(pid), length(i), bypass(j)) \\
\delta' = \{id : regacc(n, 2 * k + n_1, 2 * k + n_2, bva) \mid id : regacc(k, n_1, n_2, bva) \in \delta_A\} \\
\cup \{id : regacc(n, k + n_1, k + n_2, bvb0) \mid id : regacc(k, n_1, n_2, bvb0) \in \delta_{B0}\} \\
\cup \{id : regacc(n, n_1, n_2, bvb1) \mid id : regacc(k, n_1, n_2, bvb1) \in \delta_{B1}\} \\
ge' = (\gamma, \sigma, \delta') \\
le' = (\emptyset, nextheader(null), length(null), bypass(null)) \quad \delta'_A = null \\
\hline
\vdash (ge, le, \delta_A, \text{"layer-switch"}) \Rightarrow (ge', le', \delta'_A) \quad (SIR-3)
\end{array}$$

- Initialization of le , opened at the beginning and closed at the end of a LayerAction specification

$$\begin{array}{c}
ge = (\gamma, \sigma, \delta) \quad \gamma = (lr, cr, ps, ls, \iota, \rho) \\
le = (\xi_\iota, nh, len, bp) \quad \rho \vdash pid \Rightarrow ((fid_1 : n_1, \dots, fid_m : n_m), pstmts) \\
\forall i : 1 \leq i \leq k. id_i \notin dom(\xi_\iota) \\
\xi'_\iota = \xi_\iota \cup \{id_i : (n_1 + \dots + n_m, pins_i) \mid 1 \leq i \leq k \wedge pins_i = ((fid_1, (n_1, bv_1^i)), \dots, (fid_m, (n_m, bv_m^i)))\}, \\
\text{where all } bv \text{'s are the input from the hardware} \\
le' = (\xi'_\iota, nextheader(null), length(null), bypass(null)) \\
\hline
ge \vdash (le, ProtocolDef(pid, (id_1, \dots, id_k))) \Rightarrow le' \quad (SIL)
\end{array}$$

- Initialization of δ_A at the Cella Registers specification, opened at the beginning of a Cell A specification, and closed at the leaving of the layer context

$$\begin{array}{c}
ge = (\gamma, \sigma, \delta) \quad \gamma = (lreglen(n), creglen(k), ps, ls, \iota, \rho) \\
n = 3 * k \quad ge, le, \delta_A \vdash e_1 \Rightarrow n_1 \\
ge, le, \delta_A \vdash e_2 \Rightarrow n_2 \quad 0 \leq n_2 \leq n_1 < k \quad id \notin dom(\delta_A) \cup dom(\delta) \\
\forall id' \in dom(\delta_A). (\delta_A \vdash id' \Rightarrow regacc(k, n'_1, n'_2, bv) \rightarrow n'_1 < n_2 \vee n_1 < n'_2) \\
\forall id' \in dom(\delta). (\delta \vdash id' \Rightarrow regacc(n, n'_1, n'_2, bv) \rightarrow n'_1 < 2 * k + n_2 \vee 2 * k + n_1 < n'_2) \\
\delta'_A = \delta_A \cup \{id : regacc(k, n_1, n_2, null)\} \\
\hline
ge, le \vdash (\delta_A, IRF(id, e_1, e_2)) \Rightarrow \delta'_A \quad (SILA-1)
\end{array}$$

$$\begin{array}{c}
ge = (\gamma, \sigma, \delta) \quad \gamma = (lreglen(n), creglen(k), ps, ls, \iota, \rho) \quad n = 3 * k \\
ge, le, \delta_A \vdash e \Rightarrow m \quad 0 \leq m < k \quad id \notin dom(\delta_A) \cup dom(\delta) \\
\forall id' \in dom(\delta_A). (\delta_A \vdash id' \Rightarrow regacc(k, n'_1, n'_2, bv) \rightarrow n'_1 < m \vee m < n'_2) \\
\forall id' \in dom(\delta). (\delta \vdash id' \Rightarrow regacc(n, n'_1, n'_2, bv) \rightarrow n'_1 < 2 * k + m \vee 2 * k + m < n'_2) \\
\delta'_A = \delta_A \cup \{id : regacc(k, m, m, null)\} \\
\hline
ge, le \vdash (\delta_A, IRF(id, e)) \Rightarrow \delta'_A \quad (SILA-2)
\end{array}$$

- Initialization of δ_{B0} at the CellB0 Registers specification, opened at the beginning of a Cell B0 specification, and closed at the leaving of the layer context

$$\begin{array}{c}
ge = (\gamma, \sigma, \delta) \quad \gamma = (lreglen(n), creglen(k), ps, ls, \iota, \rho) \\
n = 3 * k \quad ge, le, \delta_{B0} \vdash e_1 \Rightarrow n_1 \\
ge, le, \delta_{B0} \vdash e_2 \Rightarrow n_2 \quad 0 \leq n_2 \leq n_1 < k \quad id \notin dom(\delta_{B0}) \cup dom(\delta) \\
\forall id' \in dom(\delta_{B0}). (\delta_{B0} \vdash id' \Rightarrow regacc(k, n'_1, n'_2, bv) \rightarrow n'_1 < n_2 \vee n_1 < n'_2) \\
\forall id' \in dom(\delta). (\delta \vdash id' \Rightarrow regacc(n, n'_1, n'_2, bv) \rightarrow n'_1 < k + n_2 \vee k + n_1 < n'_2) \\
\delta'_{B0} = \delta_{B0} \cup \{id : regacc(k, n_1, n_2, null)\} \\
\hline
ge, le \vdash (\delta_{B0}, IRF(id, e_1, e_2)) \Rightarrow \delta'_{B0} \quad (SILB0-1)
\end{array}$$

$$\begin{array}{c}
ge = (\gamma, \sigma, \delta) \quad \gamma = (lreglen(n), creglen(k), ps, ls, \iota, \rho) \quad n = 3 * k \\
ge, le, \delta_{B0} \vdash e \Rightarrow n \quad 0 \leq m < k \quad id \notin dom(\delta_{B0}) \cup dom(\delta) \\
\forall id' \in dom(\delta_{B0}). (\delta_{B0} \vdash id' \Rightarrow regacc(k, n'_1, n'_2, bv) \rightarrow n'_1 < m \vee m < n'_2) \\
\forall id' \in dom(\delta). (\delta \vdash id' \Rightarrow regacc(n, n'_1, n'_2, bv) \rightarrow n'_1 < k + m \vee k + m < n'_2) \\
\delta'_{B0} = \delta_{B0} \cup \{id : regacc(k, m, m, null)\} \\
\hline
ge, le \vdash (\delta_{B0}, IRF(id, e)) \Rightarrow \delta'_{B0} \quad (SILB0-2)
\end{array}$$

- Initialization of δ_{B1} at the CellB0 Registers specification, opened at the beginning of a Cell B1 specification, and closed at the leaving of the layer context

$$\begin{array}{c}
ge = (\gamma, \sigma, \delta) \quad \gamma = (lreglen(n), creglen(k), ps, ls, \iota, \rho) \\
n = 3 * k \quad ge, le, \delta_{B1} \vdash e_1 \Rightarrow n_1 \\
ge, le, \delta_{B1} \vdash e_2 \Rightarrow n_2 \quad 0 \leq n_2 \leq n_1 < k \quad id \notin dom(\delta_{B1}) \cup dom(\delta) \\
\forall id' \in dom(\delta_{B1}). (\delta_{B1} \vdash id' \Rightarrow regacc(k, n'_1, n'_2, bv) \rightarrow n'_1 < n_2 \vee n_1 < n'_2) \\
\forall id' \in dom(\delta). (\delta \vdash id' \Rightarrow regacc(n, n'_1, n'_2, bv) \rightarrow n'_1 < n_2 \vee n_1 < n'_2) \\
\delta'_{B1} = \delta_{B1} \cup \{id : regacc(k, n_1, n_2, null)\} \\
\hline
ge, le \vdash (\delta_{B1}, IRF(id, e_1, e_2)) \Rightarrow \delta'_{B1} \quad (SILB1-1)
\end{array}$$

$$\begin{array}{c}
ge = (\gamma, \sigma, \delta) \quad \gamma = (lreglen(n), creglen(k), ps, ls, \iota, \rho) \quad n = 3 * k \\
ge, le, \delta_{B0} \vdash e \Rightarrow m \quad 0 \leq m < k \quad id \notin dom(\delta_{B1}) \cup dom(\delta) \\
\forall id' \in dom(\delta_{B1}). (\delta_{B1} \vdash id' \Rightarrow regacc(k, n'_1, n'_2, bv) \rightarrow n'_1 < m \vee m < n'_2) \\
\forall id' \in dom(\delta). (\delta \vdash id' \Rightarrow regacc(n, n'_1, n'_2, bv) \rightarrow n'_1 < m \vee m < n'_2) \\
\delta'_{B1} = \delta_{B1} \cup \{id : regacc(k, m, m, null)\} \\
\hline
ge, le \vdash (\delta_{B1}, IRF(id, e)) \Rightarrow \delta'_{B1} \quad (SILB1-2)
\end{array}$$

- Initialization of ξ_ρ , opened at each time of the instantiation of a Protocol specification and closed at the end of that instantiation.

$$\begin{array}{c}
le = (\xi_\iota, nh, len, bp) \quad \xi_\rho = \emptyset \\
flds++ofld = ((fld_1 : c_1), \dots, (fld_k : c_k)), \text{ where } c_k \text{ to be a number or a (null)} \\
\text{There exists an unique protocol instance identified by } id, \text{ such that } (id : (len', pins)) \in \xi_\iota, \\
\text{where } pins = ((fid_1, (n_1, bv_1)), \dots, (fid_k, (n_k, bv_k))) \\
n = n_1 + n_2 + \dots + n_k \\
\xi'_\rho = \{fld_i : (id, n, n_1 + \dots + n_{i-1}, n_1 + \dots + n_i - 1), bv_i) \mid 1 \leq i \leq k\} \\
\hline
ge, le, \delta_A \vdash (\xi_\rho, ProtocolDecl(pid, Protocol((Fields(flds), OptionFields(ofld)), pstmts))) \Rightarrow \xi'_\rho \quad (SIP-1)
\end{array}$$

- Expressions

$$\begin{array}{c}
\frac{ge = (\gamma, \sigma, \delta) \quad \sigma \vdash c \Rightarrow v \quad \delta_C \text{ is } \delta_A, \delta_{B0} \text{ or } \delta_{B1}}{ge, le, \delta_C \vdash Econst(c) \Rightarrow v} \text{ SCE-1} \\
\\
\frac{ge = (\gamma, \sigma, \delta) \quad \sigma \vdash c \Rightarrow v}{ge, le, \delta_A, \xi_\rho \vdash Econst(c) \Rightarrow v} \text{ SCE-2} \quad \frac{ge = (\gamma, \sigma, \delta) \quad \sigma \vdash c \Rightarrow v}{ge \vdash Econst(c) \Rightarrow v} \text{ SCE-3}
\end{array}$$

$$\frac{ge, le, \delta_C \vdash e \Rightarrow v \quad v' = \text{trans_to_int}(v) \quad \delta_C \text{ is } \delta_A, \delta_{B0} \text{ or } \delta_{B1}}{ge, le, \delta_C \vdash \text{Eunop}(\text{Oint}, e) \Rightarrow v'} \text{SOINT-1}$$

$$\frac{ge, le, \delta_A, \xi_\rho \vdash e \Rightarrow v \quad v' = \text{trans_to_int}(v)}{ge, le, \delta_A, \xi_\rho \vdash \text{Eunop}(\text{Oint}, e) \Rightarrow v'} \text{SOINT-2}$$

$$\frac{ge, le, \delta_C \vdash e \Rightarrow v \quad v' = \text{not}(v) \quad \delta_C \text{ is } \delta_A, \delta_{B0} \text{ or } \delta_{B1}}{ge, le, \delta_C \vdash \text{Eunop}(\text{Onot}, e) \Rightarrow v'} \text{SONOT-1}$$

$$\frac{ge, le, \delta_A, \xi_\rho \vdash e \Rightarrow v \quad v' = \text{not}(v)}{ge, le, \delta_A, \xi_\rho \vdash \text{Eunop}(\text{Onot}, e) \Rightarrow v'} \text{SONOT-2}$$

$$\frac{ge, le, \delta_C \vdash e \Rightarrow bs \quad bs' = \text{bit_wise_negation}(bs) \quad \delta_C \text{ is } \delta_A, \delta_{B0} \text{ or } \delta_{B1}}{ge, le, \delta_C \vdash \text{Eunop}(\text{Oneg}, e) \Rightarrow bs'} \text{SONEG-1}$$

$$\frac{ge, le, \delta_A, \xi_\rho \vdash e \Rightarrow bs \quad bs' = \text{bit_wise_negation}(bs)}{ge, le, \delta_A, \xi_\rho \vdash \text{Eunop}(\text{Oneg}, e) \Rightarrow bs'} \text{SONEG-2}$$

$$\frac{\begin{array}{l} ge, le, \delta_C \vdash e_1 \Rightarrow v_1 \\ ge, le, \delta_C \vdash e_2 \Rightarrow v_2 \quad \text{binop} \in \{\text{Oadd}, \text{Osub}, \text{Omul}, \text{Odivint}, \text{Omod}\} \\ v = \text{do_binop}(\text{binop}, \text{trans_to_int}(v_1), \text{trans_to_int}(v_2)) \\ \delta_C \text{ is } \delta_A, \delta_{B0} \text{ or } \delta_{B1} \end{array}}{ge, le, \delta_C \vdash \text{Ebinop}(\text{binop}, e_1, e_2) \Rightarrow v} \text{SBOP-A-1}$$

$$\frac{\begin{array}{l} ge, le, \delta_A, \xi_\rho \vdash e_1 \Rightarrow v_1 \\ ge, le, \delta_A, \xi_\rho \vdash e_2 \Rightarrow v_2 \quad \text{binop} \in \{\text{Oadd}, \text{Osub}, \text{Omul}, \text{Odivint}, \text{Omod}\} \\ v = \text{do_binop}(\text{binop}, \text{trans_to_int}(v_1), \text{trans_to_int}(v_2)) \end{array}}{ge, le, \delta_A, \xi_\rho \vdash \text{Ebinop}(\text{binop}, e_1, e_2) \Rightarrow v} \text{SBOP-A-2}$$

$$\frac{\begin{array}{l} ge \vdash e_1 \Rightarrow v_1 \\ ge \vdash e_2 \Rightarrow v_2 \quad \text{binop} \in \{\text{Oadd}, \text{Osub}, \text{Omul}, \text{Odivint}, \text{Omod}\} \\ v = \text{do_binop}(\text{binop}, \text{trans_to_int}(v_1), \text{trans_to_int}(v_2)) \end{array}}{ge \vdash \text{Ebinop}(\text{binop}, e_1, e_2) \Rightarrow v} \text{SBOP-A-3}$$

$$\frac{ge, le, \delta_C \vdash e_1 \Rightarrow v_1 \quad ge, le, \delta_C \vdash e_2 \Rightarrow v_2 \quad binop \in \{Oand, Oor\} \quad v = do_logic_binop(binop, v_1, v_2) \quad \delta_C \text{ is } \delta_A, \delta_{B0} \text{ or } \delta_{B1}}{ge, le, \delta_C \vdash Ebinop(binop, e_1, e_2) \Rightarrow v} \text{ SBOPL-1}$$

$$\frac{ge, le, \delta_A, \xi_\rho \vdash e_1 \Rightarrow v_1 \quad ge, le, \delta_A, \xi_\rho \vdash e_2 \Rightarrow v_2 \quad binop \in \{Oand, Oor\} \quad v = do_logic_binop(binop, v_1, v_2)}{ge, le, \delta_A, \xi_\rho \vdash Ebinop(binop, e_1, e_2) \Rightarrow v} \text{ SBOPL-2}$$

$$\frac{ge, le, \delta_C \vdash e_1 \Rightarrow bs_1 \quad ge, le, \delta_C \vdash e_2 \Rightarrow bs_2 \quad binop \in \{Oband, Obor, Obeor\} \quad bs = bit_wise_operation(binop, bs_1, bs_2) \quad \delta_C \text{ is } \delta_A, \delta_{B0} \text{ or } \delta_{B1}}{ge, le, \delta_C \vdash Ebinop(binop, e_1, e_2) \Rightarrow bs} \text{ SBOPB-1}$$

$$\frac{ge, le, \delta_A, \xi_\rho \vdash e_1 \Rightarrow bs_1 \quad ge, le, \delta_A, \xi_\rho \vdash e_2 \Rightarrow bs_2 \quad binop \in \{Oband, Obor, Obeor\} \quad bs = bit_wise_operation(binop, bs_1, bs_2)}{ge, le, \delta_A, \xi_\rho \vdash Ebinop(binop, e_1, e_2) \Rightarrow bs} \text{ SBOPB-2}$$

$$\frac{ge, le, \delta_C \vdash e_1 \Rightarrow v_1 \quad ge, le, \delta_C \vdash e_2 \Rightarrow v_2 \quad binop \in \{Oeq, One, Olt, Ogt, Ole, Oge\} \quad v = do_relation_binop(binop, v_1, v_2) \quad \delta_C \text{ is } \delta_A, \delta_{B0} \text{ or } \delta_{B1}}{ge, le, \delta_C \vdash Ebinop(binop, e_1, e_2) \Rightarrow v} \text{ SBOPR-1}$$

$$\frac{ge, le, \delta_A, \xi_\rho \vdash e_1 \Rightarrow v_1 \quad ge, le, \delta_A, \xi_\rho \vdash e_2 \Rightarrow v_2 \quad binop \in \{Oeq, One, Olt, Ogt, Ole, Oge\} \quad v = do_relation_binop(binop, v_1, v_2)}{ge, le, \delta_A, \xi_\rho \vdash Ebinop(binop, e_1, e_2) \Rightarrow v} \text{ SBOPR-2}$$

$$\frac{ge, le, \delta_C \vdash e_1 \Rightarrow bs_1 \quad ge, le, \delta_C \vdash e_2 \Rightarrow v_2 \quad binop \in \{Osl, Osr\} \quad bs = do_shift_binop(binop, bs_1, v_2) \quad \delta_C \text{ is } \delta_A, \delta_{B0} \text{ or } \delta_{B1}}{ge, le, \delta_C \vdash Ebinop(binop, e_1, e_2) \Rightarrow bs} \text{ SBOPS-1}$$

$$\frac{ge, le, \delta_A, \xi_\rho \vdash e_1 \Rightarrow bs_1 \quad ge, le, \delta_A, \xi_\rho \vdash e_2 \Rightarrow v_2 \quad binop \in \{Osl, Osr\} \quad bs = do_shift_binop(binop, bs_1, v_2)}{ge, le, \delta_A, \xi_\rho \vdash Ebinop(binop, e_1, e_2) \Rightarrow bs} \text{ SBOPS-2}$$

$$\frac{ge, le, \delta_C \vdash e_1 \Rightarrow bs_1 \quad ge, le, \delta_C \vdash e_2 \Rightarrow bs_2 \quad bs = cat(bs_1, bs_2) \quad \delta_C \text{ is } \delta_A, \delta_{B0} \text{ or } \delta_{B1}}{ge, le, \delta_C \vdash Ebinop(Obc, e_1, e_2) \Rightarrow bs} \text{SBOPC-1}$$

$$\frac{ge, le, \delta_A, \xi_\rho \vdash e_1 \Rightarrow bs_1 \quad ge, le, \delta_A, \xi_\rho \vdash e_2 \Rightarrow bs_2 \quad bs = cat(bs_1, bs_2)}{ge, le, \delta_A, \xi_\rho \vdash Ebinop(Obc, e_1, e_2) \Rightarrow bs} \text{SBOPC-1'}$$

$$\frac{ge, le, \delta_C \vdash e_1 \Rightarrow bs_1 \quad ge, le, \delta_C \vdash e_2 \Rightarrow bs_2 \quad bs = hex_cat(bs_1, bs_2) \quad \delta_C \text{ is } \delta_A, \delta_{B0} \text{ or } \delta_{B1}}{ge, le, \delta_C \vdash Ebinop(Obc, e_1, e_2) \Rightarrow bs} \text{SBOPC-2}$$

$$\frac{ge, le, \delta_A, \xi_\rho \vdash e_1 \Rightarrow bs_1 \quad ge, le, \delta_A, \xi_\rho \vdash e_2 \Rightarrow bs_2 \quad bs = hex_cat(bs_1, bs_2)}{ge, le, \delta_A, \xi_\rho \vdash Ebinop(Obc, e_1, e_2) \Rightarrow bs} \text{SBOPC-2'}$$

$$\frac{ge, le, \delta_C \vdash e_1 : regacc(k, n_1, n_2, bs_1) \quad |bs_1| = n_1 - n_2 + 1 \quad ge, le, \delta_C \vdash e_2 : regacc(k, m_1, m_2, bs_2) \quad |bs_2| = m_1 - m_2 + 1 \quad n_2 = m_1 + 1 \quad 0 \leq m_2 \leq m_1 < n_2 \leq n_1 < k \quad bs = cat(bs_1, bs_2) \quad \delta_C \text{ is } \delta_A, \delta_{B0} \text{ or } \delta_{B1}}{ge, le, \delta_C \vdash Ebinop(Obc, e_1, e_2) : regacc(k, n_1, m_2, bs)} \text{SBOPC-3}$$

$$\frac{ge, le, \delta_A, \xi_\rho \vdash e_1 : regacc(k, n_1, n_2, bs_1) \quad |bs_1| = n_1 - n_2 + 1 \quad ge, le, \delta_A, \xi_\rho \vdash e_2 : regacc(k, m_1, m_2, bs_2) \quad |bs_2| = m_1 - m_2 + 1 \quad n_2 = m_1 + 1 \quad 0 \leq m_2 \leq m_1 < n_2 \leq n_1 < k \quad bs = cat(bs_1, bs_2)}{ge, le, \delta_A, \xi_\rho \vdash Ebinop(Obc, e_1, e_2) : regacc(k, n_1, m_2, bs)} \text{SBOPC-3'}$$

$$\frac{ge, le, \delta_C \vdash e_1 : fdacc(id, k, n_1, n_2, bs_1) \quad |bs_1| = n_2 - n_1 + 1 \quad ge, le, \delta_C \vdash e_2 : fdacc(id, k, m_1, m_2, bs_2) \quad |bs_2| = m_2 - m_1 + 1 \quad m_1 = n_2 + 1 \quad 0 \leq n_1 \leq n_2 < m_1 \leq m_2 < k \quad bs = cat(bs_1, bs_2) \quad \delta_C \text{ is } \delta_A, \delta_{B0} \text{ or } \delta_{B1}}{ge, le, \delta_C \vdash Ebinop(Obc, e_1, e_2) : fdacc(id, k, n_1, m_2, bs)} \text{SBOPC-4}$$

$$\frac{ge, le, \delta_A, \xi_\rho \vdash e_1 : fdacc(id, k, n_1, n_2, bs_1) \quad |bs_1| = n_2 - n_1 + 1 \quad ge, le, \delta_A, \xi_\rho \vdash e_2 : fdacc(id, k, m_1, m_2, bs_2) \quad |bs_2| = m_2 - m_1 + 1 \quad m_1 = n_2 + 1 \quad 0 \leq n_1 \leq n_2 < m_1 \leq m_2 < k \quad bs = cat(bs_1, bs_2)}{ge, le, \delta_A, \xi_\rho \vdash Ebinop(Obc, e_1, e_2) : fdacc(id, k, n_1, m_2, bs)} \text{SBOPC-4'}$$

$$\frac{ge, le, \delta_C \vdash e_1 \Rightarrow v \quad ge, le, \delta_C \vdash e_2 \Rightarrow n \quad hn = trans_to_hex_number(v, n) \quad \delta_C \text{ is } \delta_A, \delta_{B0} \text{ or } \delta_{B1}}{ge, le, \delta_C \vdash Ebinop(Ohexes, e_1, e_2) \Rightarrow hn} \text{SBOPH-1}$$

$$\frac{ge, le, \delta_A, \xi_\rho \vdash e_1 \Rightarrow v \quad ge, le, \delta_A, \xi_\rho \vdash e_2 \Rightarrow n \quad hn = trans_to_hex_number(v, n)}{ge, le, \delta_A, \xi_\rho \vdash Ebinop(Ohexes, e_1, e_2) \Rightarrow hn} \text{BOPH-2}$$

$$\frac{ge, le, \delta_C \vdash e_1 \Rightarrow v \quad ge, le, \delta_C \vdash e_2 \Rightarrow n \quad bn = trans_to_binary_number(v, n) \quad \delta_C \text{ is } \delta_A, \delta_{B0} \text{ or } \delta_{B1}}{ge, le, \delta_C \vdash Ebinop(Ohexes, e_1, e_2) \Rightarrow bn} \text{SBOPBT-1}$$

$$\frac{ge, le, \delta_A, \xi_\rho \vdash e_1 \Rightarrow v \quad ge, le, \delta_A, \xi_\rho \vdash e_2 \Rightarrow n \quad bn = trans_to_binary_number(v, n)}{ge, le, \delta_A, \xi_\rho \vdash Ebinop(Ohexes, e_1, e_2) \Rightarrow bn} \text{SBOPBT-2}$$

$$\frac{ge, le, \delta_C \vdash id \Rightarrow (pid, pins) \quad pins = ((fid_1, (n_1, bv_1)), \dots, (fid_k, (n_k, bv_k))) \quad n = n_1 + n_2 + \dots + n_k \quad \exists i. fid = fid_i \quad \delta_C \text{ is } \delta_A, \delta_{B0} \text{ or } \delta_{B1}}{ge, le, \delta_C \vdash Efield(id, fid) \Rightarrow fdacc(id, n, n_1 + \dots + n_{i-1}, n_1 + \dots + n_i - 1, bv_i)} \text{SEFIELD}$$

$$\frac{ge, le, \delta_C \vdash e_1 \Rightarrow regacc(n, n_1, n_2, bv) \quad ge, le, \delta_C \vdash e_2 \Rightarrow n' \quad 0 \leq n_2 \leq n_1 < n \quad 0 \leq n' \leq n_1 - n_2 \quad b = get_binary_bit(bv, n') \quad \delta_C \text{ is } \delta_A, \delta_{B0} \text{ or } \delta_{B1}}{ge, le, \delta_C \vdash EFieldBit(e_1, e_2) \Rightarrow regacc(n, n_2 + n', n_2 + n', b)} \text{SFB-1}$$

$$\frac{ge, le, \delta_A, \xi_\rho \vdash e_1 \Rightarrow regacc(n, n_1, n_2, bv) \quad ge, le, \delta_A, \xi_\rho \vdash e_2 \Rightarrow n' \quad 0 \leq n_2 \leq n_1 < n \quad 0 \leq n' \leq n_1 - n_2 \quad b = get_binary_bit(bv, n')}{ge, le, \delta_A, \xi_\rho \vdash EFieldBit(e_1, e_2) \Rightarrow regacc(n, n_2 + n', n_2 + n', b)} \text{SFB-1'}$$

$$\frac{\begin{array}{c} ge, le, \delta_C \vdash e_1 \Rightarrow fdacc(id, n, n_1, n_2, bv) \\ ge, le, \delta_C \vdash e_2 \Rightarrow n' \quad 0 \leq n_1 \leq n_2 < n \quad 0 \leq n' \leq n_2 - n_1 \\ b = get_binary_bit(bv, n') \quad \delta_C \text{ is } \delta_A, \delta_{B0} \text{ or } \delta_{B1} \end{array}}{ge, le, \delta_C \vdash EFieldBit(e_1, e_2) : fdacc(id, n, n_1 + n', n_1 + n', b)} \text{ SFB-2}$$

$$\frac{\begin{array}{c} ge, le, \delta_A, \xi_\rho \vdash e_1 \Rightarrow fdacc(id, n, n_1, n_2, bv) \\ ge, le, \delta_A, \xi_\rho \vdash e_2 \Rightarrow n' \quad 0 \leq n_1 \leq n_2 < n \\ 0 \leq n' \leq n_2 - n_1 \quad b = get_binary_bit(bv, n') \end{array}}{ge, le, \delta_A, \xi_\rho \vdash EFieldBit(e_1, e_2) : fdacc(id, n, n_1 + n', n_1 + n', b)} \text{ SFB-2'}$$

$$\frac{\begin{array}{c} ge, le, \delta_C \vdash e_1 \Rightarrow regacc(n, n_1, n_2, bv) \quad ge, le, \delta_C \vdash e_2 \Rightarrow n' \\ ge, le, \delta_C \vdash e_3 \Rightarrow n'' \quad 0 \leq n_2 \leq n_1 < n \quad 0 \leq n'' \leq n' \leq n_1 - n_2 \\ bv' = get_binary_bits(bv, n', n'') \quad \delta_C \text{ is } \delta_A, \delta_{B0} \text{ or } \delta_{B1} \end{array}}{ge, le, \delta_C \vdash EFieldSection(e_1, e_2, e_3) \Rightarrow regacc(n, n_2 + n', n_2 + n'', bv')} \text{ SFS-1}$$

$$\frac{\begin{array}{c} ge, le, \delta_A, \xi_\rho \vdash e_1 \Rightarrow regacc(n, n_1, n_2, bv) \\ ge, le, \delta_C \vdash e_2 \Rightarrow n' \quad ge, le, \delta_C \vdash e_3 \Rightarrow n'' \quad 0 \leq n_2 \leq n_1 < n \\ 0 \leq n'' \leq n' \leq n_1 - n_2 \quad bv' = get_binary_bits(bv, n', n'') \end{array}}{ge, le, \delta_A, \xi_\rho \vdash EFieldSection(e_1, e_2, e_3) \Rightarrow regacc(n, n_2 + n', n_2 + n'', bv')} \text{ SFS-1'}$$

$$\frac{\begin{array}{c} ge, le, \delta_C \vdash e_1 \Rightarrow fdacc(id, n, n_1, n_2, bv) \quad ge, le, \delta_C \vdash e_2 : (Int, n') \\ ge, le, \delta_C \vdash e_3 : (Int, n'') \quad 0 \leq n_1 \leq n_2 < n \quad 0 \leq n' \leq n_2 - n_1 \\ bv' = get_binary_bits(bv, n', n'') \quad \delta_C \text{ is } \delta_A, \delta_{B0} \text{ or } \delta_{B1} \end{array}}{ge, le, \delta_C \vdash EFieldSection(e_1, e_2, e_3) : fdacc(id, n, n_1 + n'', n_1 + n', bv')} \text{ SFS-2}$$

$$\frac{\begin{array}{c} ge, le, \delta_A, \xi_\rho \vdash e_1 \Rightarrow fdacc(id, n, n_1, n_2, bv) \\ ge, le, \delta_A, \xi_\rho \vdash e_2 : (Int, n') \\ ge, le, \delta_A, \xi_\rho \vdash e_3 : (Int, n'') \quad 0 \leq n_1 \leq n_2 < n \\ 0 \leq n' \leq n_2 - n_1 \quad bv' = get_binary_bits(bv, n', n'') \end{array}}{ge, le, \delta_A, \xi_\rho \vdash EFieldSection(e_1, e_2, e_3) : fdacc(id, n, n_1 + n'', n_1 + n', bv')} \text{ SFS-2'}$$

$$\frac{le = (\xi_\iota, nh, len, bp) \quad \xi_\iota \vdash id \Rightarrow (length(n), pins)}{ge, le \vdash ProtLen(id) \Rightarrow n} \text{ (SPLen)}$$

- Instructions

$$\frac{\begin{array}{l} ge, le, \delta_C \vdash e \Rightarrow v \\ ge, le, \delta_C \vdash ra \Rightarrow regacc(k, i, j, bv) \quad bv' = trans_to_bits(v, n) \\ n = i - j + 1 \quad \delta'_C = \delta_C \mid ra \Rightarrow regacc(k, i, j, bv') \quad \delta_C \text{ is } \delta_A, \delta_{B0} \text{ or } \delta_{B1} \end{array}}{ge, le \vdash (\delta_C, Set(ra, e)) \Rightarrow \delta'_C} \text{ SSET-1}$$

$$\frac{\begin{array}{l} ge, le, \delta_A, \xi_\rho \vdash e \Rightarrow v \\ ge, le, \delta_A, \xi_\rho \vdash ra \Rightarrow regacc(k, i, j, bv) \quad bv' = trans_to_bits(v, n) \\ n = i - j + 1 \quad \delta'_A = \delta_A \mid ra \Rightarrow regacc(k, i, j, bv') \end{array}}{ge, le \vdash (\delta_A, \xi_\rho, Set(ra, e)) \Rightarrow (\delta'_A, \xi_\rho)} \text{ SSET-2}$$

$$\frac{\begin{array}{l} ge, le, \delta_C \vdash e \Rightarrow v \quad mra = ra_1 ++ ra_2 ++ \dots ++ ra_m \\ ge, le, \delta_C \vdash ra_1 \Rightarrow regacc(k, i_1, j_1, bv_1) \\ ge, le, \delta_C \vdash ra_2 \Rightarrow regacc(k, i_2, j_2, bv_2) \\ \dots \quad ge, le, \delta_C \vdash ra_m \Rightarrow regacc(k, i_m, j_m, bv_m) \\ j_1 = i_2 + 1 \quad j_2 = i_3 + 1 \quad \dots \quad j_{m-1} = i_m + 1 \\ bv' = trans_to_bits(v, n) \quad n = i_1 - j_m + 1 \\ bv'_1 = bv'[i_1, j_1] \quad bv'_2 = bv'[i_2, j_2] \quad \dots \quad bv'_m = bv'[i_m, j_m] \\ \delta'_C = \delta_C \mid ra_1 \Rightarrow regacc(k, i_1, j_1, bv'_1), ra_2 \Rightarrow regacc(k, i_2, j_2, bv'_2), \dots, ra_m \Rightarrow regacc(k, i_m, j_m, bv'_m) \\ \delta_C \text{ is } \delta_A, \delta_{B0} \text{ or } \delta_{B1} \end{array}}{ge, le \vdash (\delta_C, Mov(mra, e)) \Rightarrow \delta'_C} \text{ SMov-1}$$

$$\frac{\begin{array}{l} ge, le, \delta_A, \xi_\rho \vdash e \Rightarrow v \quad mra = ra_1 ++ ra_2 ++ \dots ++ ra_m \\ ge, le, \delta_A, \xi_\rho \vdash ra_1 \Rightarrow regacc(k, i_1, j_1, bv_1) \\ ge, le, \delta_A, \xi_\rho \vdash ra_2 \Rightarrow regacc(k, i_2, j_2, bv_2) \\ \dots \quad ge, le, \delta_A, \xi_\rho \vdash ra_m \Rightarrow regacc(k, i_m, j_m, bv_m) \\ j_1 = i_2 + 1 \quad j_2 = i_3 + 1 \quad \dots \quad j_{m-1} = i_m + 1 \\ bv' = trans_to_bits(v, n) \quad n = i_1 - j_m + 1 \\ bv'_1 = bv'[i_1, j_1] \quad bv'_2 = bv'[i_2, j_2] \quad \dots \quad bv'_m = bv'[i_m, j_m] \\ \delta'_A = \delta_A \mid ra_1 \Rightarrow regacc(rid, i_1, j_1, bv'_1), ra_2 \Rightarrow regacc(rid, i_2, j_2, bv'_2), \dots, ra_m \Rightarrow regacc(rid, i_m, j_m, bv'_m) \end{array}}{ge, le \vdash (\delta_A, \xi_\rho, Mov(mra, e)) \Rightarrow (\delta'_A, \xi_\rho)} \text{ SMov-2}$$

$$\begin{array}{c}
ge, le, \delta_C \vdash e_1 \Rightarrow v_1 \\
ge, le, \delta_C \vdash e_2 \Rightarrow v_2 \quad ge, le, \delta_C \vdash ra \Rightarrow regacc(k, i, j, bv) \\
b = trans_to_int(v_1) == trans_to_int(v_2) \quad bv' = trans_to_bits(b, n) \\
n = i - j + 1 \quad \delta'_C = \delta_C \mid ra \Rightarrow regacc(k, i, j, bv') \quad \delta_C \text{ is } \delta_A, \delta_{B0} \text{ or } \delta_{B1} \\
\hline
ge, le \vdash (\delta_C, Eq(ra, e_1, e_2)) \Rightarrow \delta'_C \quad \text{SEQ-1}
\end{array}$$

$$\begin{array}{c}
ge, le, \delta_A, \xi_\rho \vdash e_1 \Rightarrow v_1 \\
ge, le, \delta_A, \xi_\rho \vdash e_2 \Rightarrow v_2 \quad ge, le, \delta_A, \xi_\rho \vdash ra \Rightarrow regacc(k, i, j, bv) \\
b = trans_to_int(v_1) == trans_to_int(v_2) \quad bv' = trans_to_bits(b, n) \\
n = i - j + 1 \quad \delta'_A = \delta_A \mid ra \Rightarrow regacc(k, i, j, bv') \\
\hline
ge, le \vdash (\delta_A, \xi_\rho, Eq(ra, e_1, e_2)) \Rightarrow (\delta'_A, \xi_\rho) \quad \text{SEQ-2}
\end{array}$$

$$\begin{array}{c}
ge, le, \delta_C \vdash e_1 \Rightarrow v_1 \\
ge, le, \delta_C \vdash e_2 \Rightarrow v_2 \quad ge, le, \delta_C \vdash ra \Rightarrow regacc(k, i, j, bv) \\
b = trans_to_int(v_1) > trans_to_int(v_2) \quad bv' = trans_to_bits(b, n) \\
n = i - j + 1 \quad \delta'_C = \delta_C \mid ra \Rightarrow regacc(k, i, j, bv') \quad \delta_C \text{ is } \delta_A, \delta_{B0} \text{ or } \delta_{B1} \\
\hline
ge, le \vdash (\delta_C, Lg(ra, e_1, e_2)) \Rightarrow \delta'_C \quad \text{SLG-1}
\end{array}$$

$$\begin{array}{c}
ge, le, \delta_A, \xi_\rho \vdash e_1 \Rightarrow v_1 \\
ge, le, \delta_A, \xi_\rho \vdash e_2 \Rightarrow v_2 \quad ge, le, \delta_A, \xi_\rho \vdash ra \Rightarrow regacc(k, i, j, bv) \\
b = trans_to_int(v_1) > trans_to_int(v_2) \quad bv' = trans_to_bits(b, n) \\
n = i - j + 1 \quad \delta'_A = \delta_A \mid ra \Rightarrow regacc(k, i, j, bv') \\
\hline
ge, le \vdash (\delta_A, \xi_\rho, Lg(ra, e_1, e_2)) \Rightarrow (\delta'_A, \xi_\rho) \quad \text{SLG-2}
\end{array}$$

- Action statement

$$\begin{array}{c}
\forall i : 1 \leq i \leq k. (ge \vdash (le^i, \delta_C^i, ins_i) \Rightarrow (le^{i+1}, \delta_C^{i+1})) \\
\delta_C \text{ is } \delta_A, \delta_{B0} \text{ or } \delta_{B1} \\
\hline
ge \vdash (le^1, \delta_C^1, Action(ins_1, \dots, ins_k)) \Rightarrow (le^{k+1}, \delta_C^{k+1}) \quad \text{SAS-1}
\end{array}$$

$$\begin{array}{c}
\forall i : 1 \leq i \leq k. (ge \vdash (le^i, \delta_A^i, \xi_\rho^i, ins_i) \Rightarrow le^{i+1}, (\delta_A^{i+1}, \xi_\rho^{i+1})) \\
\hline
ge, le \vdash (le^1, \delta_A^1, \xi_\rho, Action(ins_1, \dots, ins_k)) \Rightarrow (le^{k+1}, \delta_A^{k+1}, \xi_\rho^{k+1}) \quad \text{SAS-2}
\end{array}$$

- Bypass statement

$$\frac{le = (\xi_\iota, nh, len, bp) \quad \frac{ge, le, \delta_A \vdash c \Rightarrow n \quad bp' \vdash bypass(n) \quad le' = (\xi_\iota, nh, len, bp')}{ge \vdash (le, \delta_A, Bypass(c)) \Rightarrow (le', \delta_A)}}{SBYPS-1}$$

$$\frac{le = (\xi_\iota, nh, len, bp) \quad \frac{ge, le, \delta_A, \xi_\rho \vdash c \Rightarrow n \quad bp' \vdash bypass(n) \quad le' = (\xi_\iota, nh, len, bp')}{ge \vdash (le, \delta_A, \xi_\rho, Bypass(c)) \Rightarrow (le', \delta_A, \xi_\rho)}}{SBYPS-2}$$

- NextHeader statement

$$\frac{ge, le, \delta_A \vdash id \Rightarrow pid \quad le = (\xi_\iota, nh, len, bp) \quad nh' \vdash nexthead(id) \quad le' = (\xi_\iota, nh', len, bp)}{ge \vdash (le, \delta_A, NextHeader(id)) \Rightarrow (le', \delta_A)} \text{SNEXTHEADER-1}$$

$$\frac{ge, le, \delta_A, \xi_\rho \vdash id \Rightarrow pid \quad le = (\xi_\iota, nh, len, bp) \quad nh' \vdash nexthead(id) \quad le' = (\xi_\iota, nh', len, bp)}{ge \vdash (le, \delta_A, \xi_\rho, NextHeader(id)) \Rightarrow (le', \delta_A, \xi_\rho)} \text{SNEXTHEADER-2}$$

- Length statement

$$\frac{le = (\xi_\iota, nh, len, bp) \quad \frac{ge, le, \delta_A \vdash e \Rightarrow n \quad len' \vdash length(n) \quad le' = (\xi_\iota, nh, len', bp)}{ge \vdash (le, \delta_A, Length(e)) \Rightarrow (le', \delta_A)}}{SLENGTH-1}$$

$$\frac{\begin{array}{l} ge, le, \delta_A, \xi_\rho \vdash e \Rightarrow n \quad le = (\xi_\iota, nh, len, bp) \\ \text{There exists an unique protocol instance identified by id, such that } (id : (len', pins)) \in \xi_\iota \\ \xi'_\iota = \xi_\iota \mid_{id \Rightarrow (length(n), pins)} \quad le' = (\xi'_\iota, nh, len, bp) \end{array}}{ge \vdash (le, \delta_A, \xi_\rho, Length(e)) \Rightarrow (le', \delta_A, \xi_\rho)} \text{SLENGTH-2}$$

- Layer statement

$$\frac{\begin{array}{l} ls_list = (ls_1, ls_2, \dots, ls_k) \\ ge \vdash (le, \delta_C, ls_1) \Rightarrow (le^1, \delta_C^1) \quad ge \vdash (le^1, \delta_C^1, ls_1) \Rightarrow (le^2, \delta_C^2) \\ \dots \quad ge \vdash (le^{k-1}, \delta_C^{k-1}, ls_k) \Rightarrow (le^k, \delta_C^k) \quad \delta_C \text{ is } \delta_A, \delta_{B0} \text{ or } \delta_{B1} \end{array}}{ge \vdash (le, \delta_C, ls_list) \Rightarrow (le^k, \delta_C^k)} \text{SLSL}$$

$$\begin{array}{c}
if_l_list = ((e_1, l_stmts_1), (e_2, l_stmts_2), \dots, (e_k, l_stmts_k)) \quad d_l = l_stmts \\
ge, le, \delta_C \vdash e_1 \Rightarrow b_1 \quad ge, le, \delta_C \vdash e_2 \Rightarrow b_2 \quad \dots \quad ge, le, \delta_C \vdash e_k \Rightarrow b_k \\
\quad \quad \quad if\ b_1\ then\ ge \vdash (le, \delta_C, l_stmts_1) \Rightarrow (le', \delta'_C) \\
\quad \quad \quad elseif\ b_2\ then\ ge \vdash (le, \delta_C, l_stmts_2) \Rightarrow (le', \delta'_C) \\
\quad \quad \quad \dots \quad elseif\ b_k\ then\ ge \vdash (le, \delta_C, l_stmts_k) \Rightarrow (le', \delta'_C) \\
\quad \quad \quad else\ ge \vdash (le, \delta_C, l_stmts) \Rightarrow (le', \delta'_C) \quad \delta_C\ is\ \delta_A, \delta_{B0}\ or\ \delta_{B1} \\
\hline
ge \vdash (le, \delta_C, IfElseL(if_l_list, d_l)) \Rightarrow (le', \delta'_C) \quad \text{SIFEL}
\end{array}$$

- Layer local actions

$$\begin{array}{c}
caas = CellA(ca_l_s_list) \quad cb0as = CellB0(cb0_l_s_list) \\
cb1as = CellB1(cb1_l_s_list) \quad ge \vdash (le, \delta_A, ca_l_s_list) \Rightarrow (le', \delta'_A) \\
\quad \quad \quad ge \vdash (le', \delta_{B0}, cb0_l_s_list) \Rightarrow (le', \delta'_{B0}) \\
\quad \quad \quad ge \vdash (le', \delta_{B1}, cb1_l_s_list) \Rightarrow (le', \delta'_{B1}) \\
\hline
ge \vdash (le, LocalActions(caas, cb0as, cb1as)) \Rightarrow le' \quad \text{SLLA}
\end{array}$$

- Layer action

$$\frac{ge \vdash (le_{id}, las) \Rightarrow le'_{id}}{\emptyset \vdash (ge, LayerAction(id, lvs, lrd, ld, las)) \Rightarrow ge} \quad \text{SLA}$$

- Protocol statement

$$\begin{array}{c}
ps_list = (ps_1, ps_2, \dots, ps_k) \quad ge \vdash (le, \delta_A, \xi_\rho, ps_1) \Rightarrow (le^1, \delta_A^1, \xi_\rho) \\
\quad \quad \quad ge \vdash (le^1, \delta_A^1, \xi_\rho, ps_1) \Rightarrow (le^2, \delta_A^2, \xi_\rho) \\
\quad \quad \quad \dots \quad ge \vdash (le^{k-1}, \delta_A^{k-1}, \xi_\rho, ps_k) \Rightarrow (le^k, \delta_A^k, \xi_\rho) \\
\hline
ge \vdash (le, \delta_A, \xi_\rho, ps_list) \Rightarrow (le^k, \delta_A^k, \xi_\rho) \quad \text{SPSL}
\end{array}$$

$$\begin{array}{c}
if_p_list = ((e_1, p_stmts_1), (e_2, p_stmts_2), \dots, (e_k, p_stmts_k)) \\
d_p = p_stmts \\
ge, le, \delta_A, \xi_\rho \vdash e_1 \Rightarrow b_1 \quad ge, le, \delta_A, \xi_\rho \vdash e_2 \Rightarrow b_2 \quad \dots \quad ge, le, \delta_A, \xi_\rho \vdash e_k \Rightarrow b_k \\
\quad \quad \quad if\ b_1\ then\ ge \vdash (le, \delta_A, \xi_\rho, p_stmts_1) \Rightarrow (le', \delta'_A, \xi_\rho) \\
\quad \quad \quad elseif\ b_2\ then\ ge \vdash (le, \delta_A, \xi_\rho, p_stmts_2) \Rightarrow (le', \delta'_A, \xi_\rho) \\
\quad \quad \quad \dots \quad elseif\ b_k\ then\ ge \vdash (le, \delta_A, \xi_\rho, p_stmts_k) \Rightarrow (le', \delta'_A, \xi_\rho) \\
\quad \quad \quad else\ ge \vdash (le, \delta_A, \xi_\rho, p_stmts) \Rightarrow (le', \delta'_A, \xi_\rho) \\
\hline
ge \vdash (le, \delta_A, \xi_\rho, IfElseL(if_p_list, d_p)) \Rightarrow (le', \delta'_A, \xi_\rho) \quad \text{SIFEP}
\end{array}$$

- Protocol declaration

$$\frac{ge \vdash (le, \delta_A, \xi_\rho, p_stmts) \Rightarrow (le', \delta'_A, \xi_\rho)}{ge \vdash (le, \delta_A, \xi_\rho, Protocol(fields, p_stmts)) \Rightarrow (le', \delta'_A, \xi_\rho)} \text{SPROTOCOL}$$

- Global declarations

$$\frac{\begin{array}{l} ge = (\gamma, \sigma, \delta) \quad \gamma = (lr, cr, ps, ls, \iota, \rho) \\ \forall lid \in dom(\iota). (le_{lid} = (\xi_l^{lid}, \dots) \wedge \exists id, pins. \xi_l^{lid} \vdash id \Rightarrow (len, pins) \\ \rightarrow ge \vdash (le_{lid}, \delta_A^{lid}, \xi_\rho^{pid}, p) \Rightarrow (le'_{lid}, \delta'_A^{lid}, \xi_\rho^{pid})) \end{array}}{\emptyset \vdash (ge, ProtocolDecl(pid, p)) \Rightarrow ge} \text{SPDG}$$

7.3 Semantics of the P3 Assembly

7.3.1 Semantic environment

In most of the cases, a semantic environment maps variables to the values and memory for registers and fields, and has the form

$$\mathcal{E} ::= [x_1 : v_1, x_2 : v_2, \dots, x_n : v_n]$$

where $x_i \neq x_j$ for all i and j , satisfying $i \neq j$ and $(1 \leq i, j \leq n)$.

Figure 11 show all the semantic environments we use to define the semantics.

7.3.2 Judgements

The judgements used in the semantics definition can be inferred from the semantic rules in the subsection 7.3.3. To save the space, we omit to present them separately.

7.3.3 Semantic rules

- Initialization of ι , opened at the beginning of the specification and not to be closed

$$\frac{\begin{array}{l} ge = (\iota, lr, cr, \delta) \\ \iota' = \{layer_id : layer_block \mid layer_block = LayerBlock(layer_id, pins, cella, cellb0, cellb1)\} \\ ge' = (\iota', lr, cr, \delta) \end{array}}{\vdash (ge, "at-beginning-\iota") \Rightarrow ge'} \text{(AIL)}$$

Global	ge	$::= (\iota, lr, cr, \delta)$	divide global environment into four parts
	ι	$::= id \rightarrow ldef$	map a layer identifier to a layer definition
	lr	$::= lreglen(k)$	the <i>Lreglen</i> value set to k
	cr	$::= creglen(k)$	the <i>Creglen</i> value set to k
	δ	$::= \{ IRF(ofs, size, bv) \}$	The IRF environment
Layer	le	$::= (\xi, nh, len, bp, \lambda)$	divide layer local environment into five parts
	ξ	$::= id \rightarrow fdv(k, bv)$	map a protocol instance identifier to a memory
			for its fields with the size k and the bits' value bv
	nh	$::= nextheader(k)$	the <i>NextHeader</i> set to the protocol identified by
			the index (an integer k) of its identifier
	len	$::= length(k)$	the <i>Length</i> bound to an integer k
	bp	$::= bypass(k)$	the <i>Bypass</i> bound to an integer k
	λ	$::= id \rightarrow (nxt, nxt, nxt)$	map a protocol identifier to the IRF and FRA offsets
			of slots to be used future in Cell A, Cell B0 and Cell B1
	nxt	$::= irf(\{num\}) \times fra(\{num\})$	num is a hexadecimal number
Cell	ce	$::= \delta_A \mid \delta_{B0} \mid \delta_{B1}$	divide cell local environment into three parts
	δ_A	$::= (rs, idx)$	
	δ_{B0}	$::= (rs, idx)$	
	δ_{B1}	$::= (rs, idx)$	
	rs	$::= \{ IRF(ofs, size, bv) \}$	the IRF state
	idx	$::= comsindex(k)$	the commands' index k in both pb and pc_cur tables

Figure 11: Semantic Environments for the Assembly

- Initialization of lr and cr , opened at the beginning of the specification and not to be closed

$$\frac{ge = (\iota, lr, cr, \delta) \quad LrCr = Lreglen(n) Creglen(k) \quad lr' = Lreglen(n) \quad cr' = Creglen(k) \quad n = 3 * k \quad ge' = (\iota, lr', cr', \delta)}{\vdash (ge, LrCr) \Rightarrow ge'} \text{ ALRCr}$$

- Initialization of δ , initialized at the beginning of the specification (Rule AIR-1) and changed each time at the leaving of a layer context (Rule AIR-2).

$$\frac{ge = (\iota, lr, cr, \delta) \quad \delta' = \emptyset \quad ge' = (\iota, lr, cr, \delta')}{\vdash (ge, \text{"at-beginning-}\delta\text{"}) \Rightarrow ge'} \text{ (AIR-1)}$$

$$\frac{\begin{array}{l} ge = (\iota, lr, cr, \delta) \quad lr = lreglen(n) \quad cr = creglen(k) \\ n = 3 * k \quad le = (\xi, nh, len, bp, \lambda) \quad ce = (\delta_A, \delta_{B0}, \delta_{B1}) \\ \delta' = \{ IRF(2 * k + n_1, 2 * k + n_2, bva) \mid IRF(n_1, n_2, bv) \in \delta_A \} \\ \cup \{ IRF(k + n_1, k + n_2, bvb0) \mid IRF(n_1, n_2, bvb0) \in \delta_{B0} \} \\ \cup \{ IRF(n_1, n_2, bvb1) \mid IRF(n_1, n_2, bvb1) \in \delta_{B1} \} \quad ge' = (\iota, lr, cr, \delta') \\ le' = (\emptyset, null, null, null, \emptyset) \quad \delta'_C = null \quad \delta_C \text{ is } \delta_A, \delta_{B0} \text{ or } \delta_{B1} \end{array}}{\vdash (ge, le, \delta_C, \text{"layer-switch"}) \Rightarrow (ge', le', \delta'_C)} \text{ (AIR-2)}$$

- Initialization of le , opened at the beginning and closed at the end of a Layer specification

$$\frac{\begin{array}{l} ge = (\iota, lr, cr, \delta) \quad le = (\xi, nh, len, bp, \lambda) \quad ins_name \notin dom(\xi) \\ \xi' = \xi \cup \{id : fdv(ins_size, bv)\}, \text{ where all } bv\text{'s are the input from the hardware} \\ le' = (\xi', null, null, null, \emptyset) \end{array}}{ge \vdash (le, Pins(ins_name, ins_size)) \Rightarrow le'} \quad (\text{AIPINS1})$$

$$\frac{\begin{array}{l} ge = (\iota, lr, cr, \delta) \\ le = (\xi, nh, len, bp, \lambda) \quad pins = Pins(ins_name, ins_size) :: pins' \\ ge \vdash (le, Pins(ins_name, ins_size)) \Rightarrow le' \quad ge \vdash (le', pins') \Rightarrow le'' \end{array}}{ge \vdash (le, pins) \Rightarrow le''} \quad (\text{AIPINS})$$

- Initialization of δ_A at the CellA Registers specification, opened at the beginning of a Cell A specification, and closed at the leaving of the layer context

$$\frac{\begin{array}{l} ge = (\iota, lr, cr, \delta) \\ lr = (lreglen(n) \quad cr = creglen(k) \quad n = 3 * k \quad \delta_A = (rs, idx) \\ rs' = \{IRF(ofs, size, bva) \mid IRF(2 * k + ofs, size, bva) \in \delta \wedge ofs + size < k\} \\ \delta'_A = (rs', idx) \end{array}}{ge, le \vdash (\delta_A, \text{"at the beginning of Cell A"}) \Rightarrow \delta'_A} \quad (\text{AICA})$$

- Initialization of δ_{B0} at the CellB0 Registers specification, opened at the beginning of a Cell B0 specification, and closed at the leaving of the layer context

$$\frac{\begin{array}{l} ge = (\iota, lr, cr, \delta) \\ lr = (lreglen(n) \quad cr = creglen(k) \quad n = 3 * k \quad \delta_{B0} = (rs, idx) \\ rs' = \{IRF(ofs, size, bvb0) \mid IRF(k + ofs, size, bvb0) \in \delta \wedge ofs + size < k\} \\ \delta'_{B0} = (rs', idx) \end{array}}{ge, le \vdash (\delta_{B0}, \text{"at the beginning of Cell B0"}) \Rightarrow \delta'_{B0}} \quad (\text{AICB0})$$

- Initialization of δ_{B1} at the CellB0 Registers specification, opened at the beginning of a Cell B1 specification, and closed at the leaving of the layer context

$$\begin{array}{c}
ge = (\iota, lr, cr, \delta) \\
lr = (lreglen(n) \quad cr = creglen(k) \quad n = 3 * k \quad \delta_{B1} = (rs, idx) \\
rs' = \{IRF(ofs, size, bvb1) \mid IRF(ofs, size, bvb1) \in \delta \wedge ofs + size < k\} \\
\delta'_{B1} = (rs', idx) \\
\hline
ge, le \vdash (\delta_{B1}, \text{"at the beginning of Cell B1"}) \Rightarrow \delta'_{B1} \quad \text{(AICB1)}
\end{array}$$

- Expressions

$$\frac{ge = (\iota, lr, cr, \delta) \quad \sigma \vdash num \Rightarrow v \quad \delta_C \text{ is } \delta_A, \delta_{B0} \text{ or } \delta_{B1}}{ge, le, \delta_C \vdash num \Rightarrow v} \text{ ACE-1}$$

$$\frac{\delta_C = (rs, idx) \quad IRF(ofs, size, bv) \in rs \quad \delta_C \text{ is } \delta_A, \delta_{B0} \text{ or } \delta_{B1}}{ge, le, \delta_C \vdash (IRF, ofs, size) \Rightarrow bv} \text{ ACE-2}$$

$$\begin{array}{c}
le = (\xi, nh, len, bp, \lambda) \\
\xi(ins_id) = fdv(ins_size, bv') \quad ofs + size < ins_size \\
bv = substring(bv', ofs, size) \quad \delta_C \text{ is } \delta_A, \delta_{B0} \text{ or } \delta_{B1} \\
\hline
ge, le, \delta_C \vdash (ins_id, ofs, size) \Rightarrow bv \quad \text{ACE-3}
\end{array}$$

$$\frac{ge, le, \delta_C \vdash num \Rightarrow v \quad ge, le, \delta_C \vdash (IRF, ofs, size) \Rightarrow bv \quad r = \text{if } (value(bv) = v) \text{ then } \underline{true} \text{ else } \underline{false} \quad \delta_C \text{ is } \delta_A, \delta_{B0} \text{ or } \delta_{B1}}{ge, le, \delta_C \vdash ((IRF, ofs, size), num) \Rightarrow r} \text{ ACOND-1}$$

$$\frac{ge, le, \delta_C \vdash num \Rightarrow v \quad ge, le, \delta_C \vdash (ins_id, ofs, size) \Rightarrow bv \quad r = \text{if } (value(bv) = v) \text{ then } \underline{true} \text{ else } \underline{false} \quad \delta_C \text{ is } \delta_A, \delta_{B0} \text{ or } \delta_{B1}}{ge, le, \delta_C \vdash ((ins_id, ofs, size), num) \Rightarrow r} \text{ ACOND-2}$$

$$\begin{array}{c}
conds = cond :: conds' \\
ge, le, \delta_C \vdash cond \Rightarrow r_1 \quad ge, le, \delta_C \vdash conds' \Rightarrow r_2 \\
r = \text{if } (r_1 = r_2 = \underline{true}) \text{ then } \underline{true} \text{ else } \underline{false} \quad \delta_C \text{ is } \delta_A, \delta_{B0} \text{ or } \delta_{B1} \\
\hline
ge, le, \delta_C \vdash conds \Rightarrow r \quad \text{ACONDS}
\end{array}$$

- Instructions

$$\begin{array}{c}
\text{ge} = (\iota, \text{lr}, \text{cr}, \delta) \quad \sigma \vdash \text{num} \Rightarrow v \\
\delta_C = (\text{rs}, \text{idx}) \quad \text{ra} = \text{IRF}(\text{ofs}, \text{size}) \quad \text{bv}' = \text{trans_to_bits}(v, \text{size}) \\
\text{rs}' = (\text{rs} - \{\text{IRF}(\text{ofs}, \text{size}, \text{bv})\}) \cup \{\text{IRF}(\text{ofs}, \text{size}, \text{bv}')\} \\
\delta'_C = (\text{rs}', \text{idx}) \quad \delta_C \text{ is } \delta_A, \delta_{B0} \text{ or } \delta_{B1} \\
\hline
\text{ge}, \text{le} \vdash (\delta_C, \text{Set}(\text{ra}, \text{num})) \Rightarrow \delta'_C \quad \text{ASET}
\end{array}$$

$$\begin{array}{c}
\text{ge} = (\iota, \text{lr}, \text{cr}, \delta) \quad \delta_C = (\text{rs}, \text{idx}) \quad \text{ra} = \text{IRF}(\text{ofs}, \text{size}) \\
\text{ge}, \text{le}, \delta_C \vdash \text{sra} \Rightarrow v \quad \text{bv}' = \text{trans_to_bits}(v, \text{size}) \\
\text{rs}' = (\text{rs} - \{\text{IRF}(\text{ofs}, \text{size}, \text{bv})\}) \cup \{\text{IRF}(\text{ofs}, \text{size}, \text{bv}')\} \\
\delta'_C = (\text{rs}', \text{idx}) \quad \delta_C \text{ is } \delta_A, \delta_{B0} \text{ or } \delta_{B1} \\
\hline
\text{ge}, \text{le} \vdash (\delta_C, \text{Mov}(\text{ra}, \text{sra})) \Rightarrow \delta'_C \quad \text{AMov}
\end{array}$$

$$\begin{array}{c}
\text{ge} = (\iota, \text{lr}, \text{cr}, \delta) \\
\delta_C = (\text{rs}, \text{idx}) \quad \text{ra} = \text{IRF}(\text{ofs}, \text{size}) \quad \text{ge}, \text{le}, \delta_C \vdash \text{sra}_1 \Rightarrow v_1 \\
\text{ge}, \text{le}, \delta_C \vdash \text{sra}_2 \Rightarrow v_2 \quad \text{b} = (\text{trans_to_int}(v_1) == \text{trans_to_int}(v_2)) \\
\text{bv}' = \text{trans_to_bits}(\text{b}, \text{size}) \\
\text{rs}' = (\text{rs} - \{\text{IRF}(\text{ofs}, \text{size}, \text{bv})\}) \cup \{\text{IRF}(\text{ofs}, \text{size}, \text{bv}')\} \\
\delta'_C = (\text{rs}', \text{idx}) \quad \delta_C \text{ is } \delta_A, \delta_{B0} \text{ or } \delta_{B1} \\
\hline
\text{ge}, \text{le} \vdash (\delta_C, \text{Eq}(\text{ra}, \text{sra}_1, \text{sra}_2)) \Rightarrow \delta'_C \quad \text{AEQ}
\end{array}$$

$$\begin{array}{c}
\text{ge} = (\iota, \text{lr}, \text{cr}, \delta) \quad \delta_C = (\text{rs}, \text{idx}) \\
\text{ra} = \text{IRF}(\text{ofs}, \text{size}) \quad \text{ge}, \text{le}, \delta_C \vdash \text{sra}_1 \Rightarrow v_1 \quad \text{ge}, \text{le}, \delta_C \vdash \text{sra}_2 \Rightarrow v_2 \\
\text{b} = \text{trans_to_int}(v_1) > \text{trans_to_int}(v_2) \quad \text{bv}' = \text{trans_to_bits}(\text{b}, \text{size}) \\
\text{rs}' = (\text{rs} - \{\text{IRF}(\text{ofs}, \text{size}, \text{bv})\}) \cup \{\text{IRF}(\text{ofs}, \text{size}, \text{bv}')\} \\
\delta'_C = (\text{rs}', \text{idx}) \quad \delta_C \text{ is } \delta_A, \delta_{B0} \text{ or } \delta_{B1} \\
\hline
\text{ge}, \text{le} \vdash (\delta_C, \text{Lg}(\text{ra}, \text{sra}_1, \text{sra}_2)) \Rightarrow \delta'_C \quad \text{ALG}
\end{array}$$

$$\begin{array}{c}
\text{cmds} = \text{cmd} :: \text{cmds}' \quad \text{ge}, \text{le} \vdash (\delta_C, \text{cmd}) \Rightarrow \delta'_C \\
\text{ge}, \text{le} \vdash (\delta'_C, \text{cmds}') \Rightarrow \delta''_C \quad \delta_C \text{ is } \delta_A, \delta_{B0} \text{ or } \delta_{B1} \\
\hline
\text{ge}, \text{le} \vdash (\delta_C, \text{cmds}) \Rightarrow \delta''_C \quad \text{ACMDs}
\end{array}$$

- CellA

$$\begin{array}{c}
le = (\xi, nh, len, bp, \lambda) \quad \delta_A = (rs, idx) \\
ge, le, \delta_A \vdash conds \Rightarrow b \quad nh' = \text{if } (b == \text{true}) \text{ then } n_{xt_id} \text{ else } nh \\
bp' = \text{if } (b == \text{true}) \text{ then } bypas \text{ else } bp \\
idx' = \text{if } (b == \text{true}) \text{ then } sub_id \text{ else } idx \\
\delta'_A = (rs, idx') \quad le' = (\xi, nh', len, bp', \lambda) \\
\hline
ge \vdash (le, \delta_A, (hdr_id, conds, sub_id, n_{xt_id}, bypas)) \Rightarrow (le', \delta'_A) \quad \text{Acella_pb_item}
\end{array}$$

$$\begin{array}{c}
ca_pb_items = ca_pb_item :: ca_pb_items' \\
ge \vdash (le, \delta_A, ca_pb_item) \Rightarrow (le', \delta'_A) \\
ge \vdash (le', \delta'_A, ca_pb_items') \Rightarrow (le'', \delta''_A) \\
\hline
ge \vdash (le, \delta_A, Apb(ca_pb_items)) \Rightarrow (le'', \delta''_A) \quad \text{Acella_pb}
\end{array}$$

$$\begin{array}{c}
le = (\xi, nh, len, bp, \lambda) \quad \delta_A = (rs, idx) \quad ge, le \vdash (\delta_A, cmds) \Rightarrow \delta''_A \\
len' = \text{if } (sub_id == idx) \text{ then } lyr_offset \text{ else } len \\
le' = (\xi, nh, len', bp, \lambda) \quad \delta'_A = \text{if } (sub_id == idx) \text{ then } \delta''_A \text{ else } \delta_A \\
\hline
ge \vdash (le, \delta_A, (sub_id, cmds, lyr_offset)) \Rightarrow (le', \delta'_A) \quad \text{Acella_pc_cur_item}
\end{array}$$

$$\begin{array}{c}
ca_pc_cur_items = ca_pc_cur_item :: ca_pc_cur_items' \\
ge \vdash (le, \delta_A, ca_pc_cur_item) \Rightarrow (le', \delta'_A) \\
ge \vdash (le', \delta'_A, ca_pc_cur_items') \Rightarrow (le'', \delta''_A) \\
\hline
ge \vdash (le, \delta_A, ApcCur(ca_pc_cur_items)) \Rightarrow (le'', \delta''_A) \quad \text{Acella_pc_cur}
\end{array}$$

$$\begin{array}{c}
le = (\xi, nh, len, bp, \lambda) \\
ca_nxt = CellANxt(IRFOffset(n_1, \dots, n_r), ProtOffset(m_1, \dots, m_p)) \\
anxt = (irf(n_1, \dots, n_r), fra(m_1, \dots, m_p)) \\
cb0_nxt = CellB0Nxt(IRFOffset(n'_1, \dots, n'_{r'}), ProtOffset(m'_1, \dots, m'_{p'})) \\
b0nxt = (irf(n'_1, \dots, n'_{r'}), fra(m'_1, \dots, m'_{p'})) \\
cb1_nxt = CellB1Nxt(IRFOffset(n''_1, \dots, n''_{r''}), ProtOffset(m''_1, \dots, m''_{p''})) \\
b1nxt = (irf(n''_1, \dots, n''_{r''}), fra(m''_1, \dots, m''_{p''})) \\
\lambda' = \lambda \cup \{(n_{xt_id}, (anxt, b0nxt, b1nxt))\} \quad le' = (\xi, nh, len, bp, \lambda') \\
\hline
ge \vdash (le, (n_{xt_id}, ca_nxt, cb0_nxt, cb1_nxt)) \Rightarrow le' \quad \text{Acella_pc_nxt_item}
\end{array}$$

$$\begin{array}{c}
ca_pc_nxt_items = ca_pc_nxt_item :: ca_pc_nxt_items' \\
ge \vdash (le, ca_pc_nxt_item) \Rightarrow le' \\
ge \vdash (le', ca_pc_nxt_items') \Rightarrow le'' \\
\hline
ge \vdash (le, ApcNxt(ca_pc_nxt_items)) \Rightarrow le'' \quad \text{Acella_pc_nxt}
\end{array}$$

$$\begin{array}{c}
cella = CellA(cella_pb, cella_pc_cur, cella_pc_nxt) \\
ge \vdash (le, \delta_A, cella_pb) \Rightarrow (le', \delta'_A) \\
ge \vdash (le', \delta'_A, cella_pc_cur) \Rightarrow (le'', \delta''_A) \\
ge \vdash (le'', cella_pc_nxt) \Rightarrow le''' \\
\hline
ge \vdash (le, \delta_A, cella) \Rightarrow (le''', \delta''_A) \quad Acella
\end{array}$$

- CellB0

$$\frac{\delta_{B0} = (rs, idx) \quad ge, le, \delta_{B0} \vdash conds \Rightarrow b \quad idx' = \text{if } (b == \underline{true}) \text{ then } sub_id \text{ else } idx \quad \delta'_{B0} = (rs, idx')}{ge, le \vdash (\delta_{B0}, (hdr_id, conds, sub_id)) \Rightarrow \delta'_{B0}} \quad Acellb0_pb_item$$

$$\frac{\begin{array}{c} cb0_pb_items = cb0_pb_item :: cb0_pb_items' \\ ge, le \vdash (\delta_{B0}, cb0_pb_item) \Rightarrow \delta'_{B0} \\ ge, le \vdash (\delta'_{B0}, cb0_pb_items') \Rightarrow \delta''_{B0} \end{array}}{ge, le \vdash (\delta_{B0}, Apb(cb0_pb_items)) \Rightarrow \delta''_{B0}} \quad Acellb0_pb$$

$$\frac{\delta_{B0} = (rs, idx) \quad ge, le \vdash (\delta_{B0}, cmds) \Rightarrow \delta''_{B0} \quad \delta'_{B0} = \text{if } (sub_id == idx) \text{ then } \delta''_{B0} \text{ else } \delta_{B0}}{ge, le \vdash (\delta_{B0}, (sub_id, cmds)) \Rightarrow \delta'_{B0}} \quad Acellb0_pc_cur_item$$

$$\frac{\begin{array}{c} cb0_pc_cur_items = cb0_pc_cur_item :: cb0_pc_cur_items' \\ ge, le \vdash (\delta_{B0}, cb0_pc_cur_item) \Rightarrow \delta'_{B0} \\ ge, le \vdash (\delta'_{B0}, cb0_pc_cur_items') \Rightarrow \delta''_{B0} \end{array}}{ge, le \vdash (\delta_{B0}, B0pcCur(cb0_pc_cur_items)) \Rightarrow \delta''_{B0}} \quad Acellb0_pc_cur$$

$$\frac{\begin{array}{c} cellb0 = CellB0(cellb0_pb, cellb0_pc_cur) \\ ge, le \vdash (\delta_{B0}, cellb0_pb) \Rightarrow \delta'_{B0} \quad ge, le \vdash (\delta'_{B0}, cellb0_pc_cur) \Rightarrow \delta''_{B0} \end{array}}{ge, le \vdash (\delta_{B0}, cellb0) \Rightarrow \delta''_{B0}} \quad Acellb0$$

- CellB1

$$\frac{ge = (\iota, lr, cr, \delta) \quad \delta_{B1} = (rs, idx) \quad ge, le, \delta_{B1} \vdash conds \Rightarrow b \quad idx' = \text{if } (b == \text{true}) \text{ then } sub_id \text{ else } idx \quad \delta'_{B1} = (rs, idx')}{ge, le \vdash (\delta_{B1}, (hdr_id, conds, sub_id)) \Rightarrow \delta'_{B1}} \text{Acellb1_pb_item}$$

$$\frac{cb1_pb_items = cb1_pb_item :: cb1_pb_items' \quad ge, le \vdash (\delta_{B1}, cb1_pb_item) \Rightarrow \delta'_{B1} \quad ge, le \vdash (\delta'_{B1}, cb1_pb_items') \Rightarrow \delta''_{B1}}{ge, le \vdash (\delta_{B1}, \text{Apb}(cb1_pb_items)) \Rightarrow \delta''_{B1}} \text{Acellb1_pb}$$

$$\frac{\delta_{B1} = (rs, idx) \quad ge, le \vdash (\delta_{B1}, cmds) \Rightarrow \delta''_{B1} \quad \delta'_{B1} = \text{if } (sub_id == idx) \text{ then } \delta''_{B1} \text{ else } \delta_{B1}}{ge, le \vdash (\delta_{B1}, (sub_id, cmds)) \Rightarrow \delta'_{B1}} \text{Acellb1_pc_cur_item}$$

$$\frac{cb1_pc_cur_items = cb1_pc_cur_item :: cb1_pc_cur_items' \quad ge, le \vdash (\delta_{B1}, cb1_pc_cur_item) \Rightarrow \delta'_{B1} \quad ge, le \vdash (\delta'_{B1}, cb1_pc_cur_items') \Rightarrow \delta''_{B1}}{ge, le \vdash (\delta_{B1}, \text{B1pcCur}(cb1_pc_cur_items)) \Rightarrow \delta''_{B1}} \text{Acellb1_pc_cur}$$

$$\frac{cellb1 = \text{CellB1}(cellb1_pb, cellb1_pc_cur) \quad ge, le \vdash (\delta_{B1}, cellb1_pb) \Rightarrow \delta'_{B1} \quad ge, le \vdash (\delta'_{B1}, cellb1_pc_cur) \Rightarrow \delta''_{B1}}{ge, le \vdash (\delta_{B1}, cellb1) \Rightarrow \delta''_{B1}} \text{Acellb1}$$

- Layer Block

$$\frac{ge \vdash (le, pins) \Rightarrow le' \quad ge \vdash (le', \delta_A, cella) \Rightarrow (le'', \delta'_A) \quad ge, le'' \vdash (\delta_{B0}, cellb0) \Rightarrow \delta'_{B0} \quad ge, le'' \vdash (\delta_{B1}, cellb1) \Rightarrow \delta'_{B1}}{ge \vdash (le, (\delta_A, \delta_{B0}, \delta_{B1}), \text{LayerBlock}(id, pins, cella, cellb0, cellb1)) \Rightarrow (le'', (\delta'_A, \delta'_{B0}, \delta'_{B1}))} (\text{Alayer_block})$$

$$\frac{ge = (\iota, lr, cr, \delta) \quad layer_blocks = layer_block :: layer_blocks' \quad ge \vdash (le, (\delta_A, \delta_{B0}, \delta_{B1}), layer_block) \Rightarrow (le', (\delta'_A, \delta'_{B0}, \delta'_{B1})) \quad \vdash (ge, le', (\delta'_A, \delta'_{B0}, \delta'_{B1}), \text{"layer-switch"}) \Rightarrow (ge', (\emptyset, null, null, null, \emptyset), (null, null, null)) \quad \vdash (ge', layer_blocks') \Rightarrow ge''}{\vdash (ge, layer_blocks) \Rightarrow ge''} (\text{Alayer_blocks})$$

- Parser

$$\begin{array}{c}
\text{parser_asm} = \text{LrCr layer_blocks} \\
\frac{\vdash (ge, \text{"at-beginning-l"}) \Rightarrow ge_1 \quad \vdash (ge_1, \text{LrCr}) \Rightarrow ge_2 \quad \vdash (ge_2, \text{"at-beginning-l"}) \Rightarrow ge_3 \quad \vdash (ge_3, \text{layer_blocks}) \Rightarrow ge'}{\vdash (ge, \text{parser_asm}) \Rightarrow ge'} \quad (\text{Aparser})
\end{array}$$

7.4 Preserving the Semantics from AST to Assembly

We choose the translation validation approach [13] to certify the semantics preserving property in the translation from a P3 AST to the corresponding P3 assembly.

To verify the correctness of a validation function *Validate*, we should prove that $\forall S, C. \text{Validate}(S, C) = \text{true} \Rightarrow S \approx C$ [7], where *S* and *C* are a P3 AST and a P3 ASM respectively. *Validate*(S,C) = *true* indicates the success of the validation. $S \approx C$ stands for the semantic equivalence.

The validator is a component of the compiler, which will be added after the end of the translation. A transformation function with a validator can be described as [7]:

$$\begin{array}{l}
\text{Comp}'(S) = \text{match } \text{Comp}(S) \text{ with} \\
\quad | \text{Error} \rightarrow \text{Error} \\
\quad | \text{OK}(C) \rightarrow \text{if } \text{Validate}(S, C) \text{ then } \text{OK}(C) \text{ else Error}
\end{array}$$

8 Conclusion

This document is used as the manual in the design and the implementation of the P3C compiler.

Currently, we have implemented the compilation of the P3C as the requirement of the project 2017ZX01030-301-003, including the *scanning*, *parsing*, *type checking* and *translation to the ASM* as is shown in Fig.1. The translation to the configure file is implemented partially because we need the feedback from the hardware design. Unfortunately, the hardware design had been delayed for some unexpected reasons.

The verification of the P3C compiler is not the mandatory requirement of the project 2017ZX01030-301-003. However, we will continue to complete it as soon as possible for the great significance to do so.

References

- [1] The coq development team, the coq proof assistant reference manual. <http://coq.inria.fr/>.
- [2] Yves Bertot and Pierre Casteran. *Interactive Theorem Proving and Program Development - Coq'Art: The Calculus of Inductive Constructions*. Texts in Theoretical Computer Science. An EATCS Series. Springer, 2004.

- [3] Sandrine Blazy and Xavier Leroy. Mechanized semantics for the clight subset of the c language. *Journal of Automated Reasoning*, 43(3):263–288, 2009.
- [4] CompCert. <http://compcert.inria.fr>.
- [5] J.-H. Jourdan, F. Pottier, and X. Leroy. Validating lr(1) parsers. *Proceedings of 21st European Symposium on Programming, ESOP 2012, Lecture Notes in Computer Science, vol. 7211*, pages 397–416, 2012.
- [6] Xavier Leroy. Formal certification of a compiler back-end or: programming a compiler with a proof assistant. *Proceedings of the 33rd ACM SIGPLAN-SIGACT symposium on Principles of programming languages*, 41(1):42–54, January 2006.
- [7] Xavier Leroy. Formal verification of a realistic compiler. *Communications of the ACM*, 52(7):107–115, 2009.
- [8] Menhir-reference. Url. <http://soft.cs.tsinghua.edu.cn:8000>, 2018.
- [9] Greg Morrisett. Technical perspective: A compiler’s story. *Communications of the ACM*, 52(7):106–106, 2009.
- [10] V. C. Ngo, J.-P. Talpin, and T. Gautier. Translation validation for synchronous data-flow specification in the signal compiler. *Proceedings of the 35th IFIP WG 6.1 International Conference on Formal Techniques for Distributed Objects, Components, and Systems (FORTE 2015), Lecture Notes in Computer Science*, 9039:66–80, June 2015.
- [11] V. C. Ngo, J.-P. Talpin, T. Gautier, L. Besnard, , and P. Le Guernic. Verification of compiler transformations on polychronous equations. *Proceedings of IFM 2012, D. Latella and H. Treharne (Eds.)*, pages 113–127, 2012.
- [12] A. Pnueli, O. Shtrichman, and M. Siegel. Translation validation for synchronous languages. In *Proceedings of ICALP’1998. Lecture Notes in Computer Science, Volume 1443*, pages 235–246, 1998.
- [13] A. Pnueli, M. Siegel, and E. Singerman. Translation validation. In *Proceedings of TACAS’98, Lecture Notes in Computer Science*, 1384:151–166, 1998.
- [14] M. Ryabtsev and O. Strichman. Translation validation: From simulink to c. In *Proceedings of the 21st International Conference on Computer Aided Verification (CAV 2009), volume 5643 of Lecture Notes in Computer Science*, pages 696–701, June 2009.