



## 1. Description

### 1.1. Project

Project Name	MX_Pig_V1
Board Name	NUCLEO-F103RB
Generated with:	STM32CubeMX 6.1.2
Date	04/28/2022

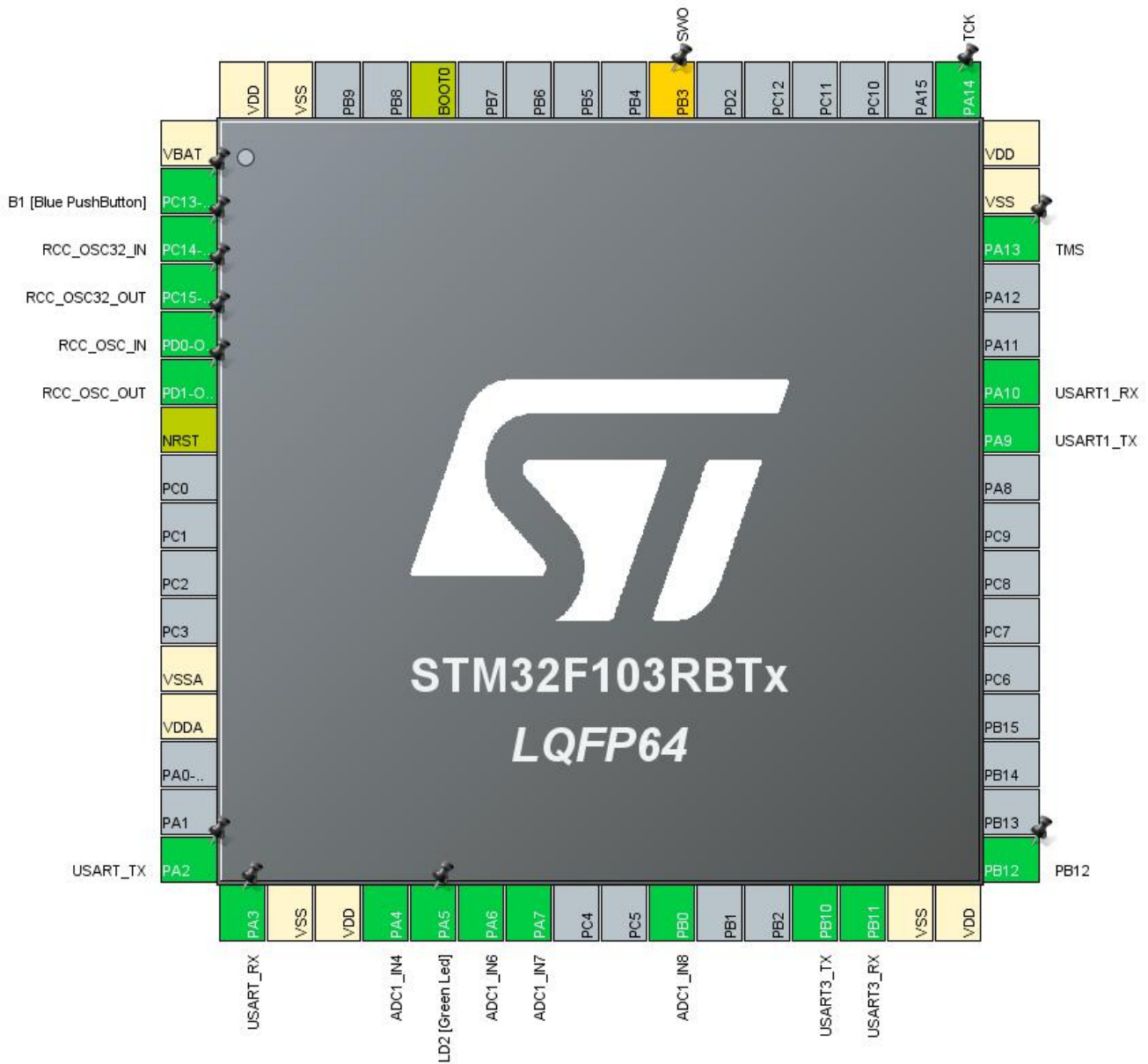
### 1.2. MCU

MCU Series	STM32F1
MCU Line	STM32F103
MCU name	STM32F103RBTx
MCU Package	LQFP64
MCU Pin number	64

### 1.3. Core(s) information

Core(s)	Arm Cortex-M3
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## 2. Pinout Configuration



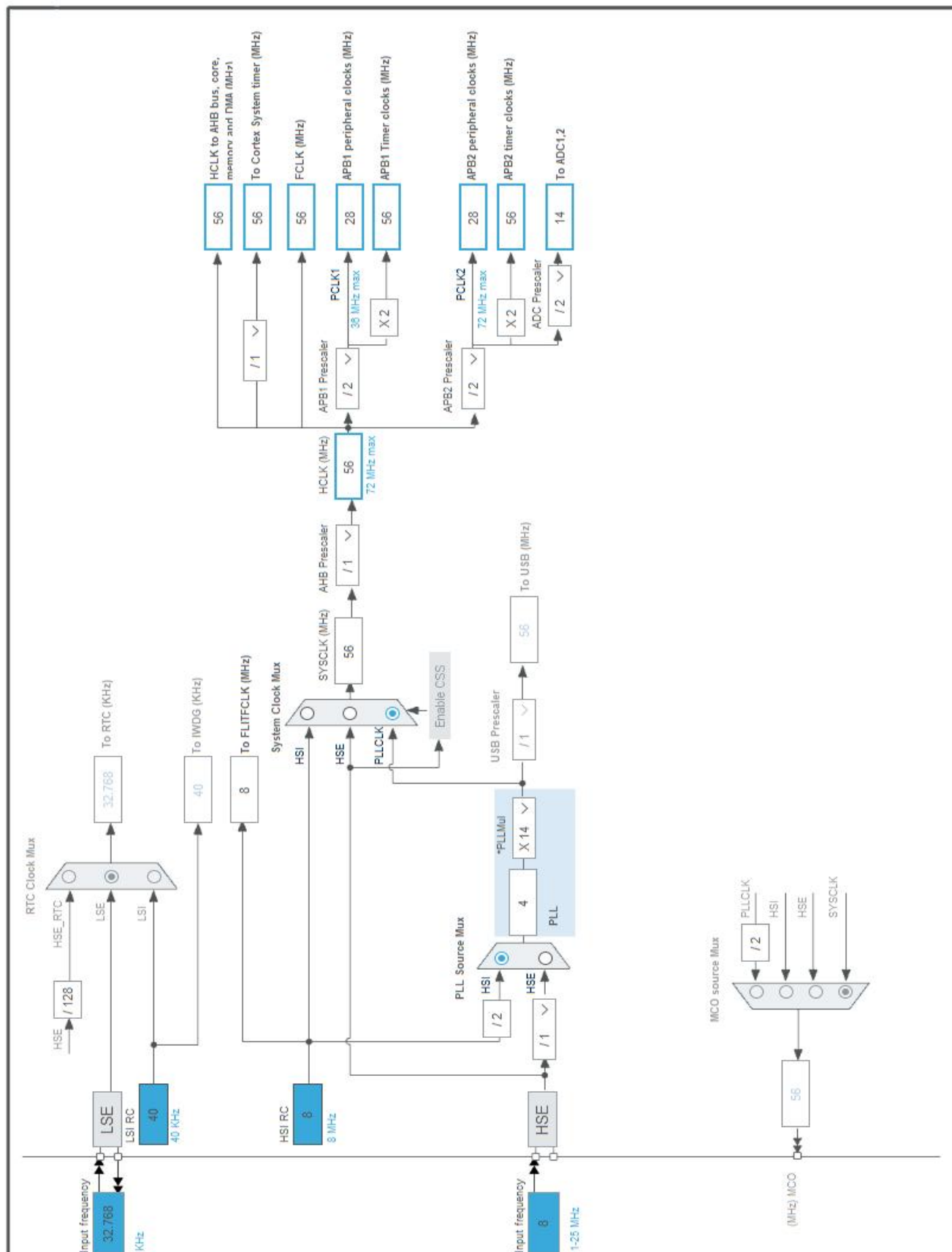
### 3. Pins Configuration

Pin Number LQFP64	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	VBAT	Power		
2	PC13-TAMPER-RTC	I/O	GPIO_EXTI13	B1 [Blue PushButton]
3	PC14-OSC32_IN	I/O	RCC_OSC32_IN	
4	PC15-OSC32_OUT	I/O	RCC_OSC32_OUT	
5	PD0-OSC_IN	I/O	RCC_OSC_IN	
6	PD1-OSC_OUT	I/O	RCC_OSC_OUT	
7	NRST	Reset		
12	VSSA	Power		
13	VDDA	Power		
16	PA2	I/O	USART2_TX	USART_TX
17	PA3	I/O	USART2_RX	USART_RX
18	VSS	Power		
19	VDD	Power		
20	PA4	I/O	ADC1_IN4	
21	PA5 *	I/O	GPIO_Output	LD2 [Green Led]
22	PA6	I/O	ADC1_IN6	
23	PA7	I/O	ADC1_IN7	
26	PB0	I/O	ADC1_IN8	
29	PB10	I/O	USART3_TX	
30	PB11	I/O	USART3_RX	
31	VSS	Power		
32	VDD	Power		
33	PB12 *	I/O	GPIO_Output	PB12
42	PA9	I/O	USART1_TX	USART1_TX
43	PA10	I/O	USART1_RX	USART1_RX
46	PA13	I/O	SYS_JTMS-SWDIO	TMS
47	VSS	Power		
48	VDD	Power		
49	PA14	I/O	SYS_JTCK-SWCLK	TCK
55	PB3 **	I/O	SYS_JTDO-TRACESWO	SWO
60	BOOT0	Boot		
63	VSS	Power		
64	VDD	Power		

\* The pin is affected with an I/O function

\*\* The pin is affected with a peripheral function but no peripheral mode is activated

## 4. Clock Tree Configuration



## 5. Software Project

### 5.1. Project Settings

Name	Value
Project Name	MX_Pig_V1.0
Project Folder	F:\code\MX_Pig_V1.0
Toolchain / IDE	MDK-ARM V5.27
Firmware Package Name and Version	STM32Cube FW_F1 V1.8.4
Application Structure	Advanced
Generate Under Root	No
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x400

### 5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	Yes
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No
Enable Full Assert	No

### 5.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	MX_GPIO_Init	GPIO
2	MX_DMA_Init	DMA
3	SystemClock_Config	RCC
4	MX_USART2_UART_Init	USART2
5	MX_USART1_UART_Init	USART1
6	MX_USART3_UART_Init	USART3
7	MX_ADC1_Init	ADC1
8	MX_TIM3_Init	TIM3

## 6. Power Consumption Calculator report

### 6.1. Microcontroller Selection

Series	STM32F1
Line	STM32F103
MCU	STM32F103RBTx
Datasheet	DS5319_Rev17

### 6.2. Parameter Selection

Temperature	25
Vdd	3.3

### 6.3. Battery Selection

Battery	Li-SOCL2(A3400)
Capacity	3400.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	100.0 mA
Max Pulse Current	200.0 mA
Cells in series	1
Cells in parallel	1



#### 6.4. Sequence

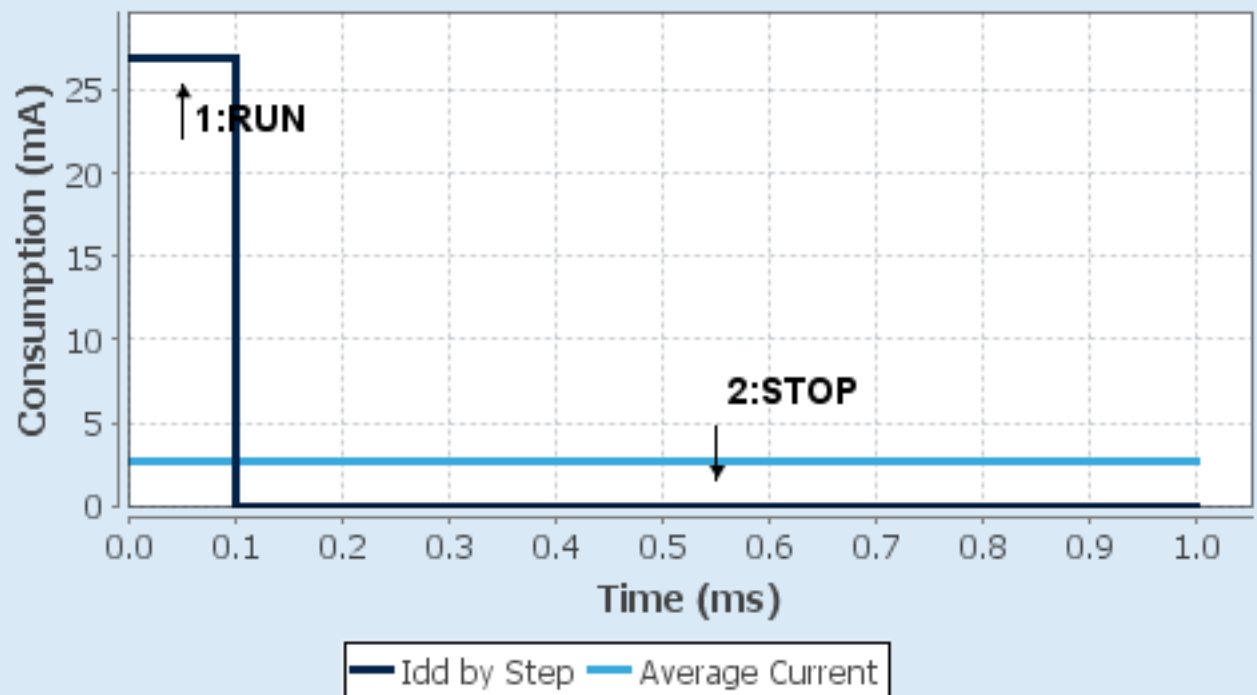
<b>Step</b>	Step1	Step2
<b>Mode</b>	RUN	STOP
<b>Vdd</b>	3.3	3.3
<b>Voltage Source</b>	Battery	Battery
<b>Range</b>	No Scale	No Scale
<b>Fetch Type</b>	FLASH	n/a
<b>CPU Frequency</b>	72 MHz	0 Hz
<b>Clock Configuration</b>	HSE PLL	Regulator LP
<b>Clock Source Frequency</b>	8 MHz	0 Hz
<b>Peripherals</b>		
<b>Additional Cons.</b>	0 mA	0 mA
<b>Average Current</b>	27 mA	14 $\mu$ A
<b>Duration</b>	0.1 ms	0.9 ms
<b>DMIPS</b>	90.0	0.0
<b>Ta Max</b>	100.99	105
<b>Category</b>	In DS Table	In DS Table

#### 6.5. Results

Sequence Time	1 ms	Average Current	2.71 mA
Battery Life	1 month, 21 days, 17 hours	Average DMIPS	61.0 DMIPS

#### 6.6. Chart

## Consumption Profile by Step



## 7. Peripherals and Middlewares Configuration

### 7.1. ADC1

mode: IN4

mode: IN6

mode: IN7

mode: IN8

mode: Temperature Sensor Channel

mode: Vrefint Channel

#### 7.1.1. Parameter Settings:

##### ADCs\_Common\_Settings:

Mode Independent mode

##### ADC\_Settings:

Data Alignment Right alignment

Scan Conversion Mode Enabled

Continuous Conversion Mode Disabled

Discontinuous Conversion Mode **Enabled \***

Number Of Discontinuous Conversions 1

##### ADC\_Regular\_ConversionMode:

Enable Regular Conversions Enable

Number Of Conversion **6 \***

External Trigger Conversion Source Regular Conversion launched by software

Rank 1

Channel Channel 4

Sampling Time **71.5 Cycles \***

Rank **2 \***

Channel **Channel 6 \***

Sampling Time **71.5 Cycles \***

Rank **3 \***

Channel **Channel 7 \***

Sampling Time **71.5 Cycles \***

Rank **4 \***

Channel **Channel 8 \***

Sampling Time **71.5 Cycles \***

Rank **5 \***

Channel **Channel Temperature Sensor \***

Sampling Time **71.5 Cycles \***

Rank	6 *
Channel	Channel Vrefint *
Sampling Time	71.5 Cycles *
<b>ADC_Injected_ConversionMode:</b>	
Enable Injected Conversions	Disable
<b>WatchDog:</b>	
Enable Analog WatchDog Mode	false

## 7.2. RCC

**High Speed Clock (HSE): BYPASS Clock Source**

**Low Speed Clock (LSE) : Crystal/Ceramic Resonator**

### 7.2.1. Parameter Settings:

#### **System Parameters:**

VDD voltage (V)	3.3
Prefetch Buffer	Enabled
Flash Latency(WS)	2 WS (3 CPU cycle)

#### **RCC Parameters:**

HSI Calibration Value	16
HSE Startup Timeout Value (ms)	100
LSE Startup Timeout Value (ms)	5000

## 7.3. SYS

**Debug: Serial Wire**

**Timebase Source: TIM1**

## 7.4. TIM3

**Clock Source : Internal Clock**

### 7.4.1. Parameter Settings:

#### **Counter Settings:**

Prescaler (PSC - 16 bits value)	3600-1 *
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value )	100-1 *
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

**Trigger Output (TRGO) Parameters:**

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

## 7.5. USART1

**Mode: Asynchronous**

7.5.1. Parameter Settings:

**Basic Parameters:**

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

**Advanced Parameters:**

Data Direction	Receive and Transmit
Over Sampling	16 Samples

## 7.6. USART2

**Mode: Asynchronous**

7.6.1. Parameter Settings:

**Basic Parameters:**

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

**Advanced Parameters:**

Data Direction	Receive and Transmit
Over Sampling	16 Samples

## 7.7. USART3

**Mode: Asynchronous**

7.7.1. Parameter Settings:

**Basic Parameters:**

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

**Advanced Parameters:**

Data Direction	Receive and Transmit
Over Sampling	16 Samples

## 7.8. FREERTOS

### Interface: CMSIS\_V1

#### 7.8.1. Config parameters:

**API:**

FreeRTOS API	CMSIS v1
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**Versions:**

FreeRTOS version	10.0.1
CMSIS-RTOS version	1.02

**Kernel settings:**

USE_PREEMPTION	Enabled
CPU_CLOCK_HZ	SystemCoreClock
TICK_RATE_HZ	1000
MAX_PRIORITIES	<b>18 *</b>
MINIMAL_STACK_SIZE	128
MAX_TASK_NAME_LEN	16
USE_16_BIT_TICKS	Disabled
IDLE_SHOULD_YIELD	Enabled
USE_MUTEXES	Enabled
USE_RECURSIVE_MUTEXES	Disabled
USE_COUNTING_SEMAPHORES	Disabled
QUEUE_REGISTRY_SIZE	8
USE_APPLICATION_TASK_TAG	Disabled
ENABLE_BACKWARD_COMPATIBILITY	Enabled
USE_PORT_OPTIMISED_TASK_SELECTION	Enabled
USE_TICKLESS_IDLE	Disabled
USE_TASK_NOTIFICATIONS	Enabled
RECORD_STACK_HIGH_ADDRESS	Disabled

**Memory management settings:**

Memory Allocation	<b>Dynamic *</b>
TOTAL_HEAP_SIZE	<b>10240 *</b>

Memory Management scheme heap\_4

**Hook function related definitions:**

USE_IDLE_HOOK	Disabled
USE_TICK_HOOK	Disabled
USE_MALLOC_FAILED_HOOK	Disabled
USE_DAEMON_TASK_STARTUP_HOOK	Disabled
CHECK_FOR_STACK_OVERFLOW	Disabled

**Run time and task stats gathering related definitions:**

GENERATE_RUN_TIME_STATS	Disabled
USE_TRACE_FACILITY	Disabled
USE_STATS_FORMATTING_FUNCTIONS	Disabled

**Co-routine related definitions:**

USE_CO_ROUTINES	Disabled
MAX_CO_ROUTINE_PRIORITIES	2

**Software timer definitions:**

USE_TIMERS	Disabled
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**Interrupt nesting behaviour configuration:**

LIBRARY_LOWEST_INTERRUPT_PRIORITY	15
LIBRARY_MAX_SYSCALL_INTERRUPT_PRIORITY	5

## 7.8.2. Include parameters:

**Include definitions:**

vTaskPrioritySet	Enabled
uxTaskPriorityGet	Enabled
vTaskDelete	Enabled
vTaskCleanUpResources	Disabled
vTaskSuspend	Enabled
vTaskDelayUntil	Disabled
vTaskDelay	Enabled
xTaskGetSchedulerState	Enabled
xTaskResumeFromISR	Enabled
xQueueGetMutexHolder	Disabled
xSemaphoreGetMutexHolder	Disabled
pcTaskGetTaskName	Disabled
uxTaskGetStackHighWaterMark	Disabled
xTaskGetCurrentTaskHandle	Disabled
eTaskGetState	Disabled
xEventGroupSetBitFromISR	Disabled
xTimerPendFunctionCall	Disabled
xTaskAbortDelay	Disabled

xTaskGetHandle	Disabled
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### 7.8.3. Advanced settings:

#### **Newlib settings (see parameter description first):**

USE_NEWLIB_REENTRANT	Disabled
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#### **Project settings (see parameter description first):**

Use FW pack heap file	Enabled
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\* User modified value



## 8. System Configuration

### 8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PA4	ADC1_IN4	Analog mode	n/a	n/a	
	PA6	ADC1_IN6	Analog mode	n/a	n/a	
	PA7	ADC1_IN7	Analog mode	n/a	n/a	
	PB0	ADC1_IN8	Analog mode	n/a	n/a	
RCC	PC14-OSC32_IN	RCC_OSC32_IN	n/a	n/a	n/a	
	PC15-OSC32_OUT	RCC_OSC32_OUT	n/a	n/a	n/a	
	PD0-OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	PD1-OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
SYS	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	TMS
	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	TCK
USART1	PA9	USART1_TX	Alternate Function Push Pull	n/a	High *	USART1_TX
	PA10	USART1_RX	Input mode	No pull-up and no pull-down	n/a	USART1_RX
USART2	PA2	USART2_TX	Alternate Function Push Pull	n/a	Low	USART_TX
	PA3	USART2_RX	*	No pull-up and no pull-down	n/a	USART_RX
USART3	PB10	USART3_TX	Alternate Function Push Pull	n/a	High *	
	PB11	USART3_RX	Input mode	No pull-up and no pull-down	n/a	
Single Mapped Signals	PB3	SYS_JTDO-TRACESWO	n/a	n/a	n/a	SWO
GPIO	PC13-TAMPER-RTC	GPIO_EXTI13	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	B1 [Blue PushButton]
	PA5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LD2 [Green Led]
	PB12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Medium *	PB12

## 8.2. DMA configuration

DMA request	Stream	Direction	Priority
ADC1	DMA1_Channel1	Peripheral To Memory	<b>High *</b>

### ADC1: DMA1\_Channel1 DMA request Settings:

Mode: **Circular \***  
Peripheral Increment: Disable  
Memory Increment: **Enable \***  
Peripheral Data Width: Half Word  
Memory Data Width: Half Word

### 8.3. NVIC configuration

#### 8.3.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Prefetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	15	0
System tick timer	true	15	0
DMA1 channel1 global interrupt	true	6	0
ADC1 and ADC2 global interrupts	true	5	0
TIM1 update interrupt	true	0	0
TIM3 global interrupt	true	5	0
USART1 global interrupt	true	7	0
EXTI line[15:10] interrupts	true	12	0
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
USART2 global interrupt	unused		
USART3 global interrupt	unused		

#### 8.3.2. NVIC Code generation

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Prefetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	false	false
Debug monitor	false	true	false
Pendable request for system service	false	false	false
System tick timer	false	false	true
DMA1 channel1 global interrupt	false	true	true
ADC1 and ADC2 global interrupts	false	true	true
TIM1 update interrupt	false	true	true
TIM3 global interrupt	false	true	true

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
USART1 global interrupt	false	true	true
EXTI line[15:10] interrupts	false	true	true

\* User modified value

## 9. System Views

### 9.1. Category view

#### 9.1.1. Current

#### Middleware

FREERTOS 

#### System Core

DMA 

GPIO 

NVIC 

RCC 

SYS 

#### Analog

ADC1 

#### Timers

TIM3 

#### Connectivity

USART1 

USART2 

USART3 

#### Computing

## 10. Docs & Resources

Type	Link
Datasheet	<a href="http://www.st.com/resource/en/datasheet/CD00161566.pdf">http://www.st.com/resource/en/datasheet/CD00161566.pdf</a>
Reference manual	<a href="http://www.st.com/resource/en/reference_manual/CD00171190.pdf">http://www.st.com/resource/en/reference_manual/CD00171190.pdf</a>
Programming manual	<a href="http://www.st.com/resource/en/programming_manual/CD00228163.pdf">http://www.st.com/resource/en/programming_manual/CD00228163.pdf</a>
Programming manual	<a href="http://www.st.com/resource/en/programming_manual/CD00283419.pdf">http://www.st.com/resource/en/programming_manual/CD00283419.pdf</a>
Errata sheet	<a href="http://www.st.com/resource/en/errata_sheet/CD00190234.pdf">http://www.st.com/resource/en/errata_sheet/CD00190234.pdf</a>
Application note	<a href="http://www.st.com/resource/en/application_note/CD00160362.pdf">http://www.st.com/resource/en/application_note/CD00160362.pdf</a>
Application note	<a href="http://www.st.com/resource/en/application_note/CD00164185.pdf">http://www.st.com/resource/en/application_note/CD00164185.pdf</a>
Application note	<a href="http://www.st.com/resource/en/application_note/CD00167326.pdf">http://www.st.com/resource/en/application_note/CD00167326.pdf</a>
Application note	<a href="http://www.st.com/resource/en/application_note/CD00167594.pdf">http://www.st.com/resource/en/application_note/CD00167594.pdf</a>
Application note	<a href="http://www.st.com/resource/en/application_note/CD00211314.pdf">http://www.st.com/resource/en/application_note/CD00211314.pdf</a>
Application note	<a href="http://www.st.com/resource/en/application_note/CD00249778.pdf">http://www.st.com/resource/en/application_note/CD00249778.pdf</a>
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Application note	<a href="http://www.st.com/resource/en/application_note/DM00080497.pdf">http://www.st.com/resource/en/application_note/DM00080497.pdf</a>
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Application note [http://www.st.com/resource/en/application\\_note/DM00327191.pdf](http://www.st.com/resource/en/application_note/DM00327191.pdf)  
Application note [http://www.st.com/resource/en/application\\_note/DM00354244.pdf](http://www.st.com/resource/en/application_note/DM00354244.pdf)  
Application note [http://www.st.com/resource/en/application\\_note/DM00315319.pdf](http://www.st.com/resource/en/application_note/DM00315319.pdf)  
Application note [http://www.st.com/resource/en/application\\_note/DM00380469.pdf](http://www.st.com/resource/en/application_note/DM00380469.pdf)  
Application note [http://www.st.com/resource/en/application\\_note/DM00395696.pdf](http://www.st.com/resource/en/application_note/DM00395696.pdf)  
Application note [http://www.st.com/resource/en/application\\_note/DM00493651.pdf](http://www.st.com/resource/en/application_note/DM00493651.pdf)  
Application note [http://www.st.com/resource/en/application\\_note/DM00536349.pdf](http://www.st.com/resource/en/application_note/DM00536349.pdf)