

## TPS6125x 3.5-MHz High Efficiency Step-Up Converter In Chip Scale Packaging

### 1 Features

- 93% Efficiency at 3.5-MHz Operation
- 21- $\mu$ A Quiescent Current in Standby Mode
- 37- $\mu$ A Quiescent Current in Normal Operation
- Wide  $V_{IN}$  Range From 2.3 V to 5.5 V
- $V_{IN} \geq V_{OUT}$  Operation
- $I_{OUT} \geq 800$  mA at  $V_{OUT} = 4.5$  V,  $V_{IN} \geq 2.65$  V
- $I_{OUT} \geq 1000$  mA at  $V_{OUT} = 5.0$  V,  $V_{IN} \geq 3.3$  V
- $I_{OUT} \geq 1500$  mA (Peak) at  $V_{OUT} = 5.0$  V,  $V_{IN} \geq 3.3$  V
- $\pm 2\%$  Total DC Voltage Accuracy
- Light-Load PFM Mode
- Selectable Standby Mode or True Load Disconnect During Shutdown
- Thermal Shutdown and Overload Protection
- Only Three Surface-Mount External Components Required
- Total Solution Size < 25 mm<sup>2</sup>
- 9-Pin NanoFree™ (CSP) Packaging

### 2 Applications

- Cell Phones, Smart Phones
- Mono and Stereo APA Applications
- USB Charging Ports (5V)

### 3 Description

The TPS6125x device provides a power supply solution for battery-powered portable applications. Intended for low-power applications, the TPS6125x supports up to 800-mA load current from a battery discharged as low as 2.65V and allows the use of low cost chip inductor and capacitors.

With a wide input voltage range of 2.3 V to 5.5 V, the device supports applications powered by Li-Ion batteries with extended voltage range. Different fixed voltage output versions are available from 3.15 V to 5.0 V.

The TPS6125x operates at a regulated 3.5-MHz switching frequency and enters power-save mode operation at light load currents to maintain high efficiency over the entire load current range. The PFM mode extends the battery life by reducing the quiescent current to 37  $\mu$ A (typ) during light load operation.

In addition, the TPS6125x device can also maintain its output biased at the input voltage level. In this mode, the synchronous rectifier is current limited allowing external load (e.g. audio amplifier) to be powered with a restricted supply. In this mode, the quiescent current is reduced to 21  $\mu$ A. During shutdown, the load is completely disconnected from the battery. Input current in shutdown mode is less than 1  $\mu$ A (typ), which maximizes battery life.

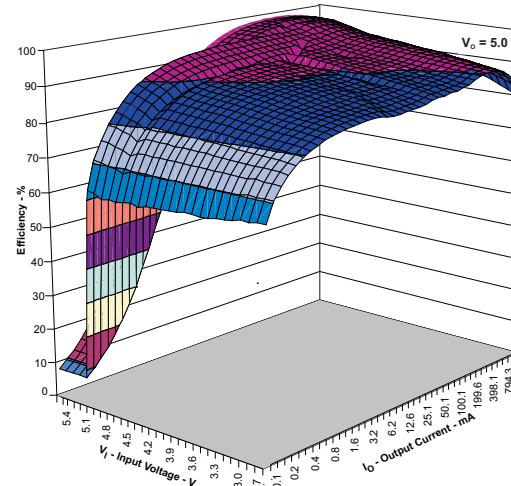
The TPS6125x offers a very small solution size due to minimum amount of external components. It allows the use of small inductors and input capacitors to achieve a small solution size.

### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS6125x	DSBGA (9)	1.206 mm × 1.306 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

### Efficiency vs Load Current



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. UNLESS OTHERWISE NOTED, this document contains PRODUCTION DATA.

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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision F (March 2016) to Revision G	Page
• Changed the <i>Package Dimensions</i> section.....	29

Changes from Revision E (March 2015) to Revision F	Page
• Added device TPS612592 .....	4

Changes from Revision D (December 2014) to Revision E	Page
• Changed Body Size (NOM) from "1.60 mm × 1.60" to "1.206 mm × 1.306" in the Device Information table.....	1
• Added table note reference to Third-Party Products Disclaimer .....	19

Changes from Revision C (August 2012) to Revision D	Page
• Added <i>ESD Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section .....	1

Changes from Revision B (May 2012) to Revision C	Page
• Added TPS61259 to data sheet header as production device.....	1
• Changed device TPS61259 to production status .....	4

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Changes from Revision A (October 2011) to Revision B	Page
• Added TPS61253 and TPS61258 to data sheet header as production devices.....	1
• Changed devices TPS61253 and TPS61258 to production status .....	4
• Changed graphic entity for <a href="#">Figure 3</a> .....	10
• Changed graphic entity for <a href="#">Figure 10</a> and <a href="#">Figure 13</a> .....	11
• Changed graphic entity for <a href="#">Figure 23</a> .....	13

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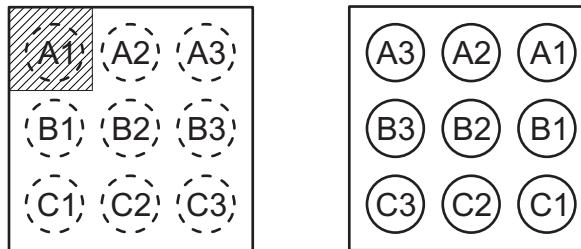
## 5 Device Options

T <sub>A</sub>	PART NUMBER <sup>(1)</sup>	OUTPUT VOLTAGE	DEVICE SPECIFIC FEATURES
-40°C to 85°C	TPS61253	5.0 V	Supports 5 V, up to 1500 mA peak loading down to 3.3 V input voltage
	TPS61254	4.5 V	Supports 4.5 V / 800 mA loading down to 2.65 V input voltage
	TPS61255 <sup>(2)</sup>	3.75 V	
	TPS61256	5.0 V	Supports 5 V / 900 mA loading down to 3.3 V input voltage
	TPS61257 <sup>(2)</sup>	4.3 V	
	TPS61258	4.5 V	Supports 4.5 V, up to 1500 mA peak loading down to 3.3 V input voltage
	TPS61259	5.1 V	Supports 5.1 V, up to 1500 mA peak loading down to 3.3 V input voltage
	TPS612592	5.2 V	Supports 5.2 V, up to 1500 mA peak loading down to 3.3 V input voltage

(1) For all available packages, see the orderable addendum at the end of the datasheet.

(2) Product preview. [Contact TI factory for more information](#)

## 6 Pin Configuration and Functions



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
BP	C3	I	This is the mode selection pin of the device and is only of relevance when the device is disabled (EN = Low). This pin must not be left floating and must be terminated. Refer to <a href="#">Table 2</a> for more details.
			BP = Low: The device is in true shutdown mode. BP = High: The output is biased at the input voltage level with a maximum load current capability of ca. 150mA. In standby mode, the device only consumes a standby current of 21µA (typ).
EN	B3	I	This is the enable pin of the device. Connecting this pin to ground forces the device into shutdown mode. Pulling this pin high enables the device. This pin must not be left floating and must be terminated.
GND	C1, C2		Ground pin.
SW	B1, B2	I/O	This is the switch pin of the converter and is connected to the drain of the internal Power MOSFETs.
VIN	A3	I	Power supply input.
VOUT	A1, A2	O	Boost converter output.

## 7 Specifications

### 7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		<b>MIN</b>	<b>MAX</b>	<b>UNIT</b>
Input voltage	Voltage at VIN <sup>(2)</sup> , VOUT <sup>(2)</sup> , SW <sup>(2)</sup> , EN <sup>(2)</sup> , BP <sup>(2)</sup>	-0.3	7	V
Input current	Continuous average current into SW <sup>(3)</sup>		1.8	A
	Peak current into SW <sup>(4)</sup>		3.5	
Power dissipation	Internally limited			
Temperature	Operating, T <sub>A</sub> <sup>(5)</sup>	-40	85	°C
	Operating virtual junction, T <sub>J</sub>	-40	150	
	Storage, T <sub>stg</sub>	-65	150	

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to network ground terminal.
- (3) Limit the junction temperature to 105°C for continuous operation at maximum output power.
- (4) Limit the junction temperature to 125°C for 5% duty cycle operation.
- (5) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature (T<sub>A(max)</sub>) is dependent on the maximum operating junction temperature (T<sub>J(max)</sub>), the maximum power dissipation of the device in the application (P<sub>D(max)</sub>), and the junction-to-ambient thermal resistance of the part/package in the application (θ<sub>JA</sub>), as given by the following equation: T<sub>A(max)</sub> = T<sub>J(max)</sub> - (θ<sub>JA</sub> × P<sub>D(max)</sub>). To achieve optimum performance, it is recommended to operate the device with a maximum junction temperature of 105°C.

### 7.2 ESD Ratings

		<b>VALUE</b>	<b>UNIT</b>
V <sub>(ESD)</sub>	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000
		Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±1000
		Machine model (MM)	±200

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions.

### 7.3 Recommended Operating Conditions

		<b>MIN</b>	<b>NOM</b>	<b>MAX</b>	<b>UNIT</b>
V <sub>I</sub>	Input voltage range	TPS61253	2.65 <sup>(1)</sup>	4.85	V
		TPS61254	2.5	4.35	
		TPS61256	2.5	4.85	
		TPS61257	2.5	4.15	
		TPS61258	2.65 <sup>(1)</sup>	4.35	
		TPS61259	2.65 <sup>(1)</sup>	4.85	
		TPS612592	2.65 <sup>(1)</sup>	4.85	
R <sub>L</sub>	Minimum resistive load for start-up	TPS6125x	55		Ω
L	Inductance		0.7	1.0	2.9
C <sub>O</sub>	Output capacitance		3.5	5	50
T <sub>A</sub>	Ambient temperature		-40	85	°C
T <sub>J</sub>	Operating junction temperature		-40	125	°C

- (1) Up to 1000mA peak output current.

## 7.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		TPS6125x	UNIT
		YFF	
		9 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	108.3	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	1.0	
R <sub>θJB</sub>	Junction-to-board thermal resistance	18	
Ψ <sub>JT</sub>	Junction-to-top characterization parameter	4.2	
Ψ <sub>JB</sub>	Junction-to-board characterization parameter	17.9	

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 7.5 Electrical Characteristics

Minimum and maximum values are at V<sub>IN</sub> = 2.3V to 5.5V, EN = 1.8V, T<sub>A</sub> = -40°C to 85°C; Circuit of Parameter Measurement Information section (unless otherwise noted). Typical values are at V<sub>IN</sub> = 3.6V, EN = 1.8V, T<sub>A</sub> = 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>SUPPLY CURRENT</b>						
I <sub>Q</sub>	Operating quiescent current into V <sub>IN</sub>	I <sub>OUT</sub> = 0mA, V <sub>IN</sub> = 3.6V EN = V <sub>IN</sub> , BP = GND Device not switching	30	45		µA
	Operating quiescent current into V <sub>OUT</sub>		7	15		µA
	Standby mode quiescent current into V <sub>IN</sub>	I <sub>OUT</sub> = 0mA, V <sub>IN</sub> = V <sub>OUT</sub> = 3.6V EN = GND, BP = V <sub>IN</sub> Device not switching	11	20		µA
	Standby mode quiescent current into V <sub>OUT</sub>		9.5	15		µA
I <sub>SD</sub>	Shutdown current	EN = GND, BP = GND	0.85	5.0		µA
V <sub>UVLO</sub>	Under-voltage lockout threshold	Falling	2.0	2.1		V
		Hysteresis	0.1			V
<b>ENABLE, BYPASS</b>						
V <sub>IL</sub>	Low-level input voltage			0.4		V
V <sub>IH</sub>	High-level input voltage		1.0			V
I <sub>Ikq</sub>	Input leakage current	Input connected to GND or V <sub>IN</sub>		0.5		µA

## Electrical Characteristics (continued)

Minimum and maximum values are at  $V_{IN} = 2.3V$  to  $5.5V$ ,  $EN = 1.8V$ ,  $T_A = -40^\circ C$  to  $85^\circ C$ ; Circuit of Parameter Measurement Information section (unless otherwise noted). Typical values are at  $V_{IN} = 3.6V$ ,  $EN = 1.8V$ ,  $T_A = 25^\circ C$  (unless otherwise noted).

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT		
<b>OUTPUT</b>										
$V_{OUT}$	Regulated DC output voltage	TPS61253	2.3V $\leq V_{IN} \leq 4.85V$ , $I_{OUT} = 0mA$ PWM operation. Open Loop	4.92	5	5.08	V			
			3.3V $\leq V_{IN} \leq 4.85V$ , 0mA $\leq I_{OUT} \leq 1000mA$ PFM/PWM operation	4.85	5	5.2				
			3.3V $\leq V_{IN} \leq 4.85V$ , 0mA $\leq I_{OUT} \leq 1500mA$ PFM/PWM operation Pulsed load test; Pulse width $\leq 20ms$ ; Duty cycle $\leq 10\%$	4.75	5	5.2				
	Regulated DC output voltage	TPS61254	2.3V $\leq V_{IN} \leq 4.35V$ , $I_{OUT} = 0mA$ PWM operation. Open Loop	4.43	4.5	4.57	V			
			2.65V $\leq V_{IN} \leq 4.35V$ , 0mA $\leq I_{OUT} \leq 800mA$ PFM/PWM operation	4.4	4.5	4.65				
	Regulated DC output voltage	TPS61256	2.3V $\leq V_{IN} \leq 4.85V$ , $I_{OUT} = 0mA$ PWM operation. Open Loop	4.92	5	5.08	V			
			2.65V $\leq V_{IN} \leq 4.85V$ , 0mA $\leq I_{OUT} \leq 700mA$ PFM/PWM operation	4.9	5	5.2				
$\Delta V_{OUT}$	Regulated DC output voltage	TPS61257	2.3V $\leq V_{IN} \leq 4.15V$ , $I_{OUT} = 0mA$ PWM operation. Open loop.	4.23	4.3	4.37	V			
			2.65V $\leq V_{IN} \leq 4.15V$ , 0mA $\leq I_{OUT} \leq 800mA$ PFM/PWM operation	4.2	4.3	4.45				
	Regulated DC output voltage	TPS61258	2.3V $\leq V_{IN} \leq 4.35V$ , $I_{OUT} = 0mA$ PWM operation. Open Loop	4.43	4.5	4.57	V			
			3.3V $\leq V_{IN} \leq 4.35V$ , 0mA $\leq I_{OUT} \leq 1500mA$ PFM/PWM operation Pulsed load test; Pulse width $\leq 20ms$ ; Duty cycle $\leq 10\%$	4.3	4.5	4.65				
	Regulated DC output voltage	TPS61259	2.3V $\leq V_{IN} \leq 4.85V$ , $I_{OUT} = 0mA$ PWM operation. Open Loop	5.02	5.1	5.18	V			
			3.4V $\leq V_{IN} \leq 4.85V$ , 0mA $\leq I_{OUT} \leq 1500mA$ PFM/PWM operation Pulsed load test; Pulse width $\leq 20ms$ ; Duty cycle $\leq 10\%$	4.75	5.1	5.3				
	Regulated DC output voltage	TPS612592	2.7V $\leq V_{IN} \leq 4.8V$ , $I_{OUT} = 0mA$ PWM operation. Open Loop	5.1	5.2	5.3	V			
$\Delta V_{OUT}$	Power-save mode output ripple voltage	TPS61254 TPS61258	PFM operation, $I_{OUT} = 1mA$	45			mVpk			
	Standby mode output ripple voltage		EN = GND, BP = $V_{IN}$ , $I_{OUT} = 0mA$	80						
	PWM mode output ripple voltage		PWM operation, $I_{OUT} = 200mA$	20						
	Power-save mode output ripple voltage	TPS61253 TPS61256 TPS61259 TPS612592	PFM operation, $I_{OUT} = 1mA$	50			mVpk			
	Standby mode output ripple voltage		EN = GND, BP = $V_{IN}$ , $I_{OUT} = 0mA$	80						

## Electrical Characteristics (continued)

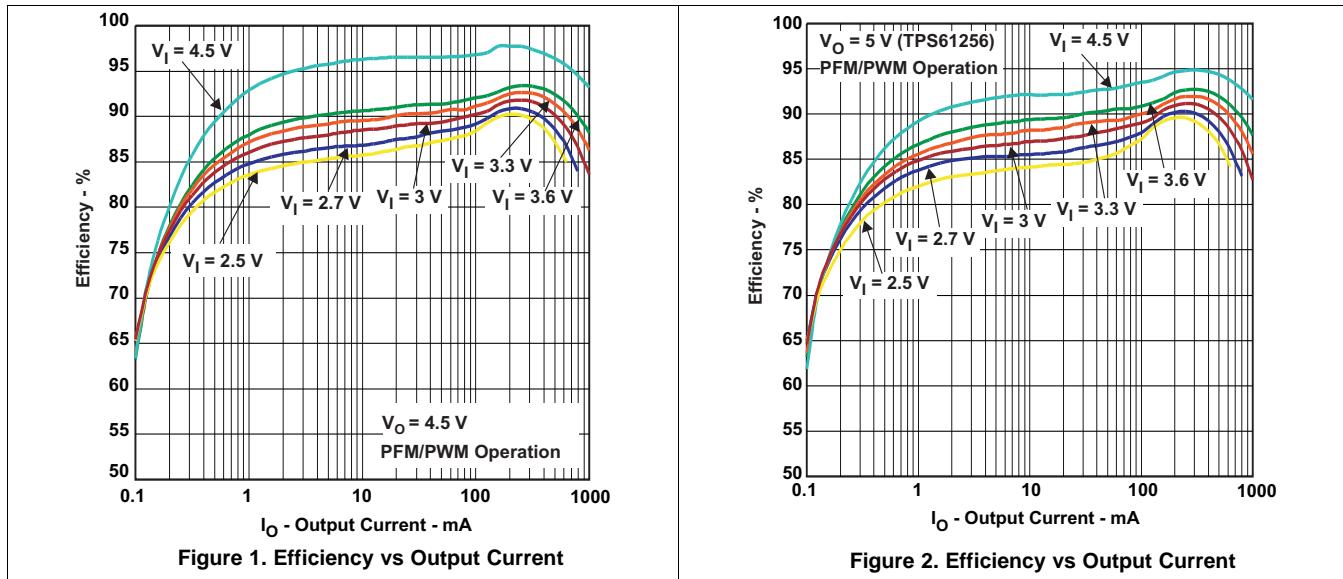
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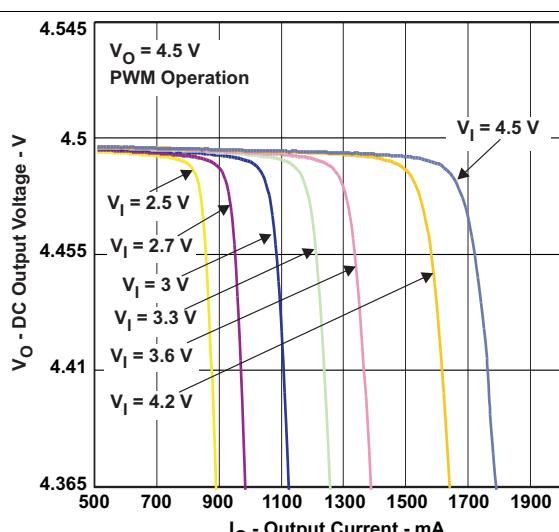
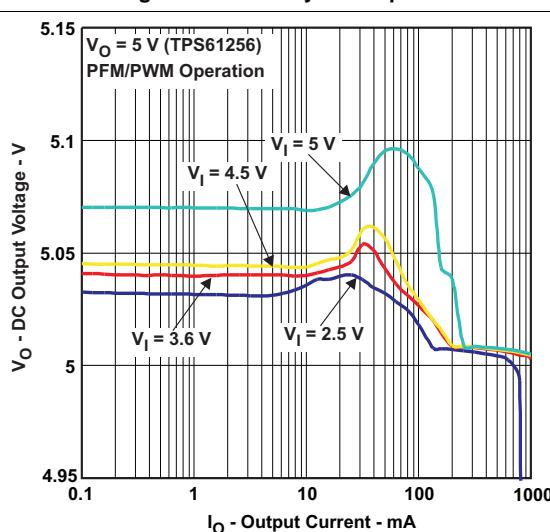
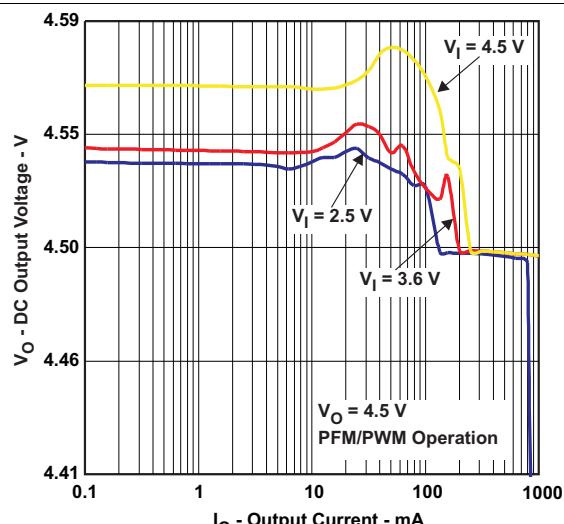
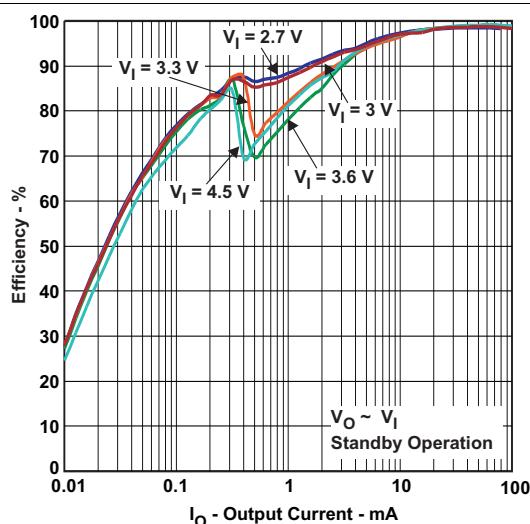
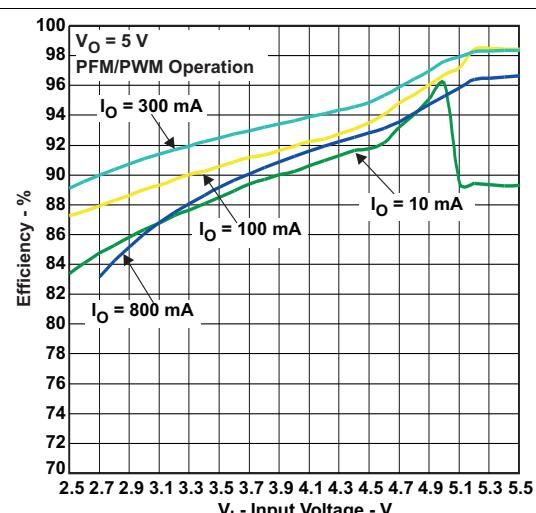
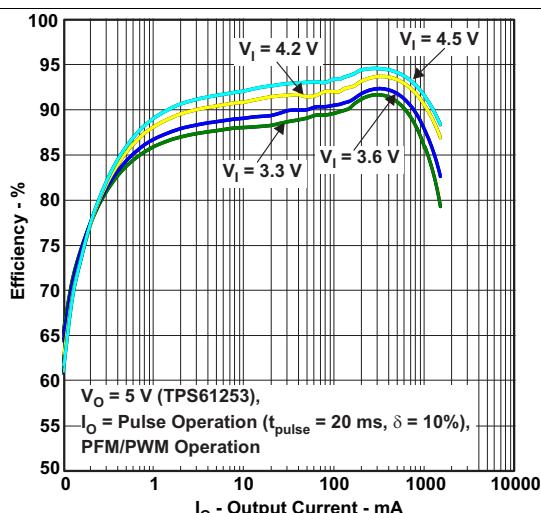
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>POWER SWITCH</b>						
$r_{DS(on)}$	High-side MOSFET on resistance		170		mΩ	
	Low-side MOSFET on resistance		100			
$I_{lkq}$	Reverse leakage current into $V_{OUT}$		EN = GND, BP = GND		3.5	µA
$I_{LIM}$	Switch valley current limit	TPS61253 TPS61258 TPS61259 TPS612592	EN = $V_{IN}$ , BP = GND. Open Loop		3300 3620 3900	mA
		TPS61254 TPS61256 TPS61257	EN = $V_{IN}$ , BP = GND. Open Loop		1900 2150 2400	
	Pre-charge mode current limit (linear mode)	EN = GND, BP = $V_{IN}$		165 215 265	mA	
Overtemperature protection						°C
Overtemperature hysteresis						°C
<b>OSCILLATOR</b>						
$f_{osc}$	Oscillator frequency	$V_{IN} = 3.6V$ $V_{OUT} = 4.5V$		3.5		MHz
<b>TIMING</b>						
Start-up time		TPS6125x	BP = GND, $I_{OUT} = 0mA$ . Time from active EN to start switching		70	µs
		TPS61253 TPS61254 TPS61256 TPS61258 TPS61259 TPS612592	BP = GND, $I_{OUT} = 0mA$ . Time from active EN to $V_{OUT}$		400	µs

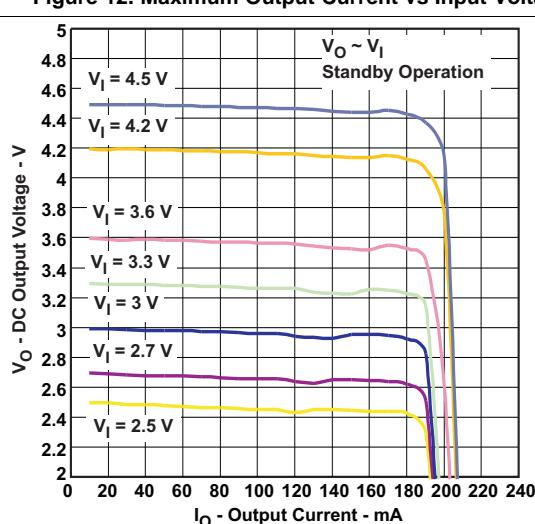
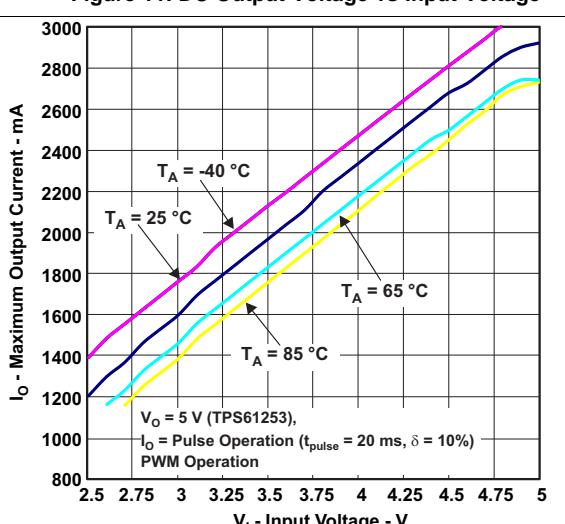
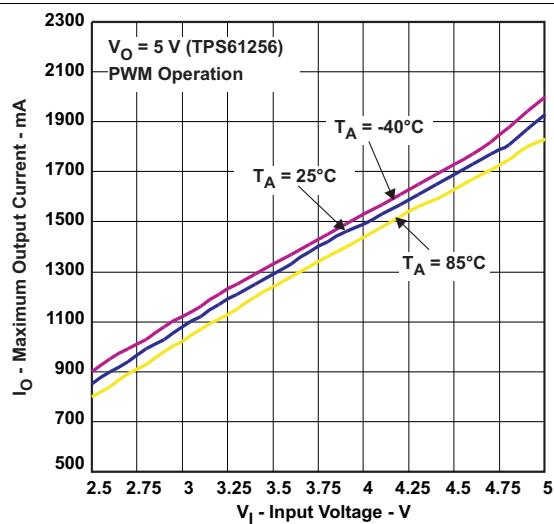
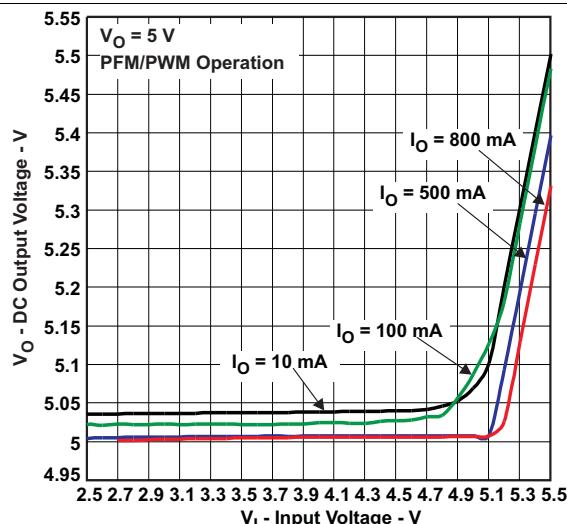
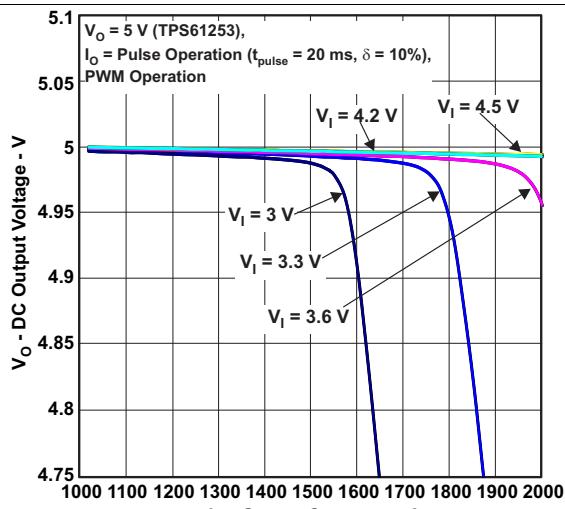
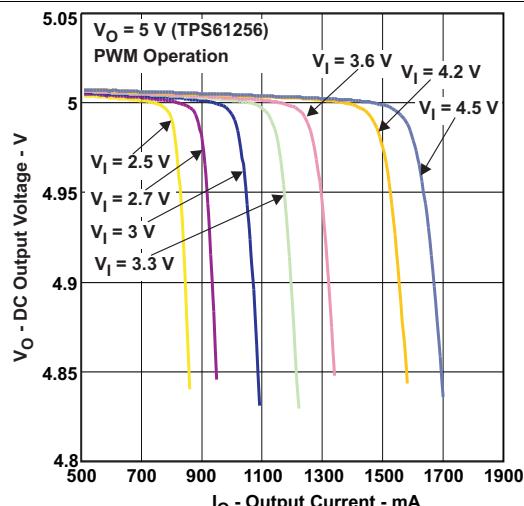
## 7.6 Typical Characteristics

**Table 1. Table of Graphs**

			FIGURE
$\eta$	Efficiency	vs Output current	Figure 1, Figure 2, Figure 3, Figure 5
		vs Input voltage	Figure 4
$V_O$	DC output voltage	vs Output current	Figure 6, Figure 7, Figure 8, Figure 9, Figure 10, Figure 14
		vs Input voltage	Figure 11
$I_O$	Maximum output current	vs Input voltage	Figure 12, Figure 13
$\Delta V_O$	Peak-to-peak output ripple voltage	vs Output current	Figure 15, Figure 16, Figure 17
$I_{CC}$	Supply current	vs Input voltage	Figure 18, Figure 19
$I_{LIM}$	DC pre-charge current	vs Differential input-output voltage	Figure 20, Figure 21
	Valley current limit	vs Temperature	Figure 22, Figure 23
$r_{DS(on)}$	MOSFET $r_{DS(on)}$	vs Temperature	Figure 24







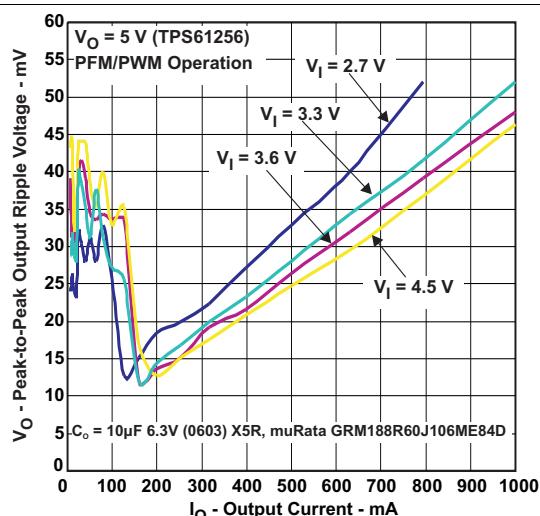


Figure 15. Peak-to-Peak Output Ripple Voltage vs Output Current

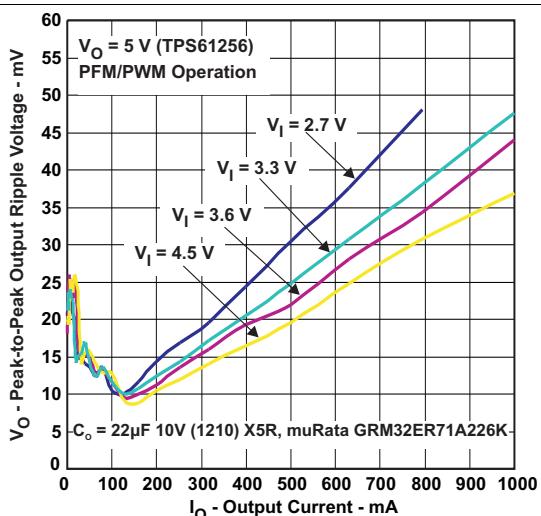


Figure 16. Peak-to-Peak Output Ripple Voltage vs Output Current

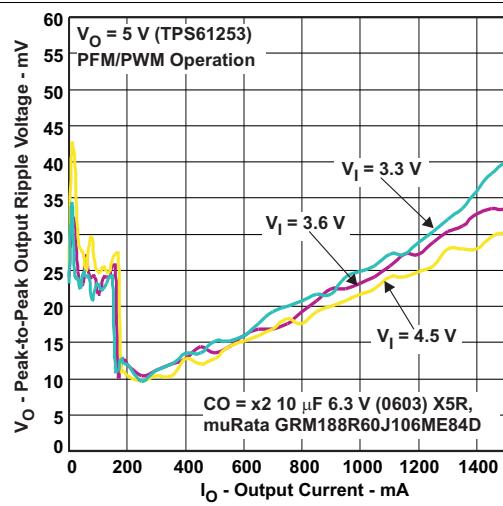


Figure 17. Peak-to-Peak Output Ripple Voltage vs Output Current

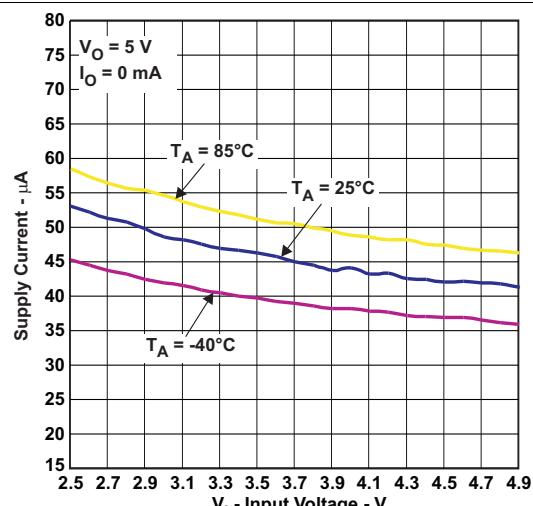


Figure 18. Supply Current vs Input Voltage

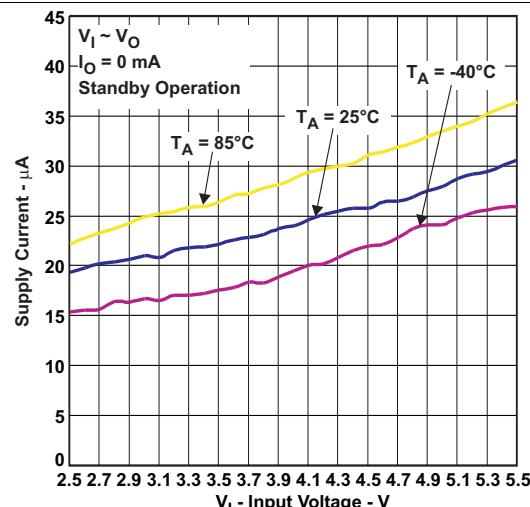


Figure 19. Supply Current vs Input Voltage

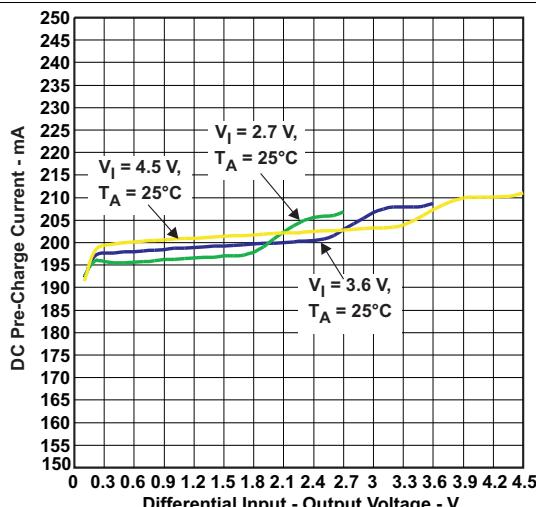


Figure 20. DC Pre-Charge Current vs Differential Input-Output Voltage

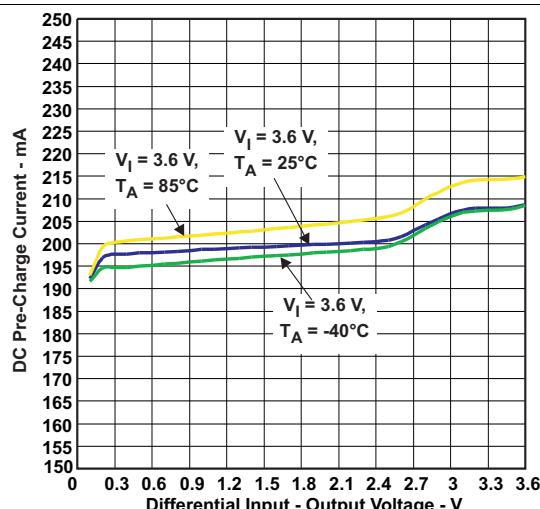


Figure 21. DC Pre-Charge Current vs Differential Input-Output Voltage

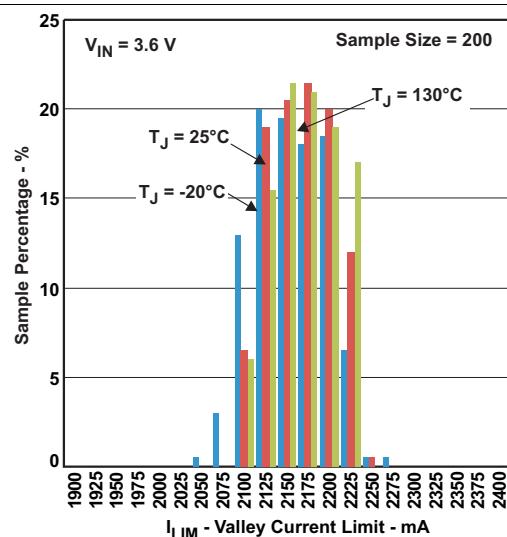


Figure 22. Valley Current Limit

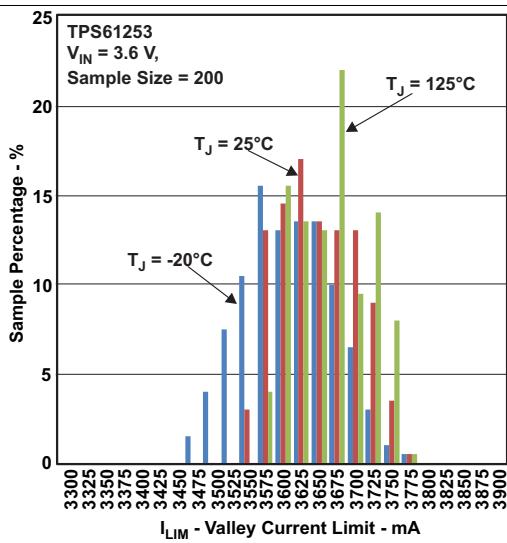


Figure 23. Valley Current Limit

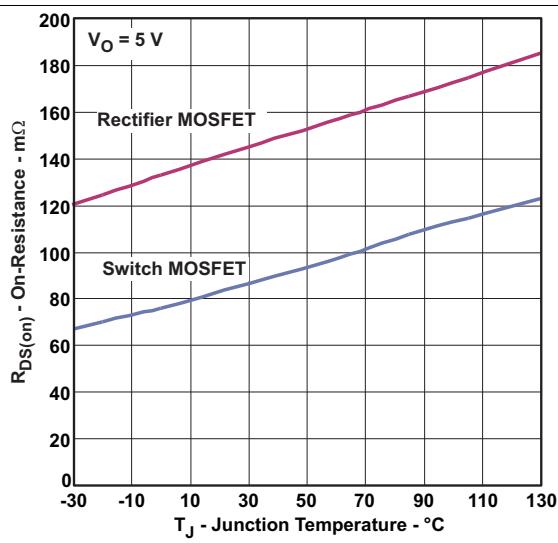
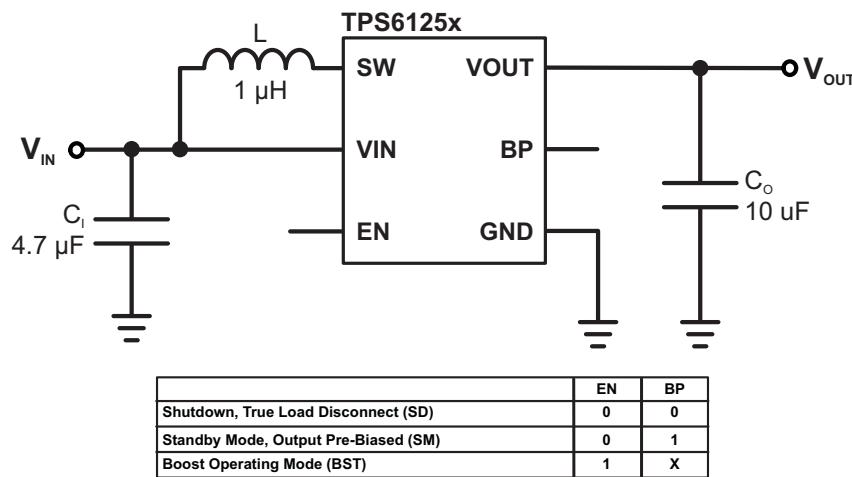


Figure 24. MOSFET  $r_{DS(on)}$  vs Temperature

## 8 Parameter Measurement Information



**Figure 25. Parameter Measurement Schematic**

## 9 Detailed Description

### 9.1 Overview

The TPS6125x synchronous step-up converter typically operates at a quasi-constant 3.5-MHz frequency pulse width modulation (PWM) at moderate to heavy load currents. At light load currents, the TPS6125x converter operates in power-save mode with pulse frequency modulation (PFM).

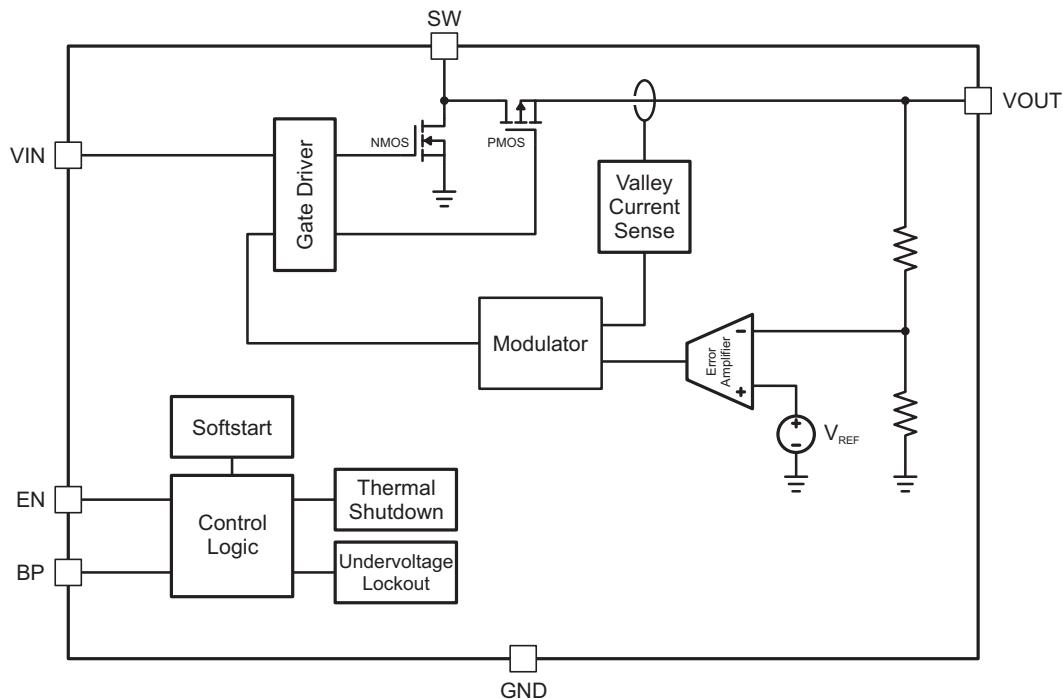
During PWM operation, the converter uses a novel quasi-constant on-time valley current mode control scheme to achieve excellent line/load regulation and allows the use of a small ceramic inductor and capacitors. Based on the  $V_{IN}/V_{OUT}$  ratio, a simple circuit predicts the required on-time.

At the beginning of the switching cycle, the low-side N-MOS switch is turned-on and the inductor current ramps up to a peak current that is defined by the on-time and the inductance. In the second phase, once the on-timer has expired, the rectifier is turned-on and the inductor current decays to a preset valley current threshold. Finally, the switching cycle repeats by setting the on timer again and activating the low-side N-MOS switch.

In general, a dc/dc step-up converter can only operate in "true" boost mode, i.e. the output "boosted" by a certain amount above the input voltage. The TPS6125x device operates differently as it can smoothly transition in and out of zero duty cycle operation. Therefore the output can be kept as close as possible to its regulation limits even though the converter is subject to an input voltage that tends to be excessive. In this operation mode, the output current capability of the regulator is limited to ca. 150mA. Refer to [Figure 11](#) for further details.

The current mode architecture with adaptive slope compensation provides excellent transient load response, requiring minimal output filtering. Internal soft-start and loop compensation simplifies the design process while minimizing the number of external components.

### 9.2 Functional Block Diagram



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## 9.3 Feature Description

### 9.3.1 Current Limit Operation

The TPS6125x device employs a valley current limit sensing scheme. Current limit detection occurs during the off-time by sensing of the voltage drop across the synchronous rectifier.

The output voltage is reduced as the power stage of the device operates in a constant current mode. The maximum continuous output current ( $I_{OUT(CL)}$ ), before entering current limit (CL) operation, can be defined by [Equation 1](#).

$$I_{OUT(CL)} = (1 - D) \cdot (I_{VALLEY} + \frac{1}{2} \Delta I_L) \quad (1)$$

The duty cycle (D) can be estimated by [Equation 2](#)

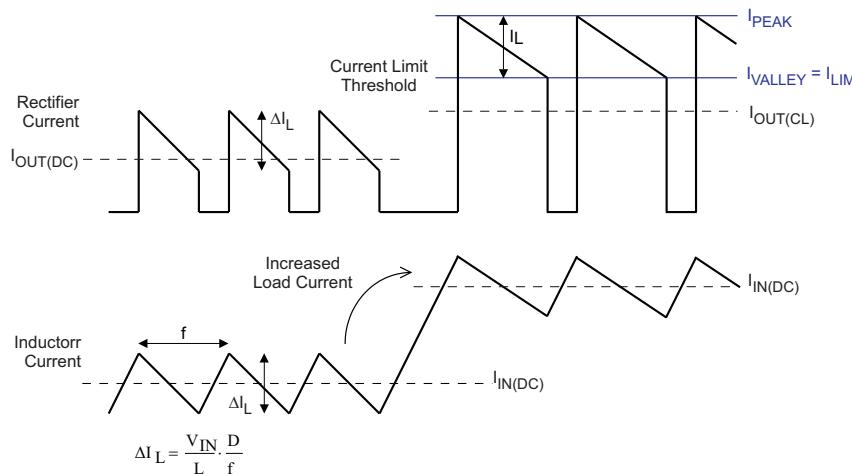
$$D = 1 - \frac{V_{IN} \cdot \eta}{V_{OUT}} \quad (2)$$

and the peak-to-peak current ripple ( $\Delta I_L$ ) is calculated by [Equation 3](#)

$$\Delta I_L = \frac{V_{IN}}{L} \cdot \frac{D}{f} \quad (3)$$

The output current,  $I_{OUT(DC)}$ , is the average of the rectifier ripple current waveform. When the load current is increased such that the lower peak is above the current limit threshold, the off-time is increased to allow the current to decrease to this threshold before the next on-time begins (so called frequency fold-back mechanism). When the current limit is reached the output voltage decreases during further load increase.

[Figure 26](#) illustrates the inductor and rectifier current waveforms during current limit operation.



**Figure 26. Inductor/Rectifier Currents in Current Limit Operation**

### 9.3.2 Enable

The TPS6125x device starts operation when EN is set high and starts up with the soft-start sequence. For proper operation, the EN pin must be terminated and must not be left floating.

Pulling the EN and BP pins low forces the device in shutdown, with a shutdown current of typically 1  $\mu$ A. In this mode, true load disconnect between the battery and load prevents current flow from  $V_{IN}$  to  $V_{OUT}$ , as well as reverse flow from  $V_{OUT}$  to  $V_{IN}$ .

Pulling the EN pin low and the BP pin high forces the device in standby mode, refer to the [Standby Mode](#) section for more details.

## Feature Description (continued)

### 9.3.3 Load Disconnect and Reverse Current Protection

Regular boost converters do not disconnect the load from the input supply and therefore a connected battery will be discharged during shutdown. The advantage of TPS6125x is that this converter disconnects the output from the input of the power supply when it is disabled (so called true shutdown mode). In case of a connected battery it prevents it from being discharged during shutdown of the converter.

### 9.3.4 Softstart

The TPS6125x device has an internal softstart circuit that limits the inrush current during start-up. The first step in the start-up cycle is the pre-charge phase. During pre-charge, the rectifying switch is turned on until the output capacitor is charged to a value close to the input voltage. The rectifying switch is current limited (approximately 200 mA) during this phase. This mechanism is used to limit the output current under short-circuit condition.

Once the output capacitor has been biased to the input voltage, the converter starts switching. The soft-start system progressively increases the on-time as a function of the input-to-output voltage ratio. As soon as the output voltage is reached, the regulation loop takes control and full current operation is permitted.

### 9.3.5 Undervoltage Lockout

The under voltage lockout circuit prevents the device from malfunctioning at low input voltages and the battery from excessive discharge. It disables the output stage of the converter once the falling  $V_{IN}$  trips the under-voltage lockout threshold  $V_{UVLO}$  which is typically 2.0V. The device starts operation once the rising  $V_{IN}$  trips  $V_{UVLO}$  threshold plus its hysteresis of 100 mV at typically 2.1 V.

### 9.3.6 Thermal Regulation

The TPS6125x device contains a thermal regulation loop that monitors the die temperature during the pre-charge phase. If the die temperature rises to high values of about 110 °C, the device automatically reduces the current to prevent the die temperature from increasing further. Once the die temperature drops about 10 °C below the threshold, the device will automatically increase the current to the target value. This function also reduces the current during a short-circuit condition.

### 9.3.7 Thermal Shutdown

As soon as the junction temperature,  $T_J$ , exceeds 140°C (typ.) the device goes into thermal shutdown. In this mode, the high-side and low-side MOSFETs are turned-off. When the junction temperature falls below the thermal shutdown minus its hysteresis, the device continues the operation.

## 9.4 Device Functional Modes

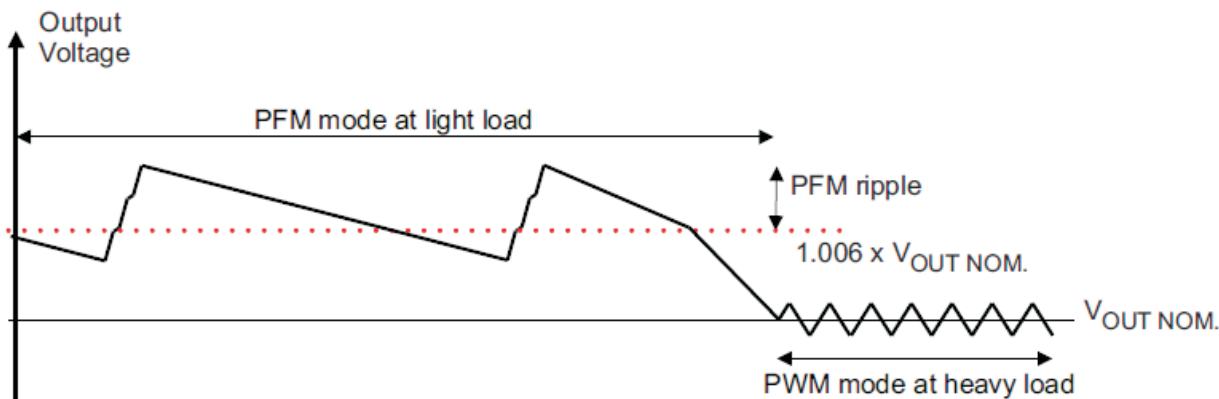
### 9.4.1 Power Save Mode

The TPS6125x integrates a power save mode to improve efficiency at light load. In power save mode the converter only operates when the output voltage trips below a set threshold voltage.

It ramps up the output voltage with several pulses and goes into power save mode once the output voltage exceeds the set threshold voltage.

The PFM mode is left and PWM mode entered in case the output current can not longer be supported in PFM mode.

## Device Functional Modes (continued)



**Figure 27. Power Save**

### 9.4.2 Standby Mode

The TPS6125x device is able to maintain its output biased at the input voltage level. In so called standby mode ( $EN = 0$ ,  $BP = 1$ ), the synchronous rectifier is current limited to ca. 150mA allowing an external load (e.g. audio amplifier) to be powered with a restricted supply. The output voltage is slightly reduced due to voltage drop across the rectifier MOSFET and the inductor DC resistance. The device consumes only a standby current of 21  $\mu$ A (typ).

**Table 2. Operating Mode Control**

OPERATING MODE	EN	BP
Shutdown, True Load Disconnect (SD)	0	0
Standby Mode, Output Pre-Biased (SM)	0	1
Boost Operating Mode (BST)	1	0
	1	1

## 10 Application and Implementation

### NOTE

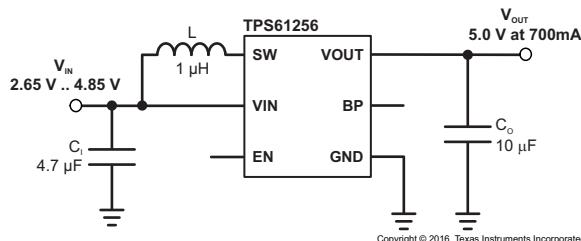
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 10.1 Application Information

With a wide input voltage range of 2.3 V to 5.5 V, the TPS6125x supports applications powered by Li-Ion batteries with extended voltage range. Intended for low-power applications, it supports up to 800-mA load current from a battery discharged as low as 2.65 V and allows the use of low cost chip inductor and capacitors. Different fixed voltage output versions are available from 3.15 V to 5.0 V. The TPS6125x offers a very small solution size due to minimum amount of external components. It allows the use of small inductors and input capacitors to achieve a small solution size. During shutdown, the load is completely disconnected from the battery.

### 10.2 Typical Application

This section details an application with TPS61256 to output fixed 5.0 V.


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**Figure 28. Smallest Solution Size Application**

#### 10.2.1 Design Requirements

In this example, TPS61256 is used to design a 5-V power supply with up to 700-mA output current capability. The TPS61256 can be powered by one-cell Li-ion battery, and in this example the input voltage range is from 2.65 V to 4.85 V.

#### 10.2.2 Detailed Design Procedure

**Table 3. List of Components**

REFERENCE	DESCRIPTION	PART NUMBER, MANUFACTURER <sup>(1)</sup>
L <sup>(2)</sup>	1.0 μH, 1.8 A, 48 mΩ, 3.2 x 2.5 x 1.0mm max. height	LQM32PN1R0MG0, muRata
L <sup>(3)</sup>	1.0 μH, 3.7 A, 37 mΩ, 3.2 x 2.5 x 1.2mm max. height	DFE322512C, TOKO
C <sub>I</sub>	4.7 μF, 6.3 V, 0402, X5R ceramic	GRM155R60J475M, muRata
C <sub>O</sub>	10 μF, 6.3 V, 0603, X5R ceramic	GRM188R60J106ME84, muRata

(1) See [Third-Party Products Disclaimer](#)

(2) Inductor used to characterize TPS61254YFF, TPS61255YFF, TPS61256YFF and TPS61257YFF devices.

(3) Inductor used to characterize TPS61253YFF, TPS61258YFF and TPS61259YFF devices.

##### 10.2.2.1 Inductor Selection

A boost converter normally requires two main passive components for storing energy during the conversion, an inductor and an output capacitor. It is advisable to select an inductor with a saturation current rating higher than the possible peak current flowing through the power switches.

The inductor peak current varies as a function of the load, the input and output voltages and can be estimated using [Equation 4](#).

$$I_{L(\text{PEAK})} = \frac{V_{\text{IN}} \cdot D}{2 \cdot f \cdot L} + \frac{I_{\text{OUT}}}{(1-D) \cdot \eta} \quad \text{with} \quad D = 1 - \frac{V_{\text{IN}} \cdot \eta}{V_{\text{OUT}}} \quad (4)$$

Selecting an inductor with insufficient saturation performance can lead to excessive peak current in the converter. This could eventually harm the device and reduce its reliability.

When selecting the inductor, as well as the inductance, parameters of importance are: maximum current rating, series resistance, and operating temperature. The inductor DC current rating should be greater (by some margin) than the maximum input average current, refer to [Equation 5](#) and [Current Limit Operation](#) section for more details.

$$I_{L(\text{DC})} = \frac{V_{\text{OUT}}}{V_{\text{IN}}} \cdot \frac{1}{\eta} \cdot I_{\text{OUT}} \quad (5)$$

The TPS6125x series of step-up converters have been optimized to operate with an effective inductance in the range of 0.7  $\mu\text{H}$  to 2.9  $\mu\text{H}$  and with output capacitors in the range of 10  $\mu\text{F}$  to 47  $\mu\text{F}$ . The internal compensation is optimized for an output filter of  $L = 1 \mu\text{H}$  and  $C_O = 10 \mu\text{F}$ . Larger or smaller inductor values can be used to optimize the performance of the device for specific operating conditions. For more details, see the [Checking Loop Stability](#) section.

In high-frequency converter applications, the efficiency is essentially affected by the inductor AC resistance (i.e. quality factor) and to a smaller extent by the inductor DCR value. To achieve high efficiency operation, care should be taken in selecting inductors featuring a quality factor above 25 at the switching frequency. Increasing the inductor value produces lower RMS currents, but degrades transient response. For a given physical inductor size, increased inductance usually results in an inductor with lower saturation current.

The total losses of the coil consist of both the losses in the DC resistance,  $R_{(\text{DC})}$ , and the following frequency-dependent components:

- The losses in the core material (magnetic hysteresis loss, especially at high switching frequencies)
- Additional losses in the conductor from the skin effect (current displacement at high frequencies)
- Magnetic field losses of the neighboring windings (proximity effect)
- Radiation losses

The following inductor series from different suppliers have been used with the TPS6125x converters.

**Table 4. List of Inductors**

MANUFACTURER <sup>(1)</sup>	SERIES	DIMENSIONS (in mm)
HITACHI METALS	KSLI-322512BL1-1R0	3.2 x 2.5 x 1.2 max. height
	LQM32PN1R0MG0	3.2 x 2.5 x 1.0 max. height
	LQM2HPN1R0MG0	2.5 x 2.0 x 1.0 max. height
	LQM21PN1R5MC0	2.0 x 1.2 x 0.55 max height
TOKO	DFE322512C-1R0	3.2 x 2.5 x 1.2 max. height
	MDT2012-CLR1R0AM	2.0 x 1.2 x 0.58 max height

(1) See [Third-Party Products Disclaimer](#)

### 10.2.2.2 Output Capacitor

For the output capacitor, it is recommended to use small ceramic capacitors placed as close as possible to the V<sub>OUT</sub> and GND pins of the IC. If, for any reason, the application requires the use of large capacitors which can not be placed close to the IC, using a smaller ceramic capacitor in parallel to the large one is highly recommended. This small capacitor should be placed as close as possible to the V<sub>OUT</sub> and GND pins of the IC. To get an estimate of the recommended minimum output capacitance, [Equation 6](#) can be used.

$$C_{\text{MIN}} = \frac{I_{\text{OUT}} \cdot (V_{\text{OUT}} - V_{\text{IN}})}{f \cdot \Delta V \cdot V_{\text{OUT}}} \quad (6)$$

Where f is the switching frequency which is 3.5 MHz (typ.) and  $\Delta V$  is the maximum allowed output ripple.

With a chosen ripple voltage of 20mV, a minimum effective capacitance of  $9\mu F$  is needed. The total ripple is larger due to the ESR of the output capacitor. This additional component of the ripple can be calculated using [Equation 7](#)

$$V_{ESR} = I_{OUT} \cdot R_{ESR} \quad (7)$$

An MLCC capacitor with twice the value of the calculated minimum should be used due to DC bias effects. This is required to maintain control loop stability. The output capacitor requires either an X7R or X5R dielectric. Y5V and Z5U dielectric capacitors, aside from their wide variation in capacitance over temperature, become resistive at high frequencies. There are no additional requirements regarding minimum ESR. Larger capacitors cause lower output voltage ripple as well as lower output voltage drop during load transients but the total output capacitance value should not exceed ca.  $50\mu F$ .

**DC bias effect:** high cap. ceramic capacitors exhibit DC bias effects, which have a strong influence on the device's effective capacitance. Therefore the right capacitor value has to be chosen very carefully. Package size and voltage rating in combination with material are responsible for differences between the rated capacitor value and its effective capacitance. For instance, a  $10\mu F$  X5R 6.3-V 0603 MLCC capacitor would typically show an effective capacitance of less than  $4\mu F$  (under 5 V bias condition, high temperature).

In applications featuring high pulsed load currents (e.g. TPS61253 based solution) it is recommended to run the converter with a reasonable amount of effective output capacitance, for instance x2  $10\mu F$  X5R 6.3-V 0603 MLCC capacitors connected in parallel.

#### 10.2.2.3 Input Capacitor

Multilayer ceramic capacitors are an excellent choice for input decoupling of the step-up converter as they have extremely low ESR and are available in small footprints. Input capacitors should be located as close as possible to the device. While a  $4.7\mu F$  input capacitor is sufficient for most applications, larger values may be used to reduce input current ripple without limitations.

Take care when using only ceramic input capacitors. When a ceramic capacitor is used at the input and the power is being supplied through long wires, such as from a wall adapter, a load step at the output can induce ringing at the VIN pin. This ringing can couple to the output and be mistaken as loop instability or could even damage the part. Additional "bulk" capacitance (electrolytic or tantalum) should in this circumstance be placed between  $C_I$  and the power source lead to reduce ringing that can occur between the inductance of the power source leads and  $C_I$ .

#### 10.2.2.4 Checking Loop Stability

The first step of circuit and stability evaluation is to look from a steady-state perspective at the following signals:

- Switching node, SW
- Inductor current,  $I_L$
- Output ripple voltage,  $V_{OUT(AC)}$

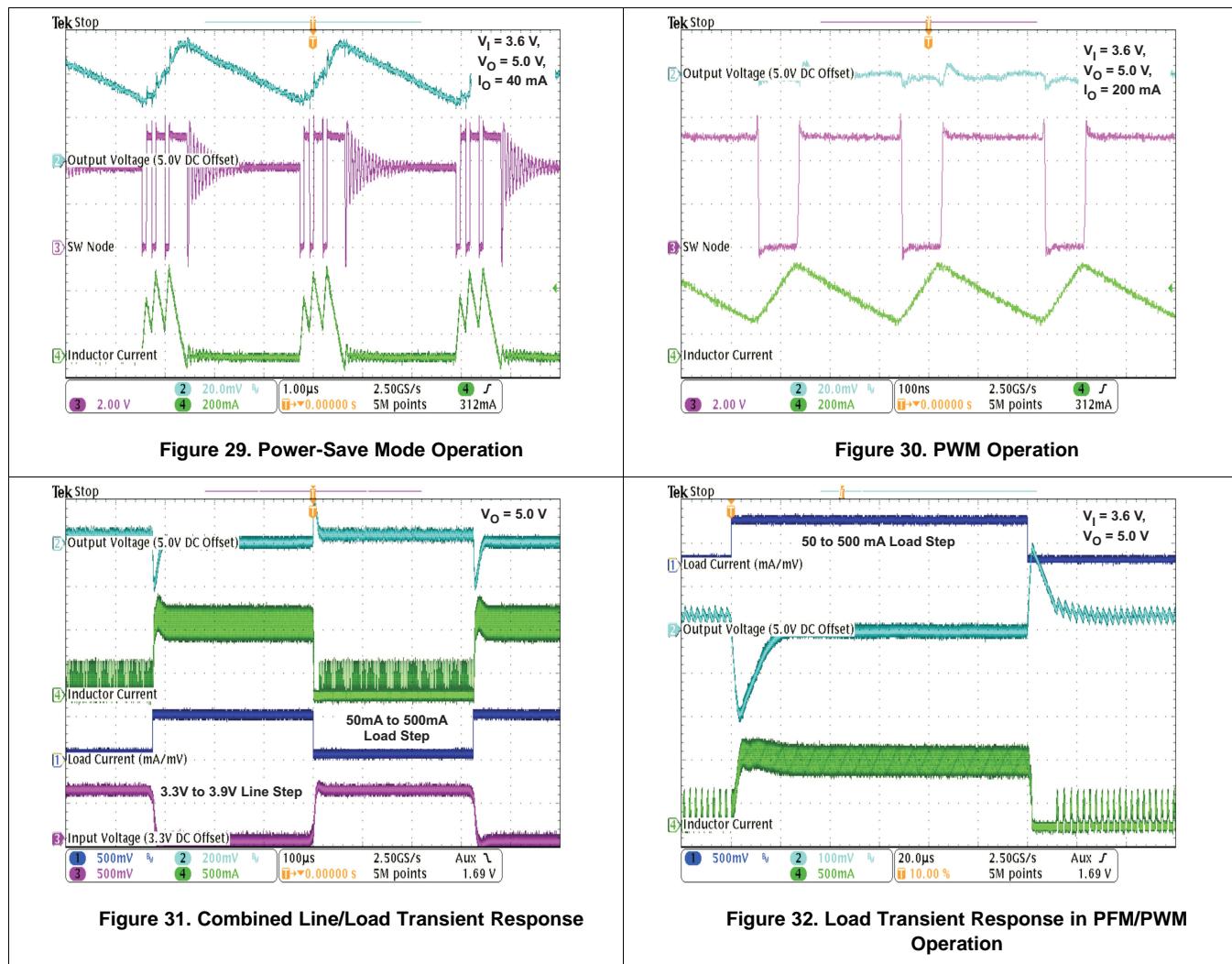
These are the basic signals that need to be measured when evaluating a switching converter. When the switching waveform shows large duty cycle jitter or the output voltage or inductor current shows oscillations, the regulation loop may be unstable. This is often a result of board layout and/or L-C combination.

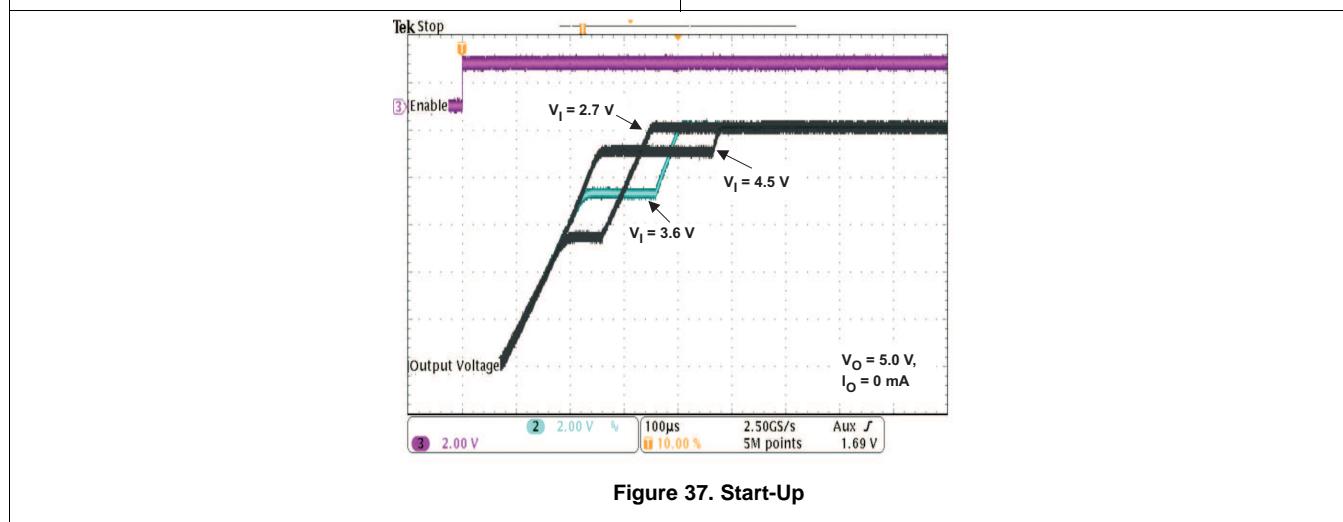
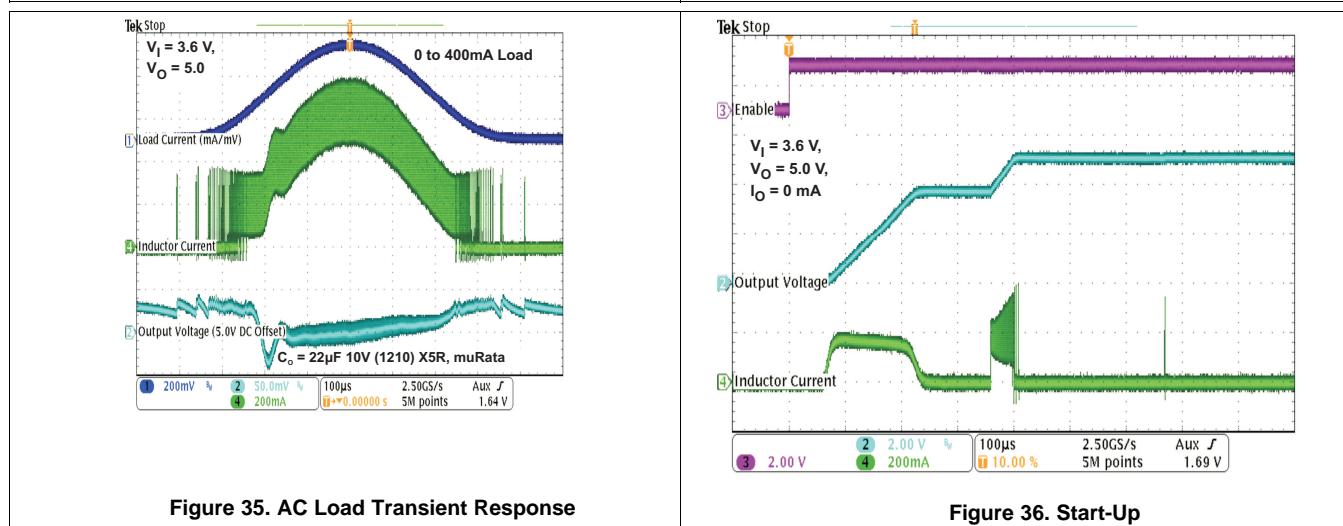
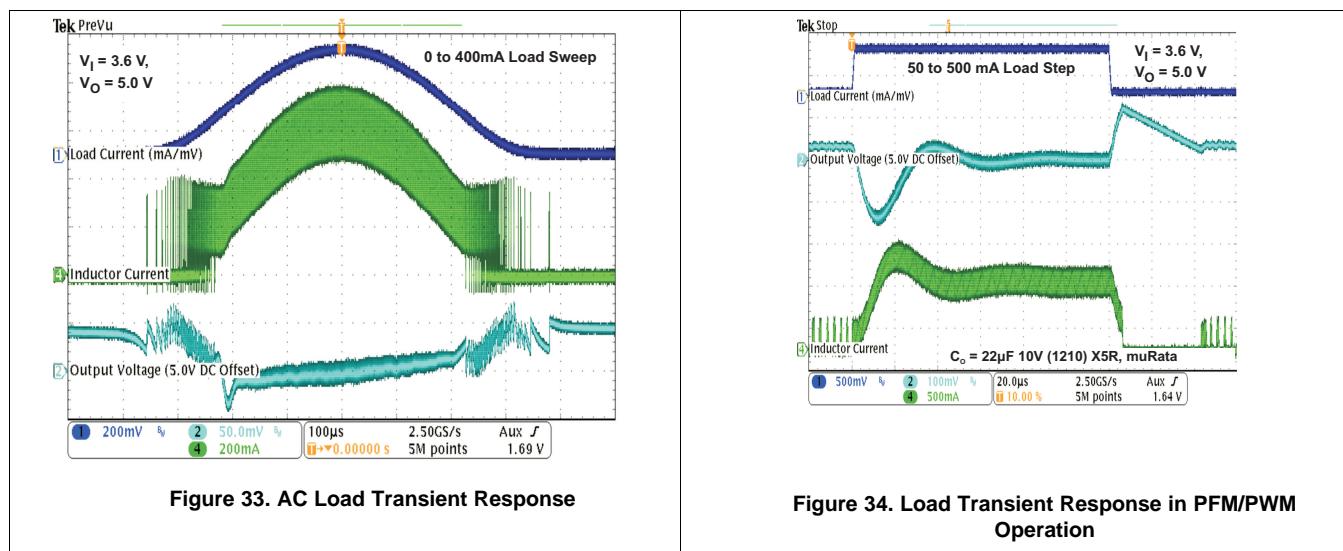
As a next step in the evaluation of the regulation loop, the load transient response is tested. The time between the application of the load transient and the turn on of the P-channel MOSFET, the output capacitor must supply all of the current required by the load.  $V_{OUT}$  immediately shifts by an amount equal to  $\Delta I_{(LOAD)} \times ESR$ , where ESR is the effective series resistance of  $C_{OUT}$ .  $\Delta I_{(LOAD)}$  begins to charge or discharge  $C_{OUT}$  generating a feedback error signal used by the regulator to return  $V_{OUT}$  to its steady-state value. The results are most easily interpreted when the device operates in PWM mode.

During this recovery time,  $V_{OUT}$  can be monitored for settling time, overshoot or ringing that helps judge the converter's stability. Without any ringing, the loop has usually more than  $45^\circ$  of phase margin. Because the damping factor of the circuitry is directly related to several resistive parameters (e.g., MOSFET  $r_{DS(on)}$ ) that are temperature dependant, the loop stability analysis has to be done over the input voltage range, load current range, and temperature range.

### 10.2.3 Application Curves

	<b>FIGURE</b>
PFM operation	Figure 29
PWM operation	Figure 30
Combined line/load transient response	Figure 31
Load transient response	Figure 32, Figure 34
AC load transient response	Figure 33, Figure 35
Start-up	Figure 36, Figure 37





## 10.3 System Examples

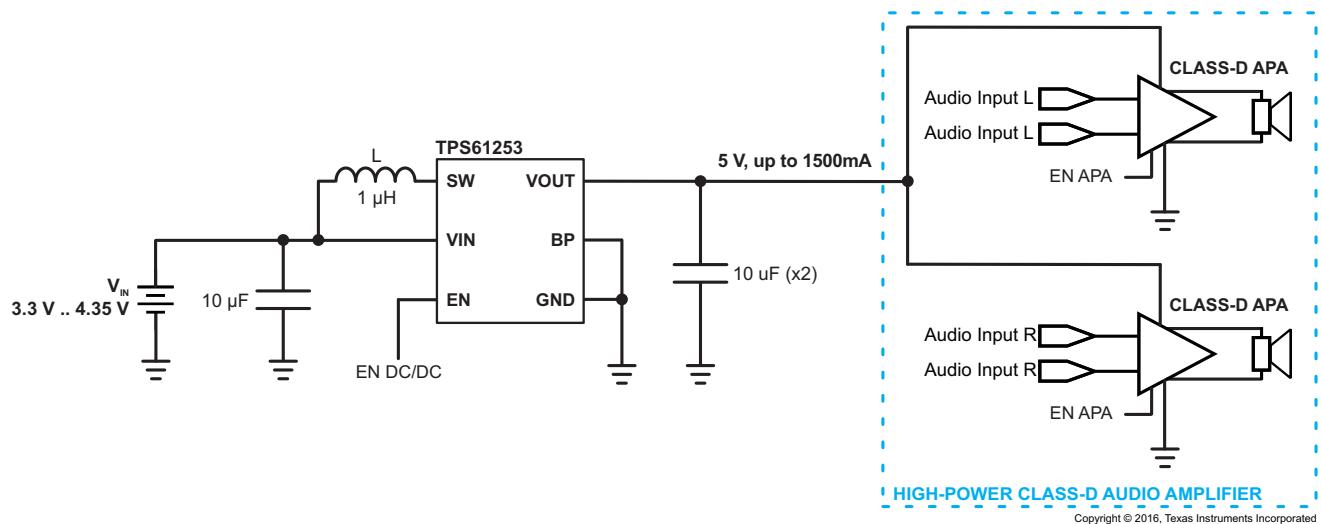


Figure 38. "Boosted" Stereo Audio Power Supply

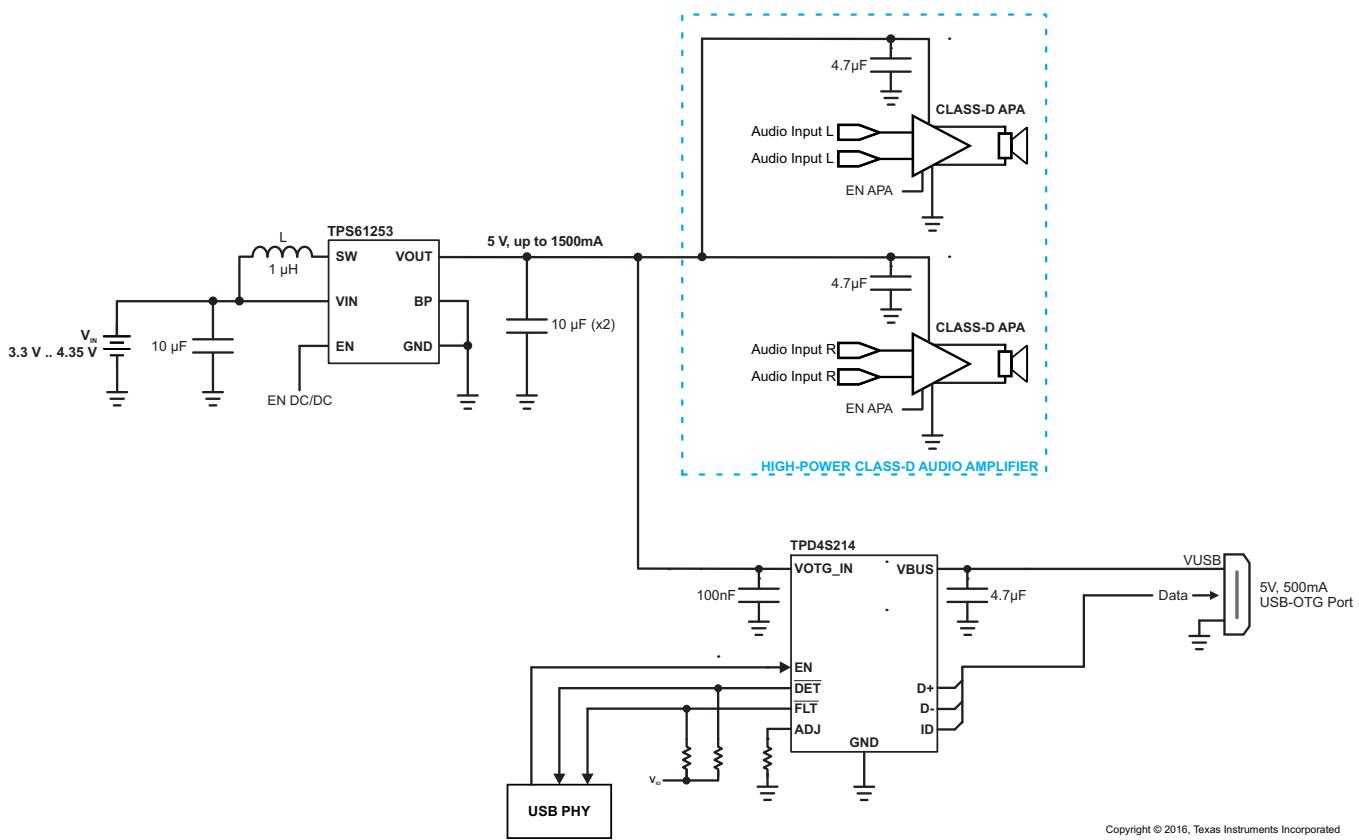
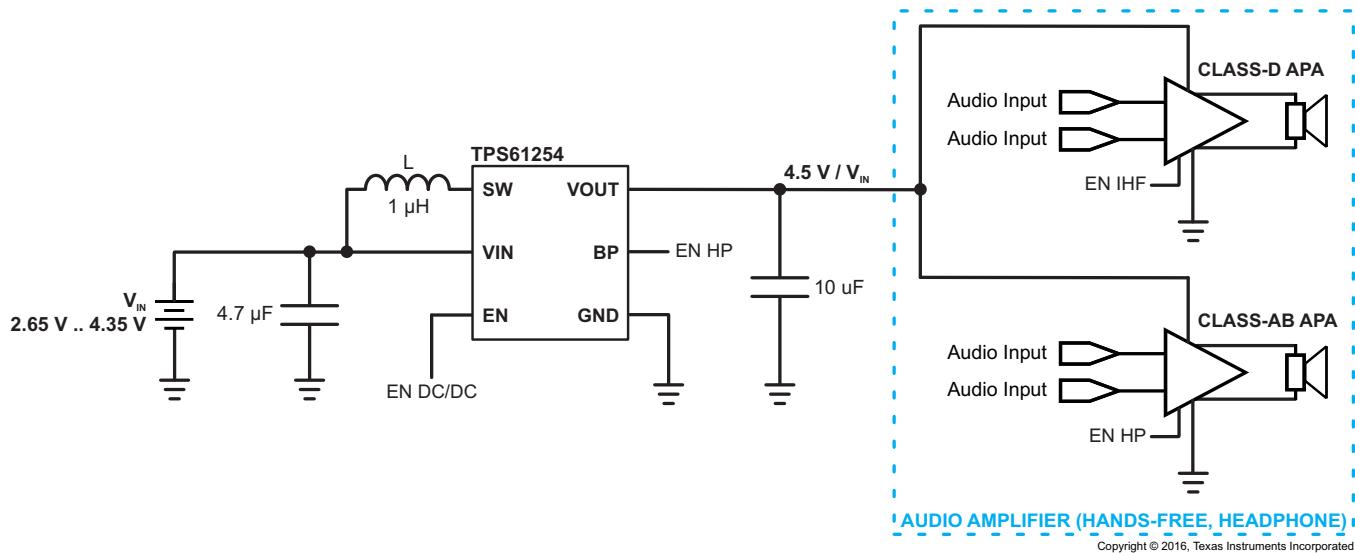
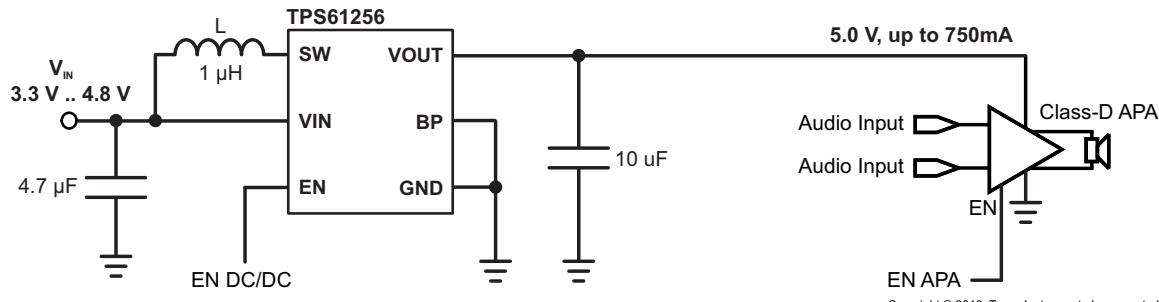


Figure 39. Single Cell Li-Ion Power Solution for Tablet PCs Featuring "Boosted" Audio Power Supply and USB-OTG I/F

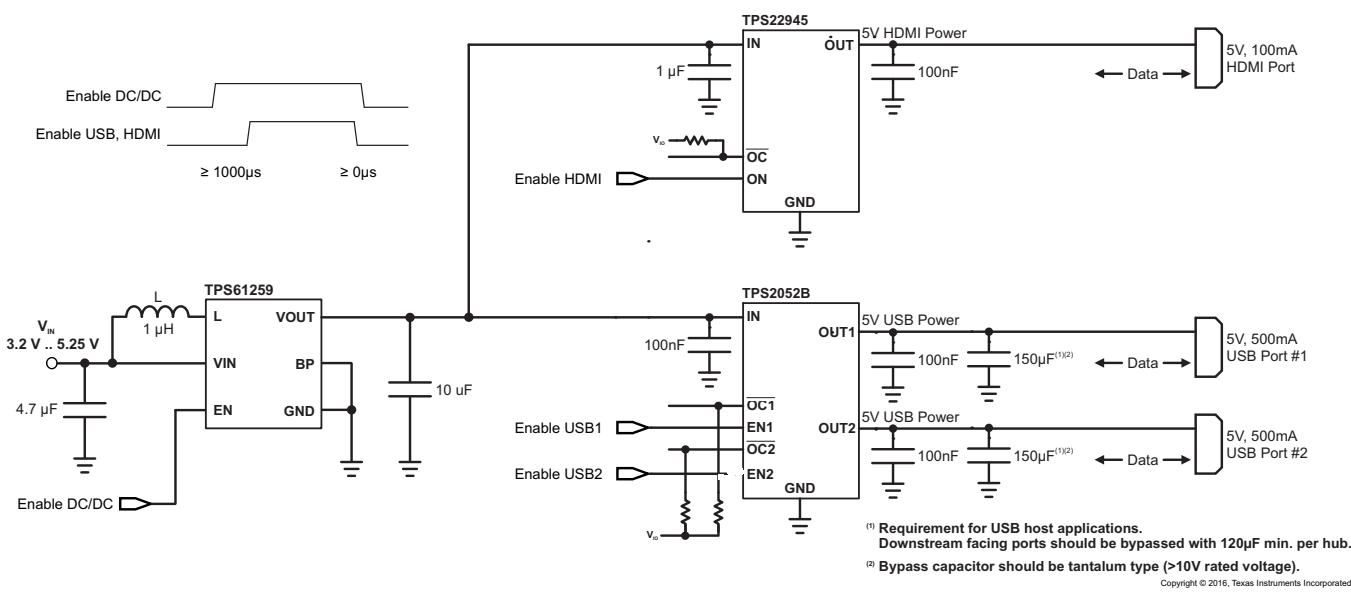
## System Examples (continued)



**Figure 40. Combined Audio Amplifier Power Supply**



**Figure 41. "Boosted" Audio Power Supply**



**Figure 42. Single Cell Li-Ion Power Solution for Tablet PCs Featuring x2 USB Host Ports, HDMI I/F**

## 11 Power Supply Recommendations

The power supply can be three-cell alkaline, NiCd or NiMH, or one-cell Li-Ion or Li-Polymer battery. The input supply should be well regulated with the rating of TPS6125x. If the input supply is located more than a few inches from the device, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. An electrolytic or tantalum capacitor with a value of 47  $\mu$ F is a typical choice.

## 12 Layout

### 12.1 Layout Guidelines

For all switching power supplies, the layout is an important step in the design, especially at high peak currents and high switching frequencies. If the layout is not carefully done, the regulator could show stability problems as well as EMI problems. Therefore, use wide and short traces for the main current path and for the power ground tracks. The input capacitor, output capacitor, and the inductor should be placed as close as possible to the IC. Use a common ground node for power ground and a different one for control ground to minimize the effects of ground noise. Connect these ground nodes at any place close to the ground pins of the IC.

### 12.2 Layout Example

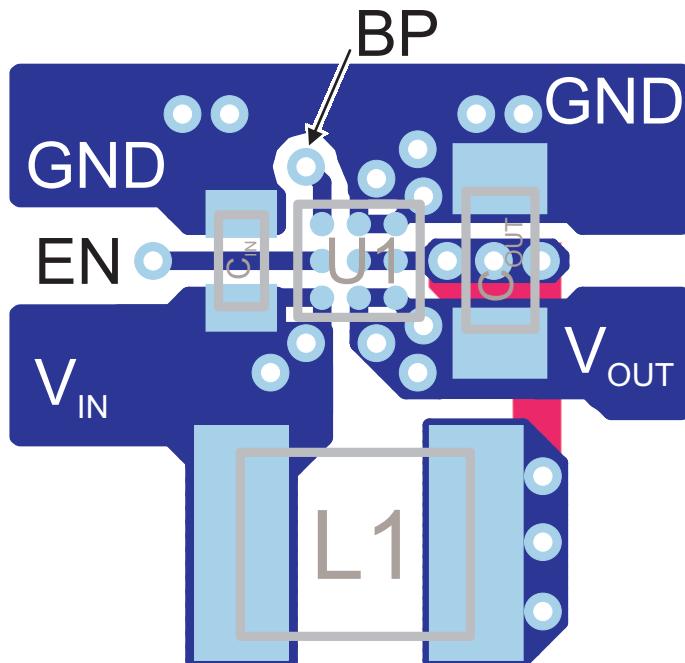


Figure 43. Suggested Layout (Top)

## 12.3 Thermal Considerations

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependent issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power-dissipation limits of a given component.

Three basic approaches for enhancing thermal performance are listed below:

- Improving the power dissipation capability of the PCB design
- Improving the thermal coupling of the component to the PCB
- Introducing airflow in the system

As power demand in portable designs is more and more important, designers must figure the best trade-off between efficiency, power dissipation and solution size. Due to integration and miniaturization, junction temperature can increase significantly which could lead to bad application behaviors (i.e. premature thermal shutdown or worst case reduce device reliability).

Junction-to-ambient thermal resistance is highly application and board-layout dependent. In applications where high maximum power dissipation exists (e.g. TPS61253 or TPS61259 based solutions), special care must be paid to thermal dissipation issues in board design. The device operating junction temperature ( $T_J$ ) should be kept below 125°C.

## 13 Device and Documentation Support

### 13.1 Device Support

#### 13.1.1 Third-Party Products Disclaimer

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### 13.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**Table 5. Related Links**

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TPS61253	<a href="#">Click here</a>				
TPS61254	<a href="#">Click here</a>				
TPS61256	<a href="#">Click here</a>				
TPS61258	<a href="#">Click here</a>				
TPS61259	<a href="#">Click here</a>				
TPS612592	<a href="#">Click here</a>				

### 13.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates — go to the product folder for your device on ti.com. In the upper right-hand corner, click the *Alert me* button to register and receive a weekly digest of product information that has changed (if any). For change details, check the revision history of any revised document.

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**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 13.5 Trademarks

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### 13.6 Electrostatic Discharge Caution

 These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 13.7 Glossary

[SLYZ022 — TI Glossary](#).

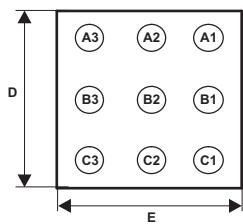
This glossary lists and explains terms, acronyms, and definitions.

## 14 Mechanical, Packaging, and Orderable Information

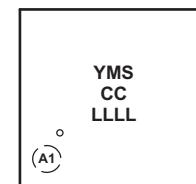
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

### 14.1 Package Summary

**Chip Scale Package  
(Bottom View)**



**Chip Scale Package  
(Top View)**



Code:

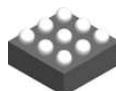
- YM - 2 digit date code
- S - assembly site code
- CC - chip code (see ordering table)
- LLLL - lot trace code

#### 14.1.1 Package Dimensions

The dimensions for the YFF-9 package are shown in [Table 6](#). See the package drawing at the end of this data sheet.

**Table 6. YFF-9 Package Dimensions**

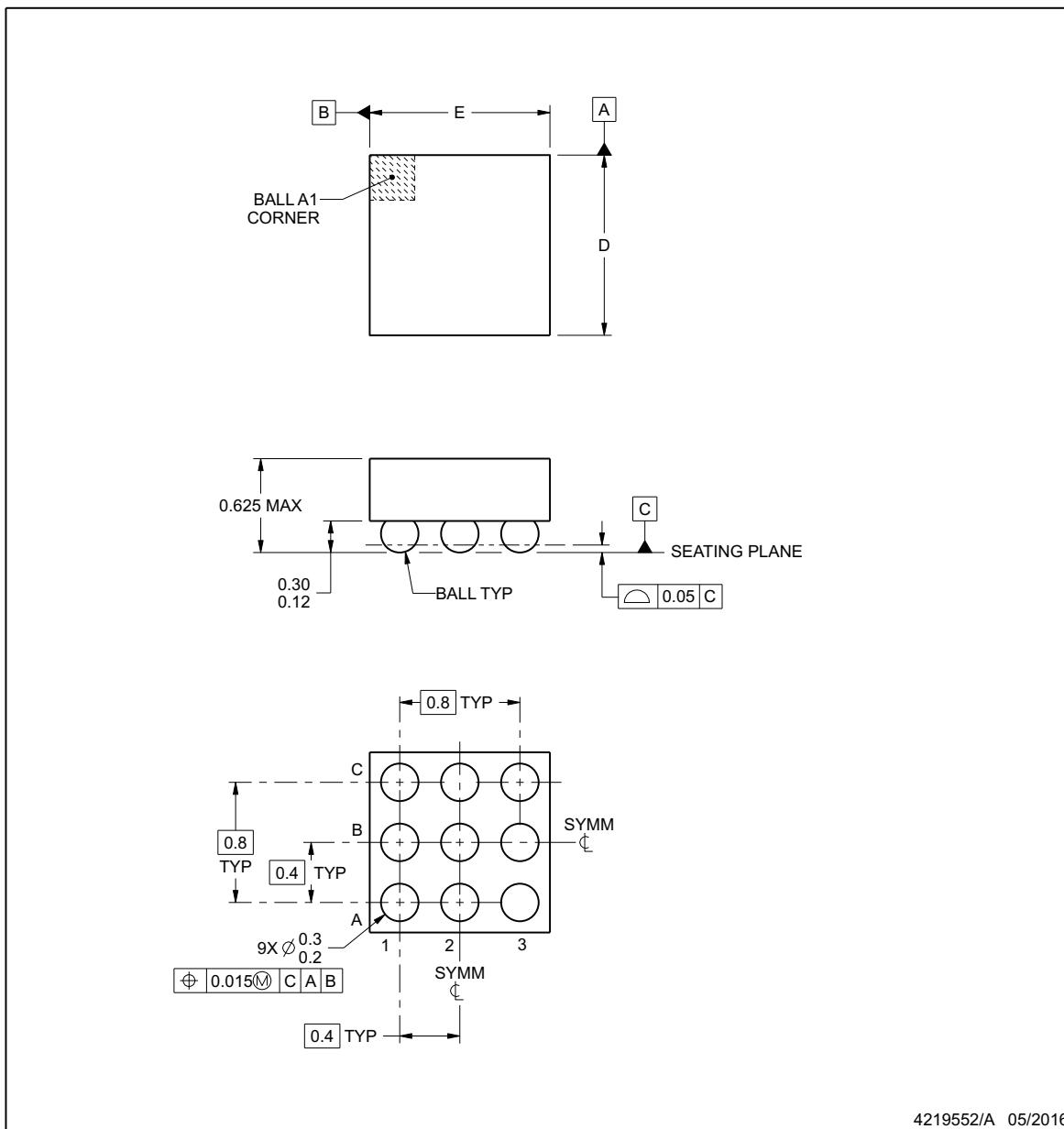
PACKAGED DEVICES	D	E
TPS6125xYFF	max = 1.236mm; min = 1.176 mm	max = 1.336 mm, min = 1.276 mm



## PACKAGE OUTLINE

**YFF0009**
**DSBGA - 0.625 mm max height**

DIE SIZE BALL GRID ARRAY



4219552/A 05/2016

**NOTES:**

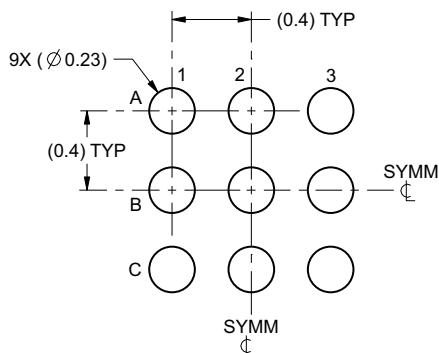
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

## EXAMPLE BOARD LAYOUT

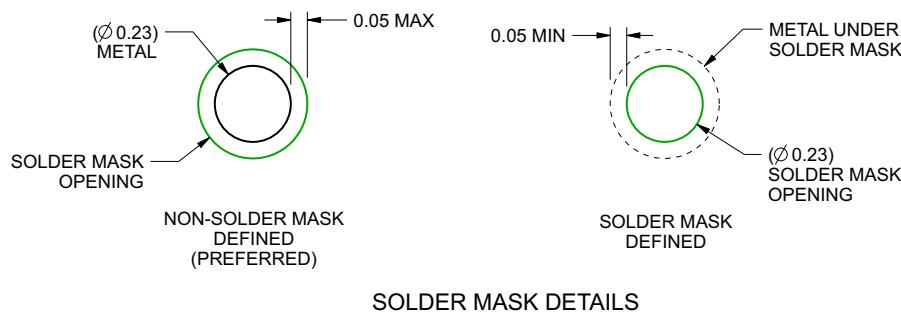
**YFF0009**

**DSBGA - 0.625 mm max height**

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE  
SCALE:30X



SOLDER MASK DETAILS  
NOT TO SCALE

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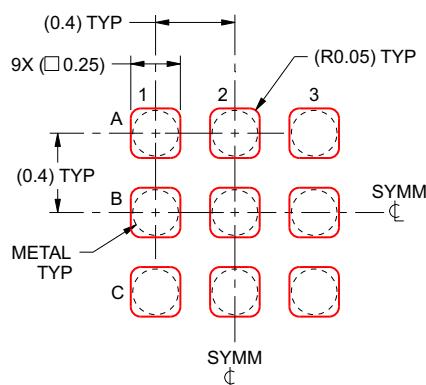
NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 ([www.ti.com/lit/snva009](http://www.ti.com/lit/snva009)).

## EXAMPLE STENCIL DESIGN

**YFF0009**
**DSBGA - 0.625 mm max height**

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE  
BASED ON 0.1 mm THICK STENCIL  
SCALE:30X

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS61253YFFR	ACTIVE	DSBGA	YFF	9	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	SBF	<span style="background-color: red; color: white;">Samples</span>
TPS61253YFFT	ACTIVE	DSBGA	YFF	9	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	SBF	<span style="background-color: red; color: white;">Samples</span>
TPS61254YFFR	ACTIVE	DSBGA	YFF	9	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	QWR	<span style="background-color: red; color: white;">Samples</span>
TPS61254YFFT	ACTIVE	DSBGA	YFF	9	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	QWR	<span style="background-color: red; color: white;">Samples</span>
TPS61256YFFR	ACTIVE	DSBGA	YFF	9	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	RAV	<span style="background-color: red; color: white;">Samples</span>
TPS61256YFFT	ACTIVE	DSBGA	YFF	9	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	RAV	<span style="background-color: red; color: white;">Samples</span>
TPS61258YFFR	ACTIVE	DSBGA	YFF	9	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	SAZ	<span style="background-color: red; color: white;">Samples</span>
TPS61258YFFT	ACTIVE	DSBGA	YFF	9	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	SAZ	<span style="background-color: red; color: white;">Samples</span>
TPS612592YFFR	ACTIVE	DSBGA	YFF	9	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	14A	<span style="background-color: red; color: white;">Samples</span>
TPS612592YFFT	ACTIVE	DSBGA	YFF	9	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	14A	<span style="background-color: red; color: white;">Samples</span>
TPS61259YFFR	ACTIVE	DSBGA	YFF	9	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	SAY	<span style="background-color: red; color: white;">Samples</span>
TPS61259YFFT	ACTIVE	DSBGA	YFF	9	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	SAY	<span style="background-color: red; color: white;">Samples</span>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

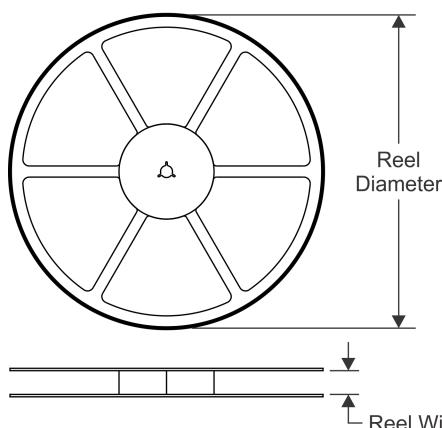
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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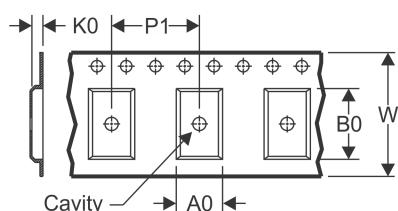
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## TAPE AND REEL INFORMATION

### REEL DIMENSIONS

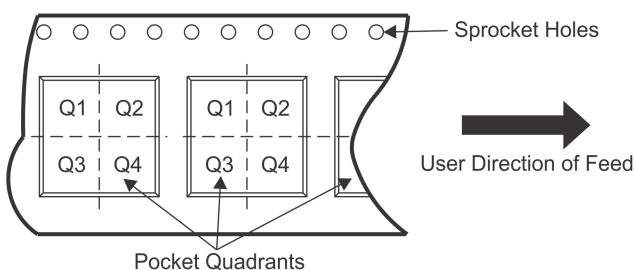


### TAPE DIMENSIONS



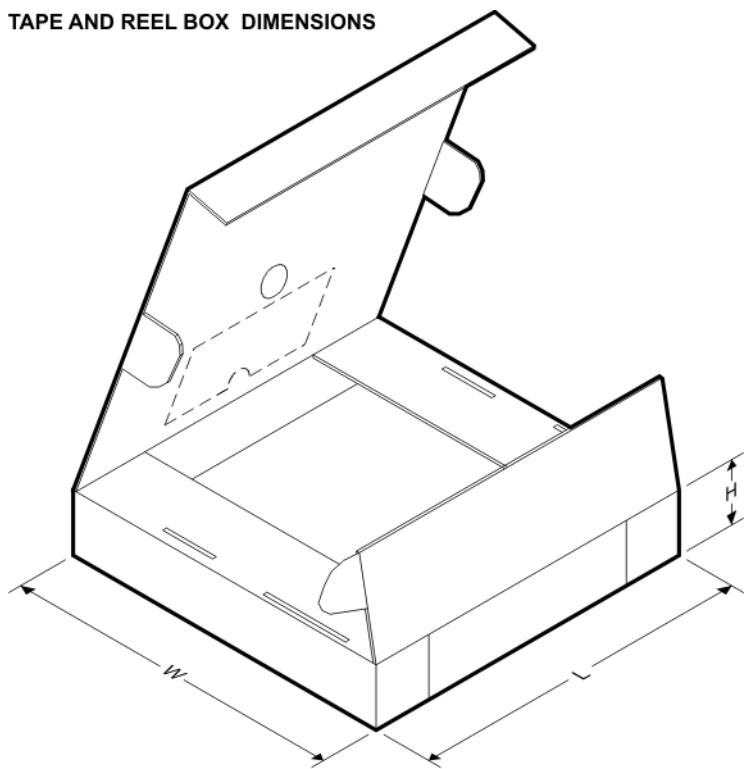
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS61253YFFR	DSBGA	YFF	9	3000	180.0	8.4	1.41	1.31	0.69	2.0	8.0	Q1
TPS61253YFFT	DSBGA	YFF	9	250	180.0	8.4	1.41	1.31	0.69	2.0	8.0	Q1
TPS61254YFFR	DSBGA	YFF	9	3000	180.0	8.4	1.41	1.31	0.69	2.0	8.0	Q1
TPS61254YFFT	DSBGA	YFF	9	250	180.0	8.4	1.41	1.31	0.69	2.0	8.0	Q1
TPS61256YFFR	DSBGA	YFF	9	3000	180.0	8.4	1.41	1.31	0.69	2.0	8.0	Q1
TPS61256YFFT	DSBGA	YFF	9	250	180.0	8.4	1.41	1.31	0.69	2.0	8.0	Q1
TPS61258YFFR	DSBGA	YFF	9	3000	180.0	8.4	1.41	1.31	0.69	2.0	8.0	Q1
TPS61258YFFT	DSBGA	YFF	9	250	180.0	8.4	1.41	1.31	0.69	2.0	8.0	Q1
TPS612592YFFR	DSBGA	YFF	9	3000	180.0	8.4	1.41	1.31	0.69	2.0	8.0	Q1
TPS61259YFFR	DSBGA	YFF	9	3000	180.0	8.4	1.41	1.31	0.69	2.0	8.0	Q1
TPS61259YFFT	DSBGA	YFF	9	250	180.0	8.4	1.41	1.31	0.69	2.0	8.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS61253YFFR	DSBGA	YFF	9	3000	182.0	182.0	20.0
TPS61253YFFT	DSBGA	YFF	9	250	182.0	182.0	20.0
TPS61254YFFR	DSBGA	YFF	9	3000	182.0	182.0	20.0
TPS61254YFFT	DSBGA	YFF	9	250	182.0	182.0	20.0
TPS61256YFFR	DSBGA	YFF	9	3000	182.0	182.0	20.0
TPS61256YFFT	DSBGA	YFF	9	250	182.0	182.0	20.0
TPS61258YFFR	DSBGA	YFF	9	3000	182.0	182.0	20.0
TPS61258YFFT	DSBGA	YFF	9	250	182.0	182.0	20.0
TPS612592YFFR	DSBGA	YFF	9	3000	182.0	182.0	20.0
TPS612592YFFT	DSBGA	YFF	9	250	182.0	182.0	20.0
TPS61259YFFR	DSBGA	YFF	9	3000	182.0	182.0	20.0
TPS61259YFFT	DSBGA	YFF	9	250	182.0	182.0	20.0

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