



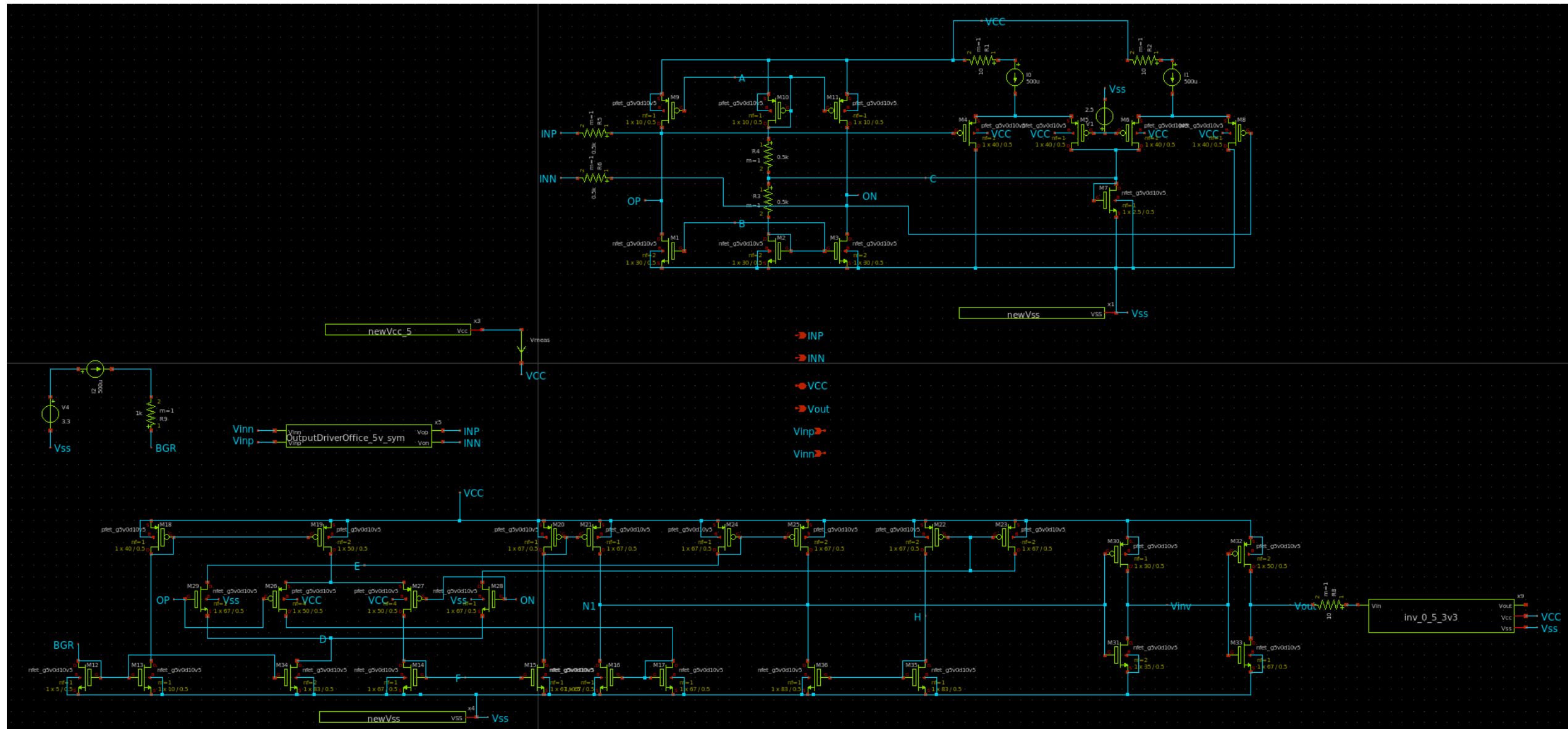
LVDS (Tx/Rx) Design With 5V Devices in Sky130nm Process

November 2023
Revision 0.1

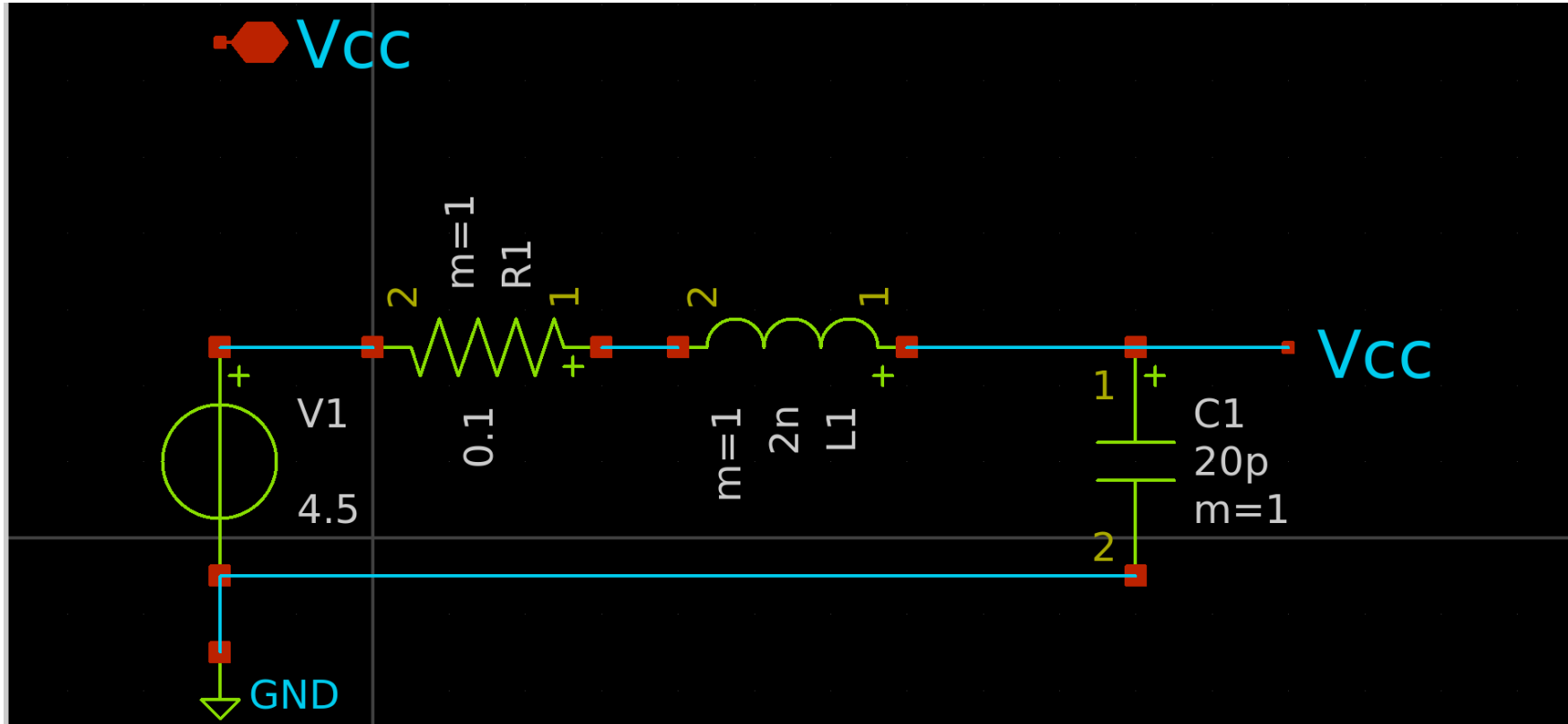
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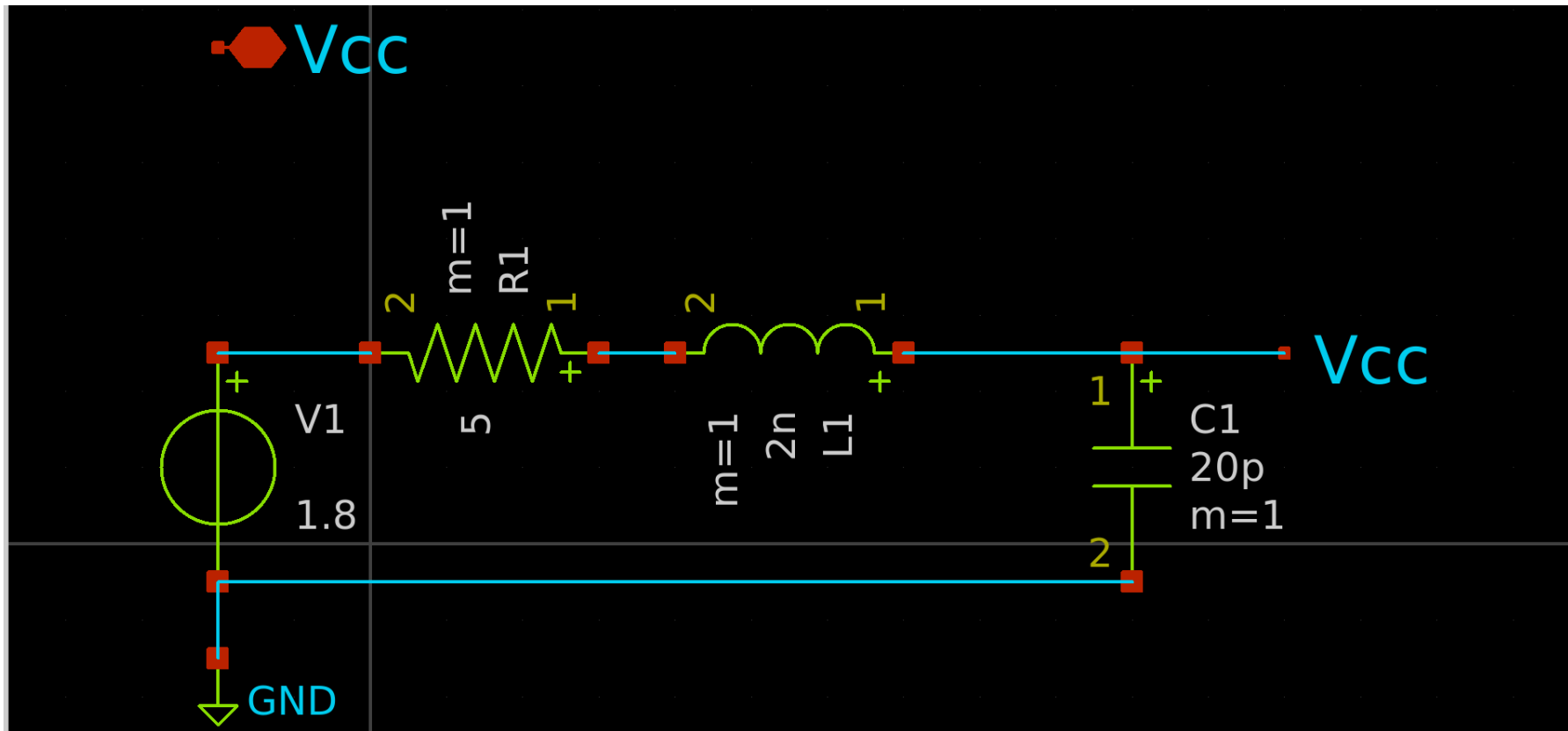
Transceiver Top Level



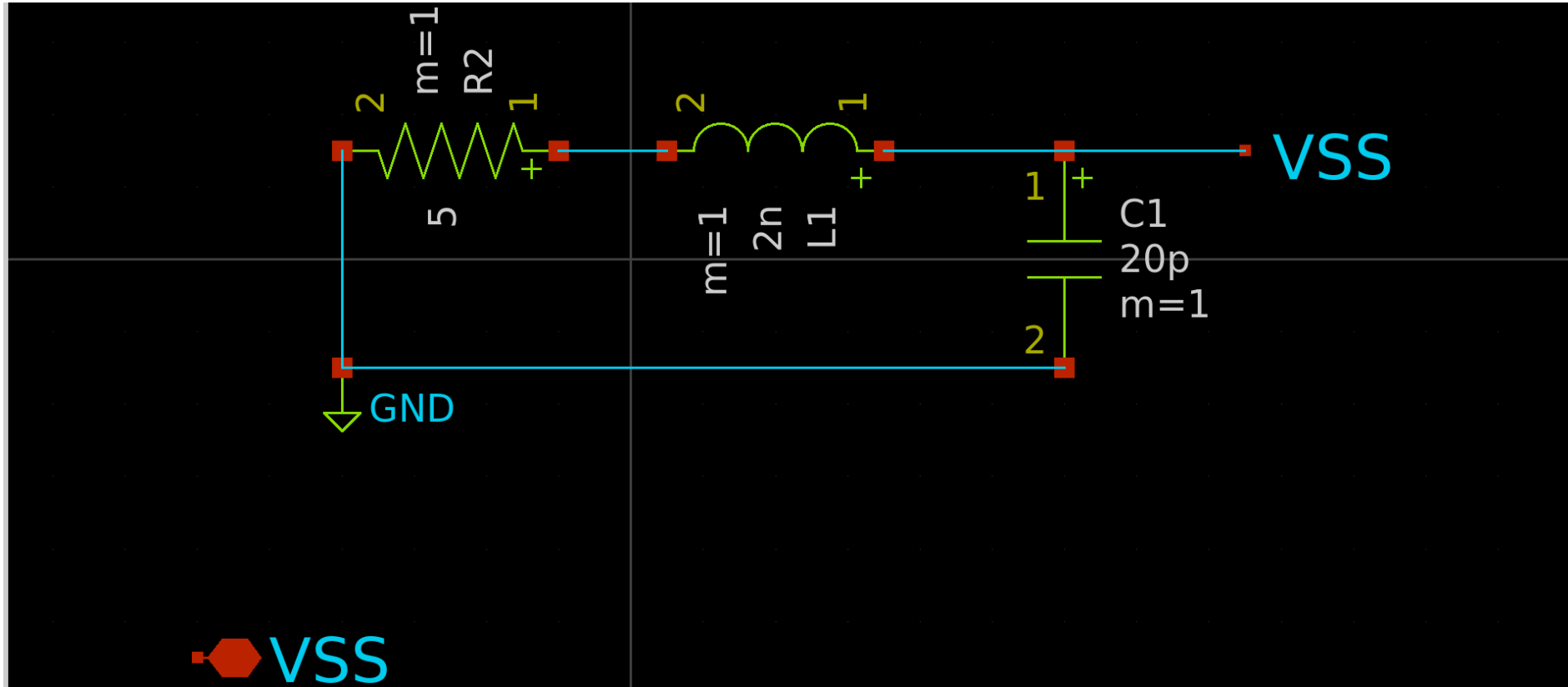
Power Supply



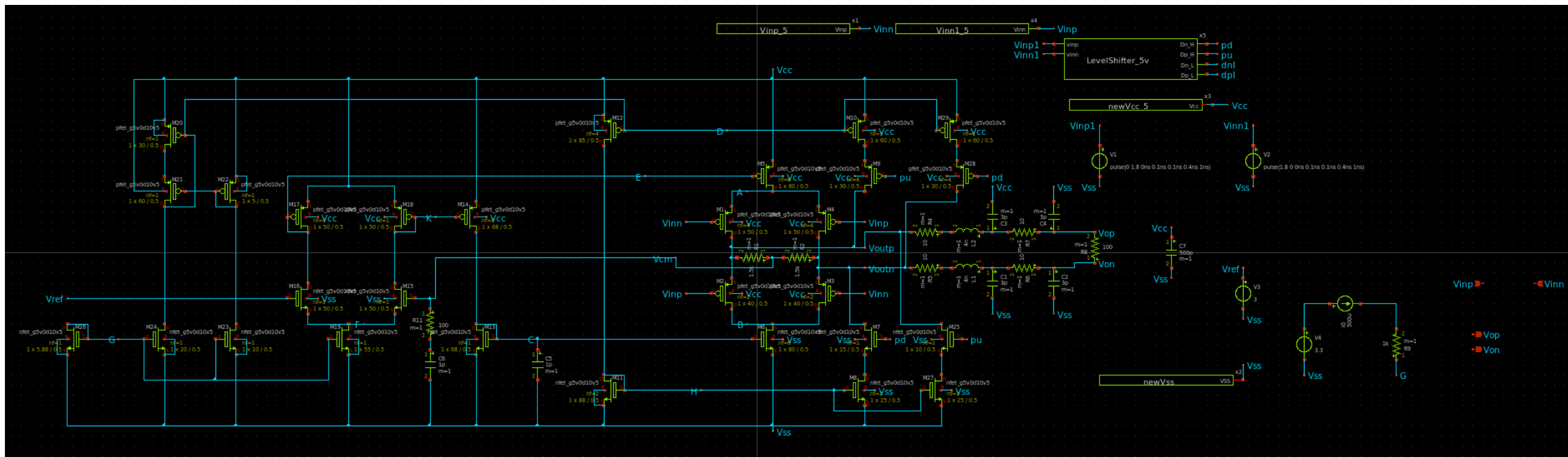
Power Supply (1.8V)



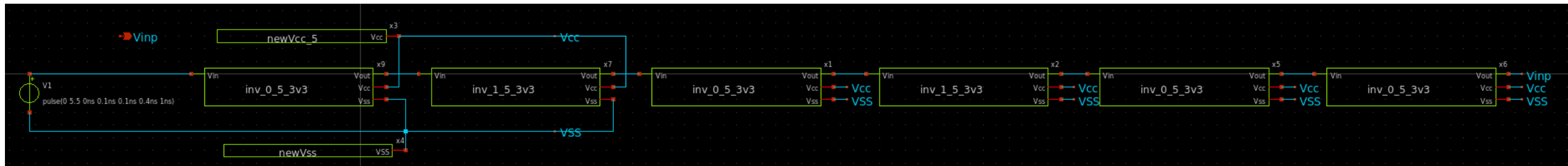
VSS(Ground)



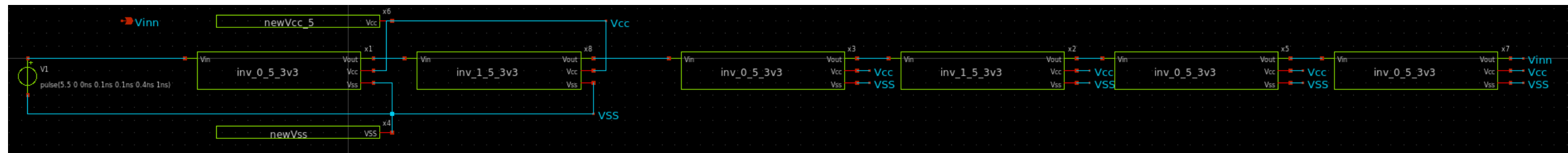
Transmitter



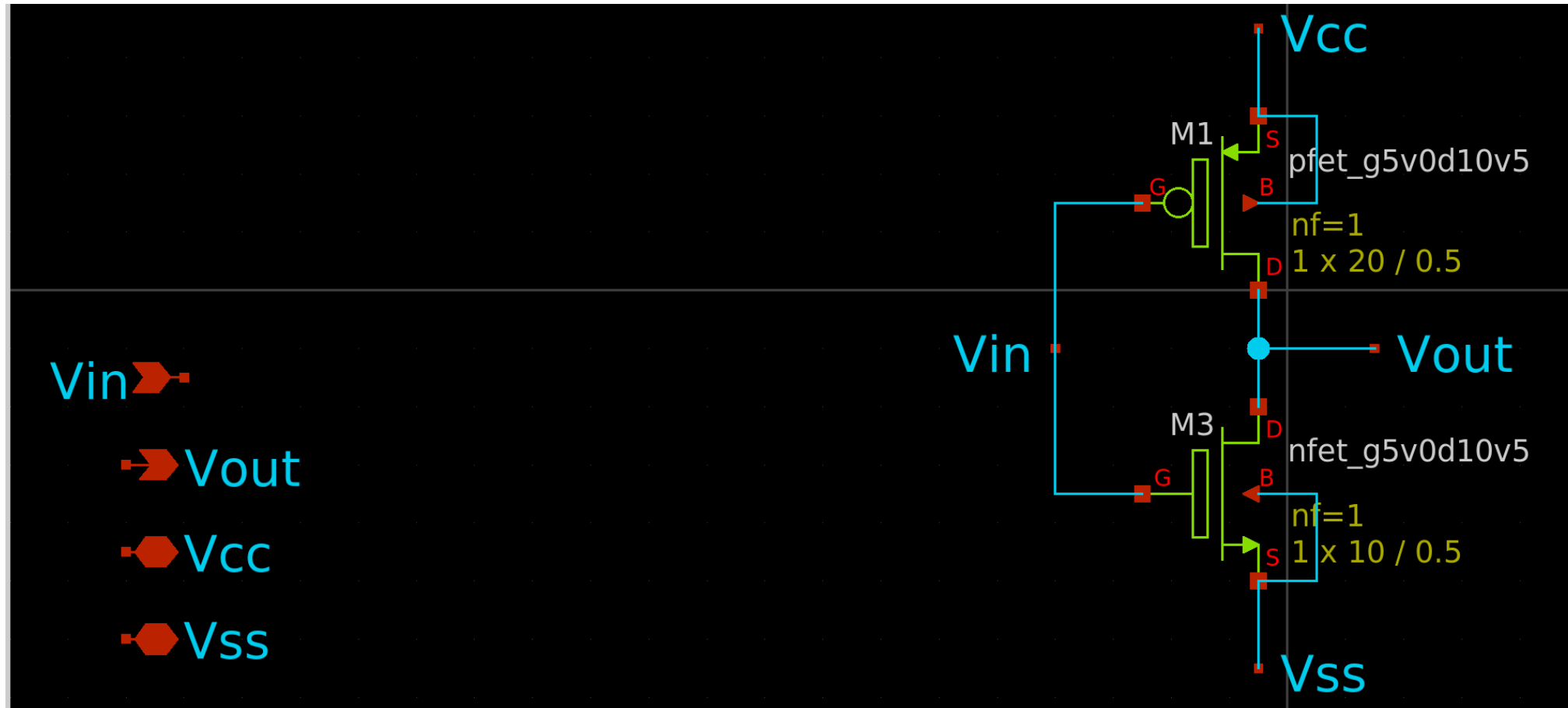
Input Pulse (Positive Stimulus)



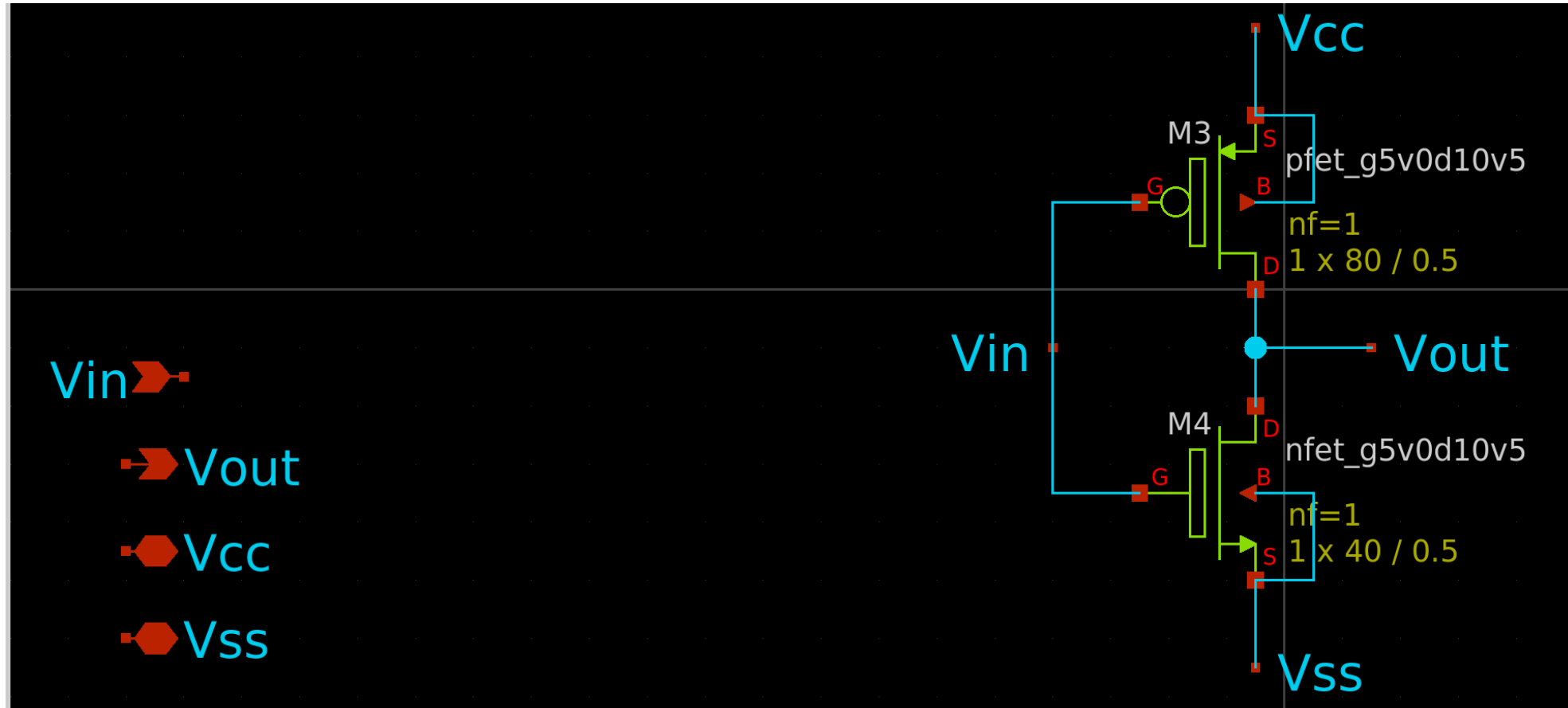
Input Pulse (Negative Stimulus)



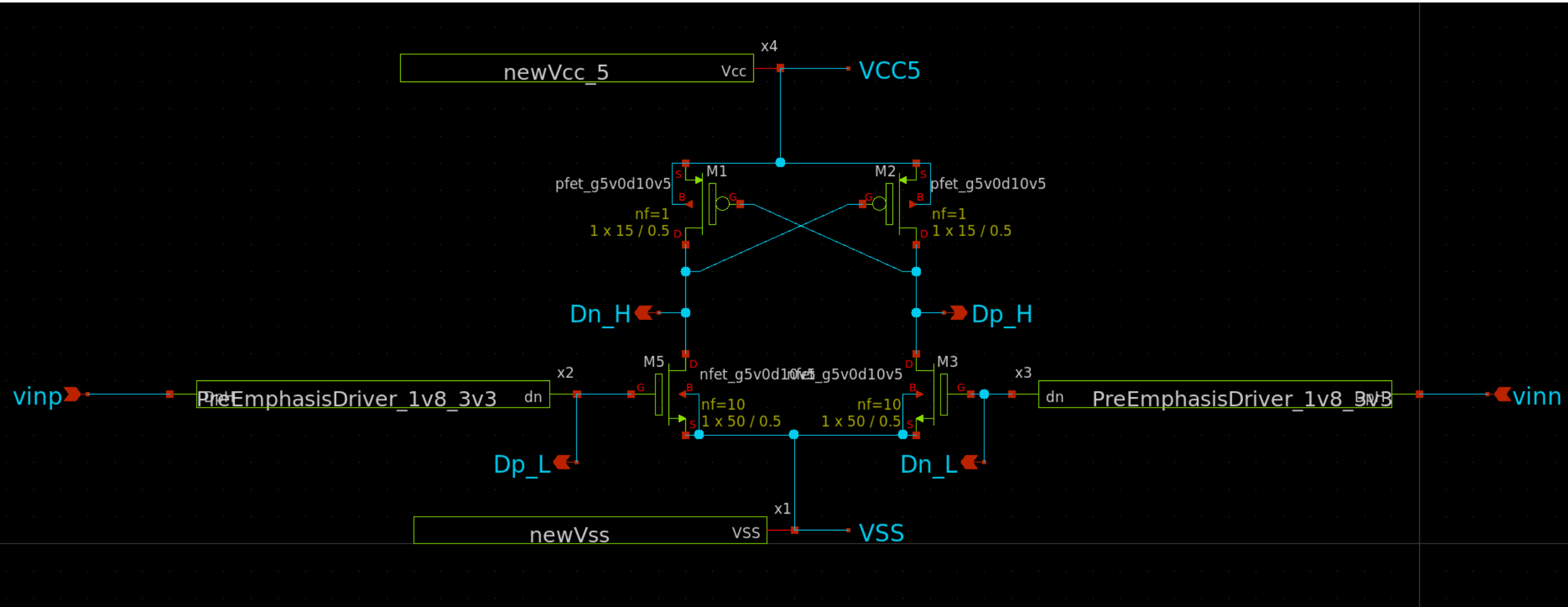
Stimulus Inverter 1



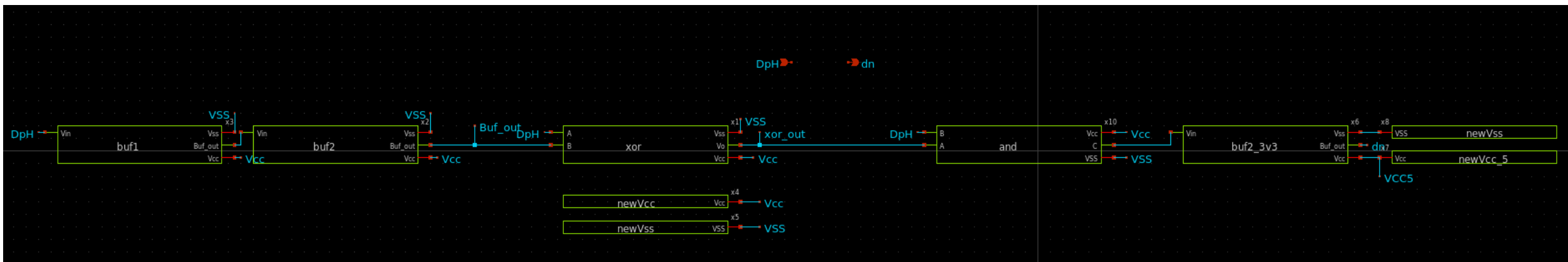
Stimulus Inverter 2



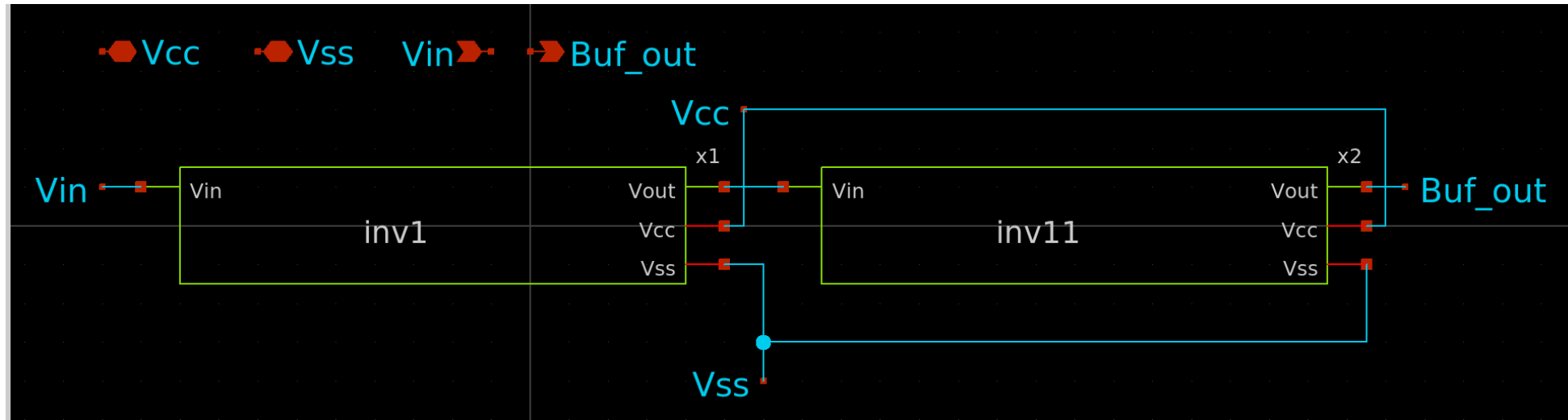
Level Shifter



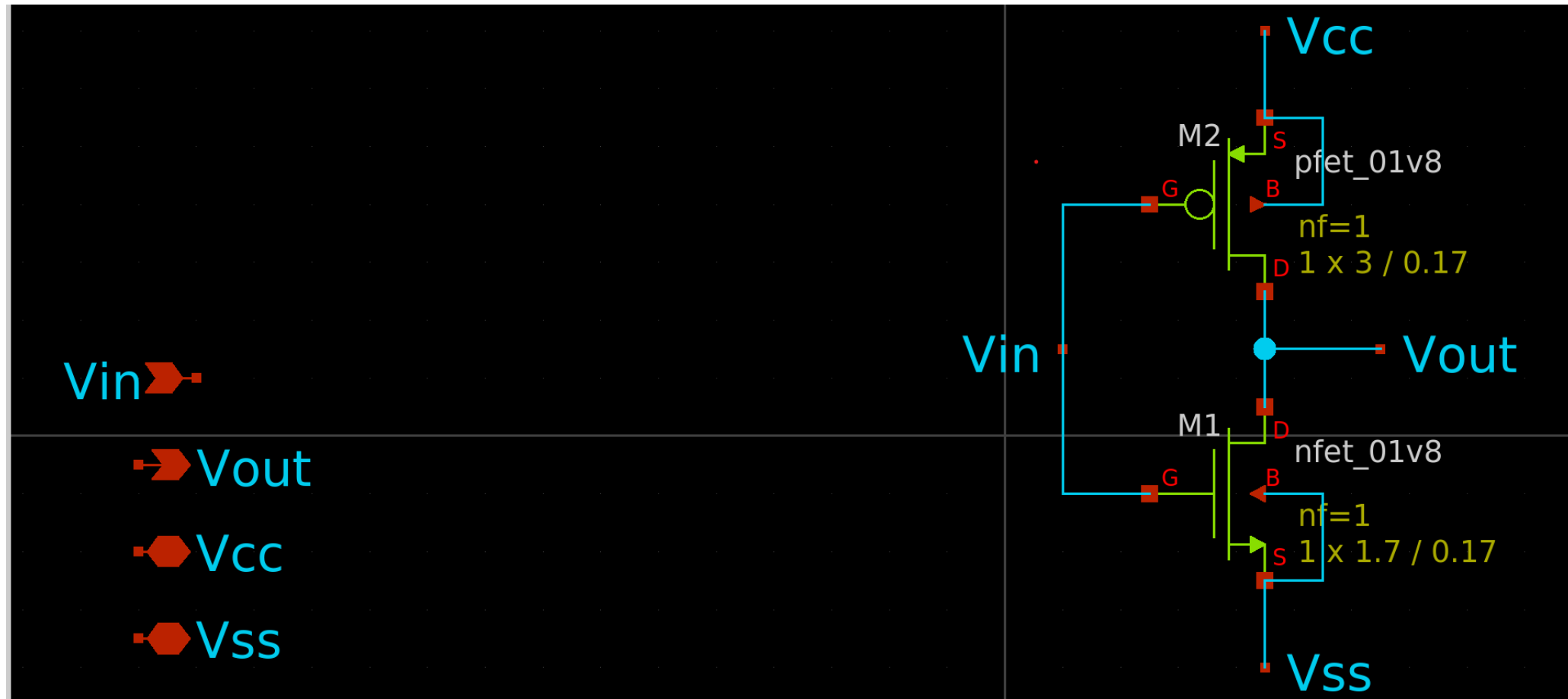
Pre-Emphasis Driver (PED)



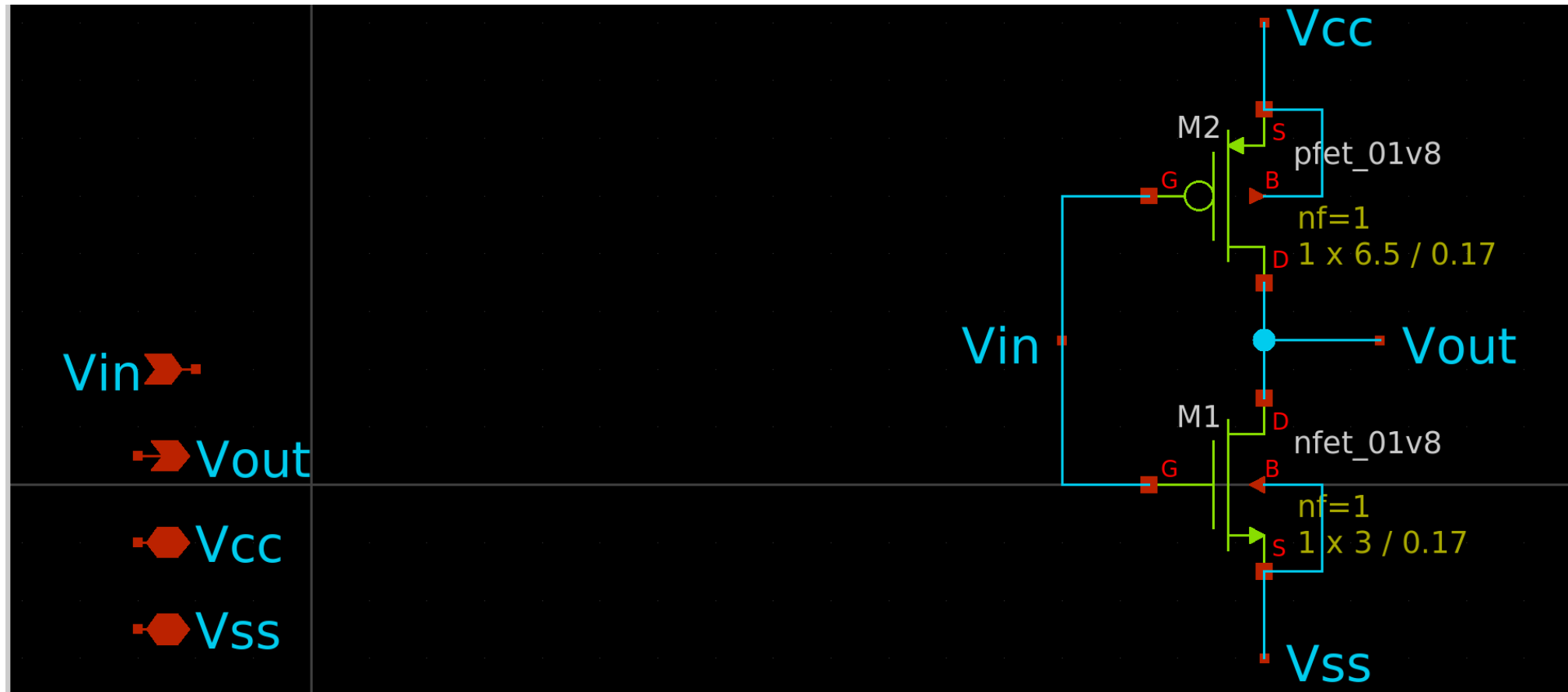
PED Buffer 1



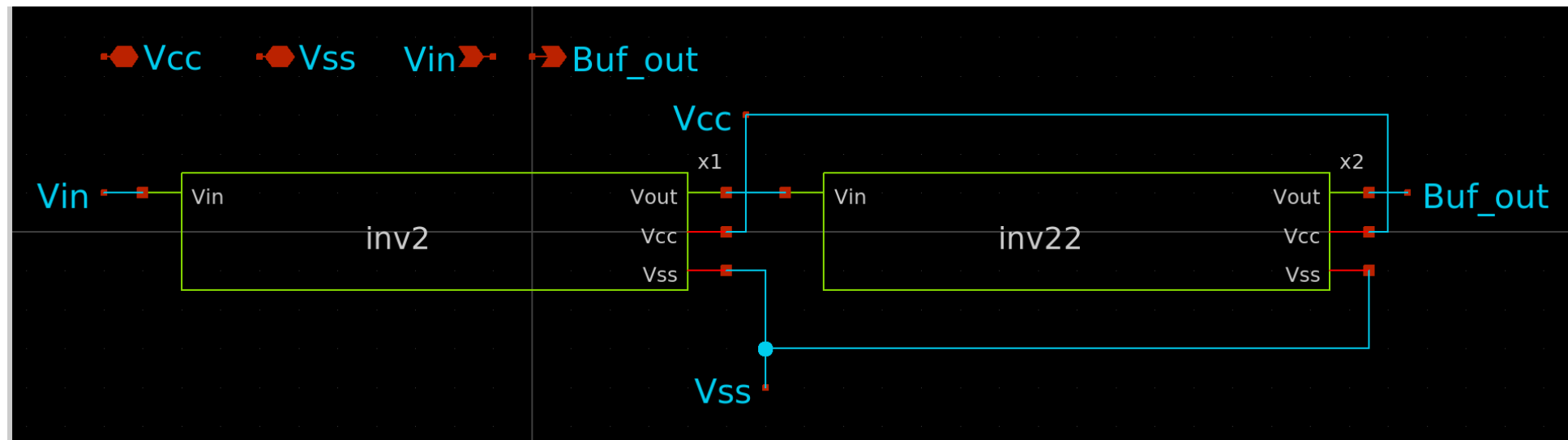
1.8V Inverter 1 (PED Buffer 1)



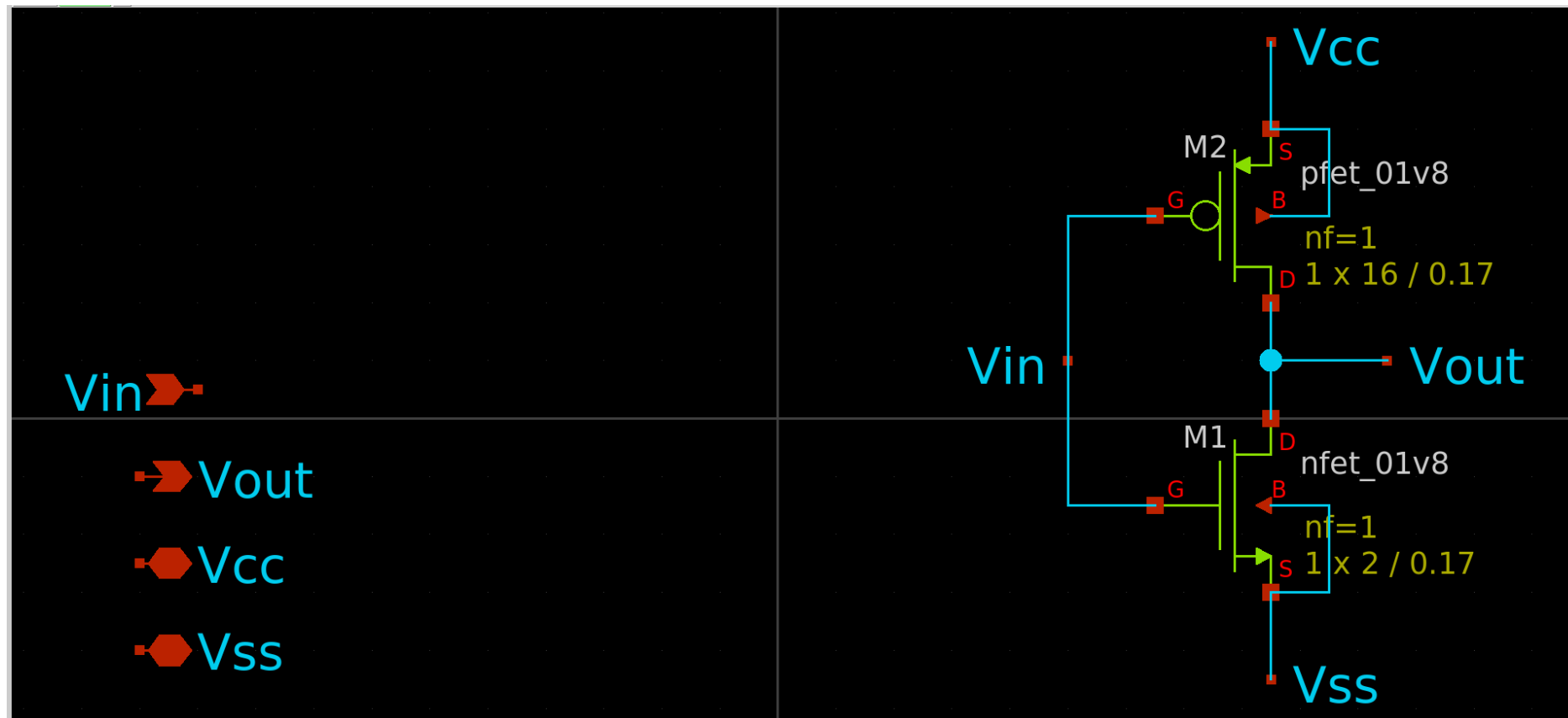
1.8V Inverter 2 (PED Buffer 1)



PED Buffer 2



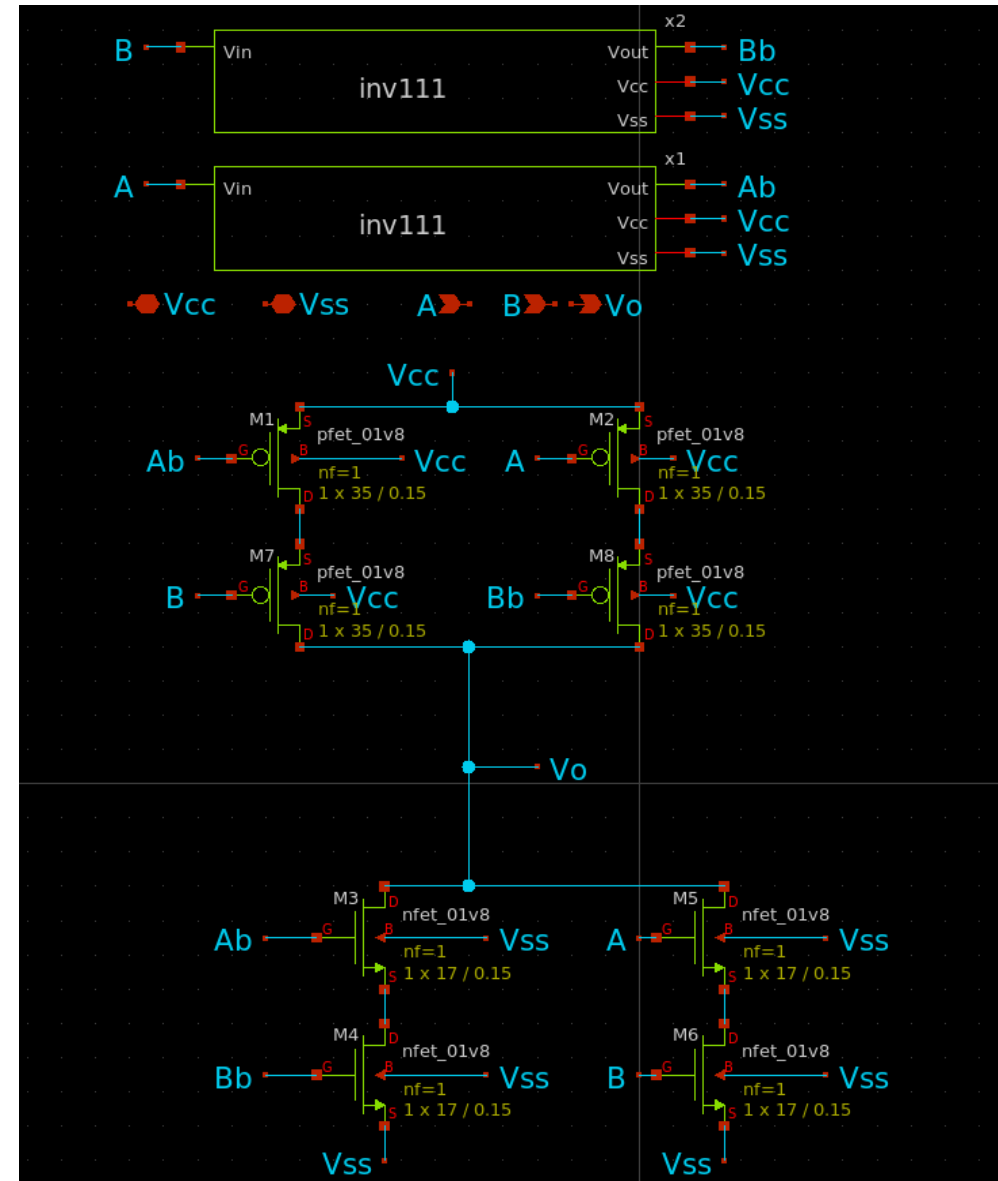
1.8V Inverter 1 (PED Buffer 2)



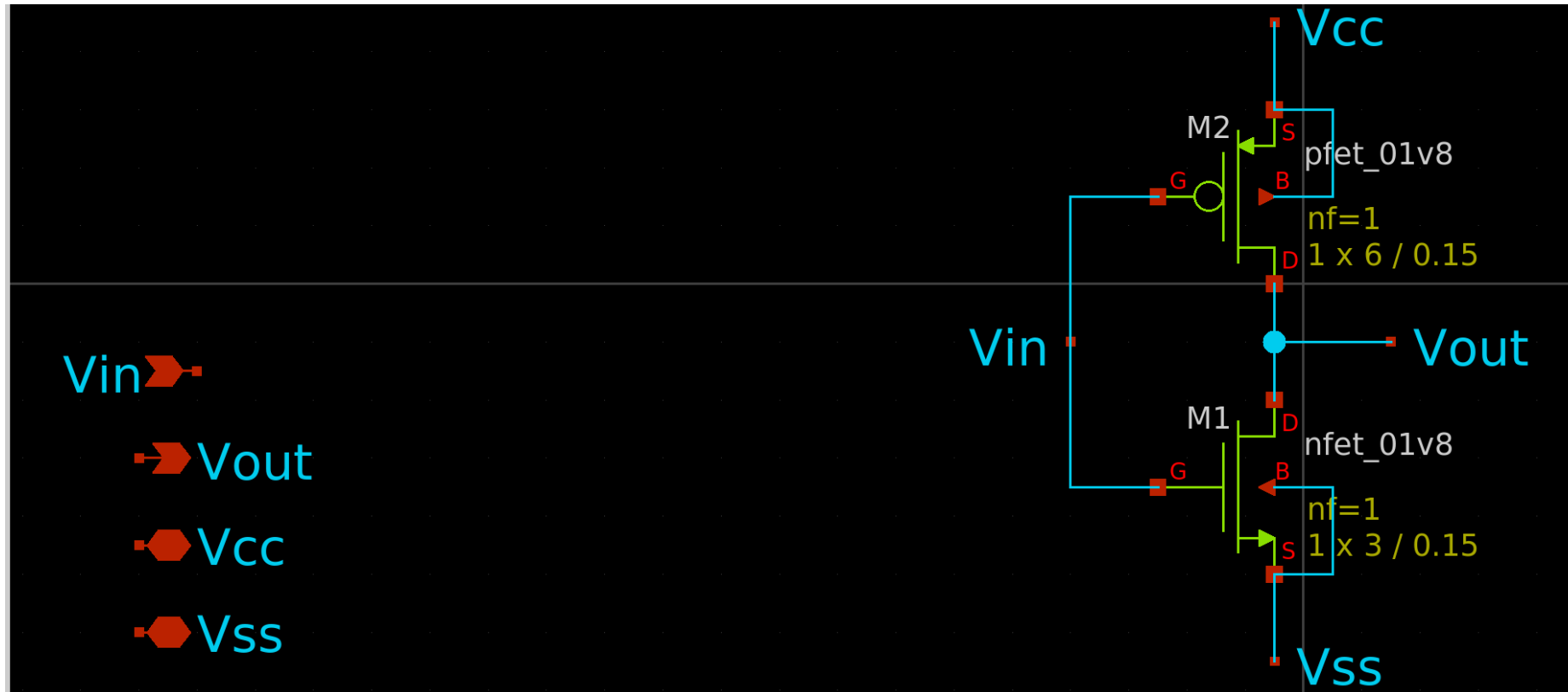
1.8V Inverter 2 (PED Buffer 2)



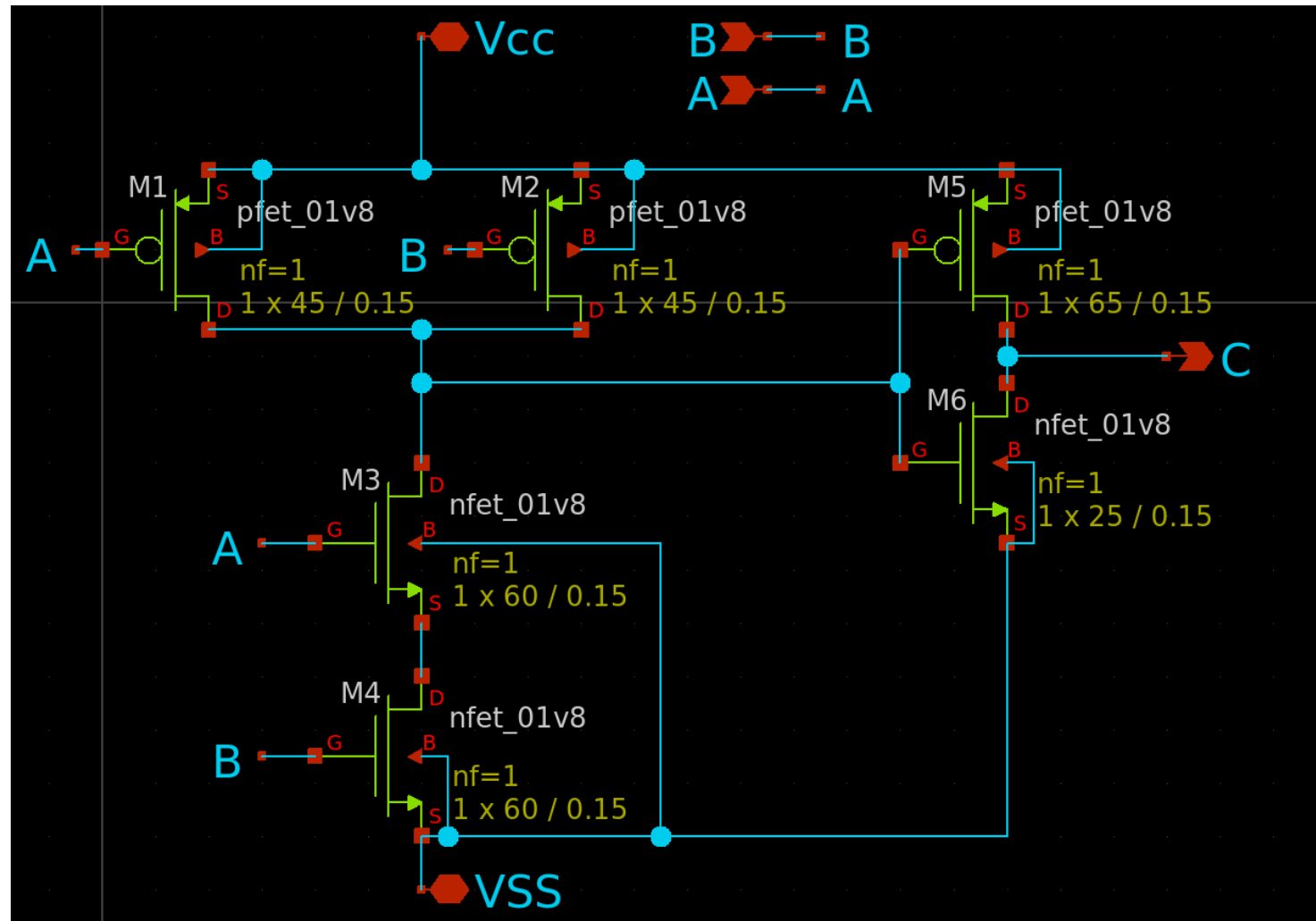
PED EX-OR Gate



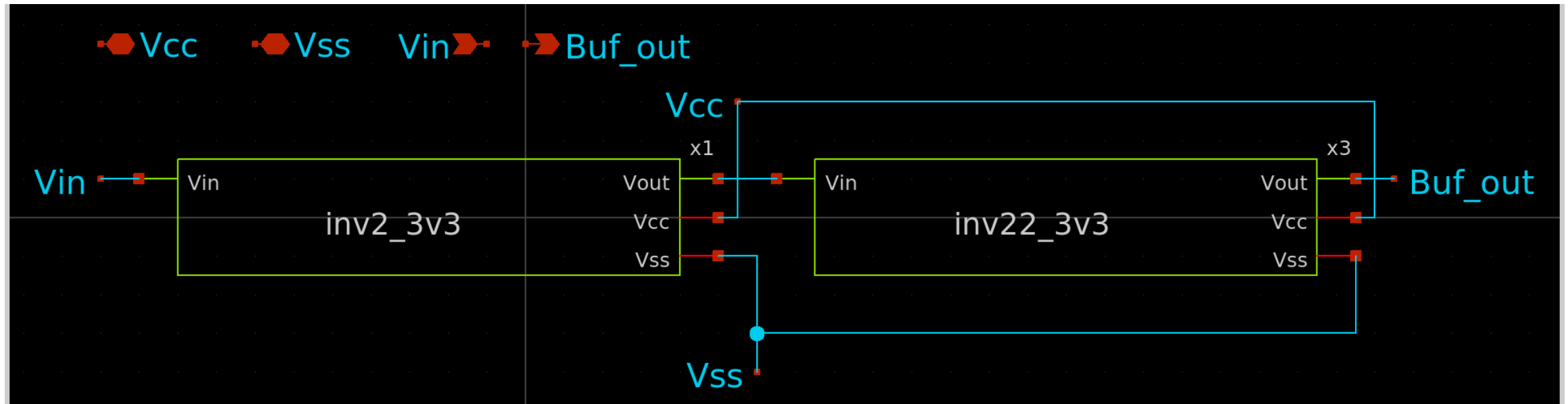
Inverter (PED EX-OR Gate)



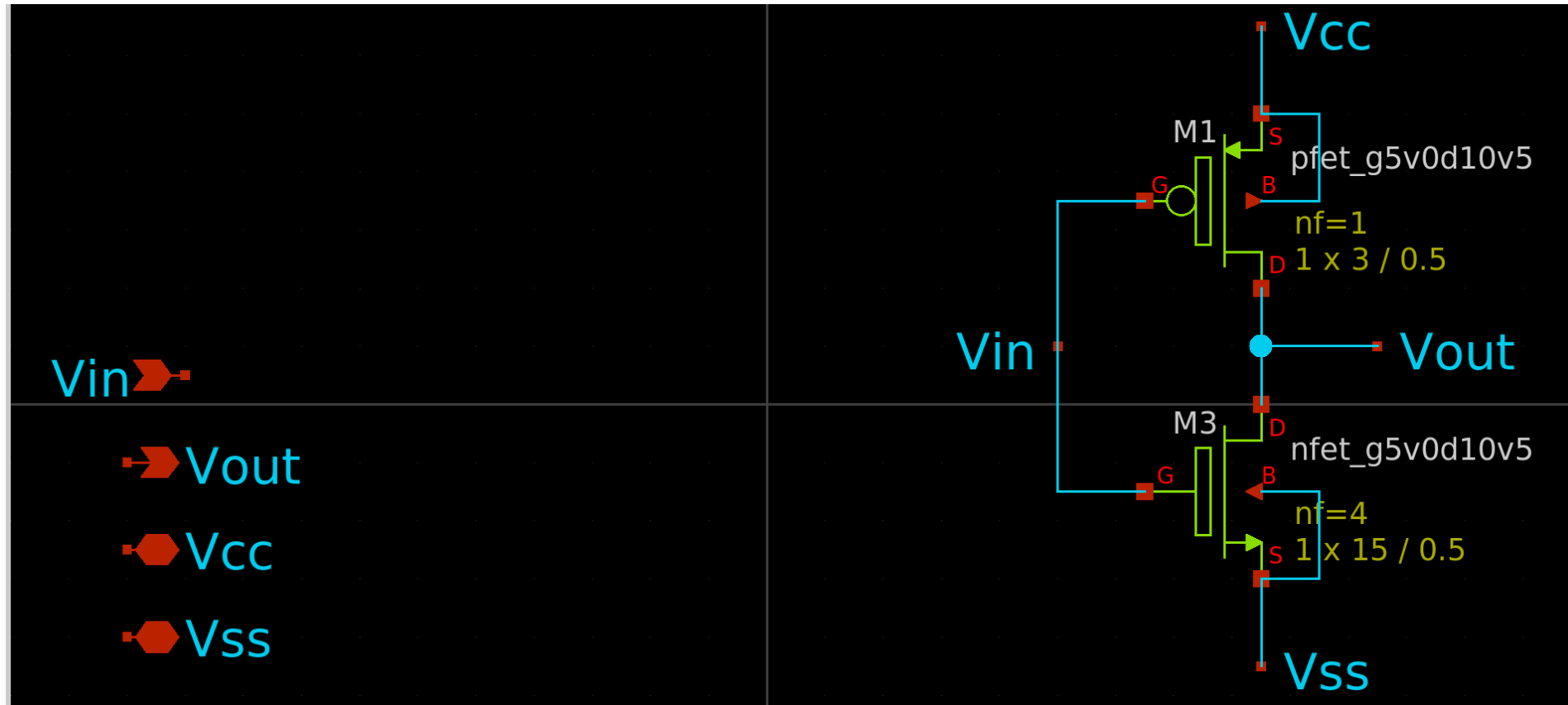
PED AND Gate



PED Buffer 5V



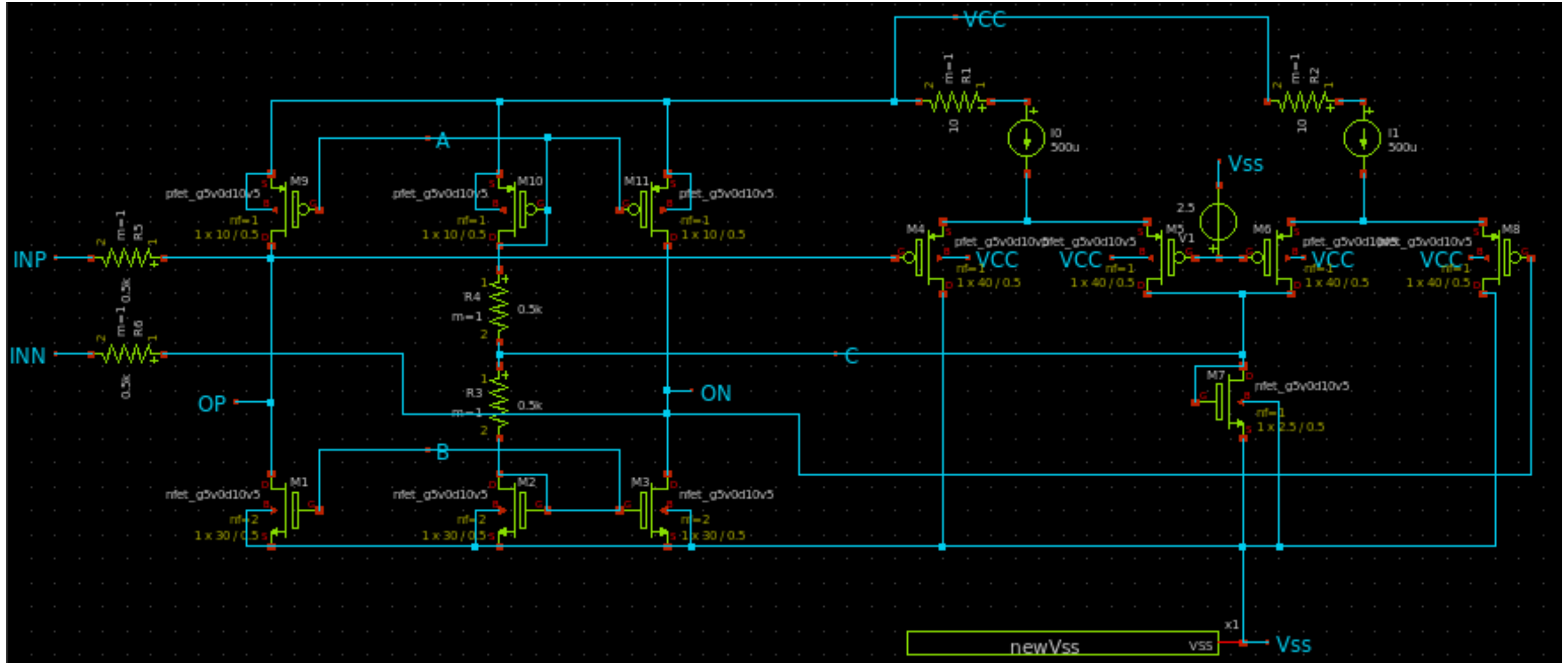
Inverter 1 (PED Buffer 5V)



Inverter 2 (PED Buffer 5V)



Common Mode Level Shifter (Receiver)



Rail-to-Rail Comparator (Receiver)

