LVDS Transceiver (Tx/Rx) Design
With 5V Devices in
Skywater130nm Open-Source Silicon Process

November 2023
Revision 0.1

PO Box 9276
San Jose, CA 95157
www.lewiz.com
Email: support@lewiz.com

Table of Contents

A 1 Gbps LVDS Transceiver in SkyWater 130 nm Technology

1. Overview

Low-voltage differential signaling (LVDS), also known as TIA/EIA-644, is a technical standard that specifies electrical characteristics of a differential, serial signaling standard. Many data communication standards and applications use it and add a data link layer as defined in the OSI model on top of it. LVDS offers a data rate as high as 3.125 Gbps, way higher than other differential signaling standards but, with a trade-off of shorter cable length, as low as 10 m.

LVDS applications include as a driver, receiver, transceiver, and Buffer. A LVDS transceiver combines the functions of both the receiver and the driver into a single component, enabling bidirectional communication and support for multi-drop and multipoint topologies. The purpose of a LVDS transceiver is to interconnect circuits or equipment via a reliable data communications link.

2. Input-Output

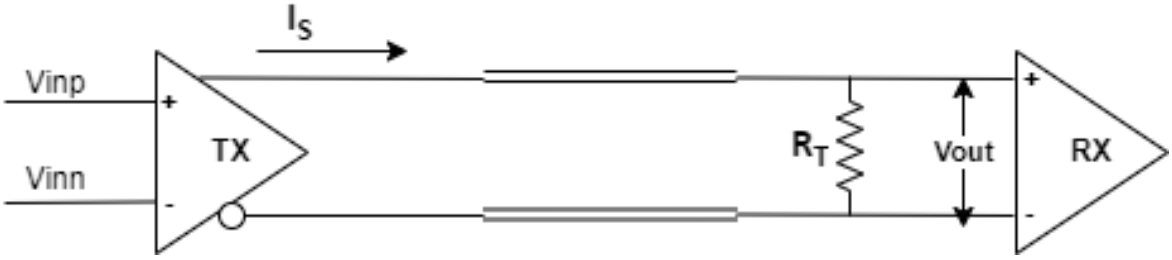

Figure 1. Top Level I/O Block Diagram

A typical LVDS serial link point-to-point communication is shown. Vinn is the input voltage to the inverting terminal and Vinp is the input voltage of the non-inverting terminal. A typical serial link involves a single transmitter (TX) and receiver (RX) pair. A current source (Is) is derived from the TX, and the output amplitude Vout is formed by the current source flowing through the terminated resistor (RT) to establish voltage in the input of RX. By changing the current direction, the same amplitude with the opposite polarity is created to generate the logic of zeros and ones.

3. Block Diagram

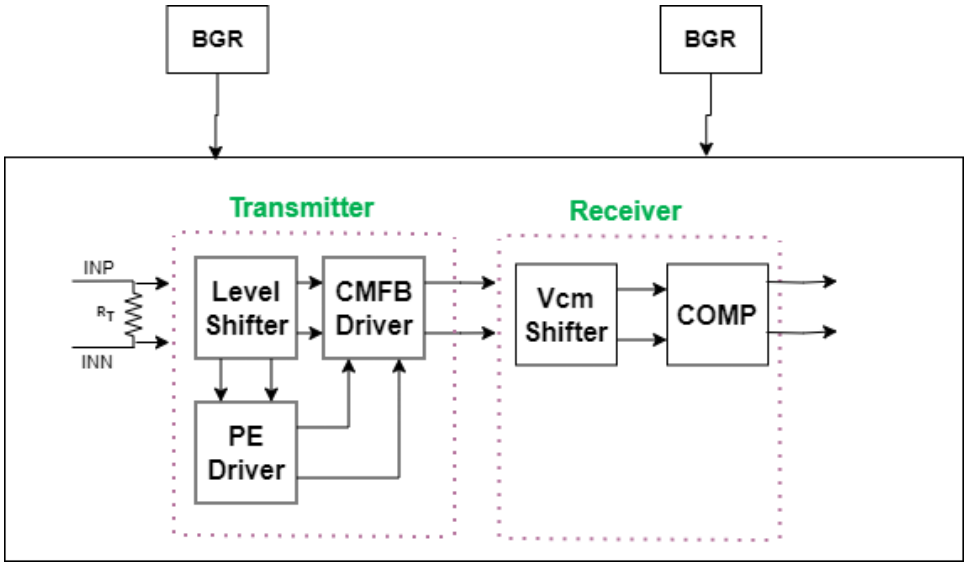

Figure 2 Architectural Block Diagram of the Transceiver

The proposed LVDS transceiver is shown in the figure. It employs differential data transmission, and the receiver is configured as a switched-polarity signal generator. The transmitter includes a CMOS H-bridge output driver with a common mode feedback (CMFB) circuit, a high-speed level shifter (LS) and pre-emphasis (PE) driver, while the receiver is composed of a pre-stage common mode voltage (Vcm) shifter and a rail-to-rail comparator (COMP). In addition, two bandgap references (BGR) are embedded in the scheme to provide proper DC bias for transmitters and receivers, respectively. The transmitter deals with the input data and sends them to the receiver. Then the receiver addresses the data. Therefore, only if both the transmitter and receiver are operated properly can the transmitted signals be output.

4. Electrical Characteristics

	SKY130 130 nm CMOS
Supply Voltage (V)/ VREF	5/1.8
Output Swing (mV)	340
Data Rate (Gbps)	1
Power (mW)	190
FOM # (mW/Gbps)	190
Common Mode Voltage (V)	3.4 (Driver)
Common Mode Input Voltage Range (V) (Receiver)	2.6-3.9

FOM = Power/Data Rate

Table 1

Parameters	Description	Min	Max	Units
VOD	Differential output voltage	256	428	mV
VOS	Offset voltage	3.379	3.383	V
DVOD	|Change to VOD|		5	|mV|
DVOS	|Change to VOS|		95	|mV|
ISA, ISB	Short circuit current		27	|mA|
tr/tf	Output rise/fall times (1 Gbps)		0.381	ns
IIN	Input current		20	|µA|
VTH	Receive threshold voltage		80	mV
VIN	Input voltage range	0	5.5	V
	Output common mode voltage	0.76	4.13	V

† tui is unit interval (i.e. bit width).

Table 2

Appendix:

- VOD - Output differential voltage: the amplitude result of (DO+) – (DO-)
- DVOD - Output differential voltage unbalanced: the difference in amplitude between the positive and negative LVDS outputs
- VOS - Offset voltage: the common-mode voltage of the LVDS output
- DVOS - Offset voltage unbalanced: the difference in common-mode voltage between the positive and negative LVDS outputs
- IIN - Input current: the amount of current drawn by each TTL input

5. Architecture Design

5.1 Receiver

Common Mode Voltage Shifter

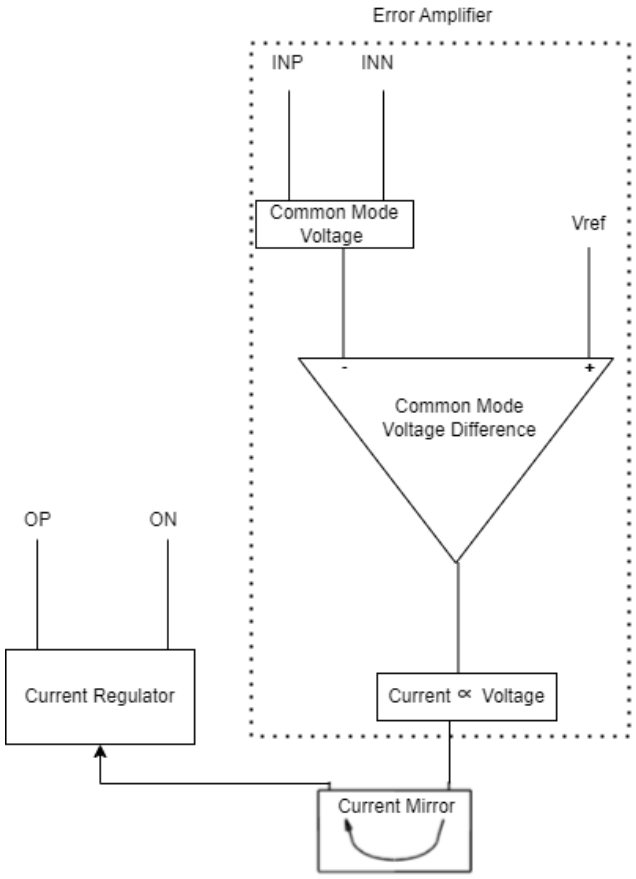

Figure 3 Architectural Block Diagram of the Common Mode Voltage Shifter

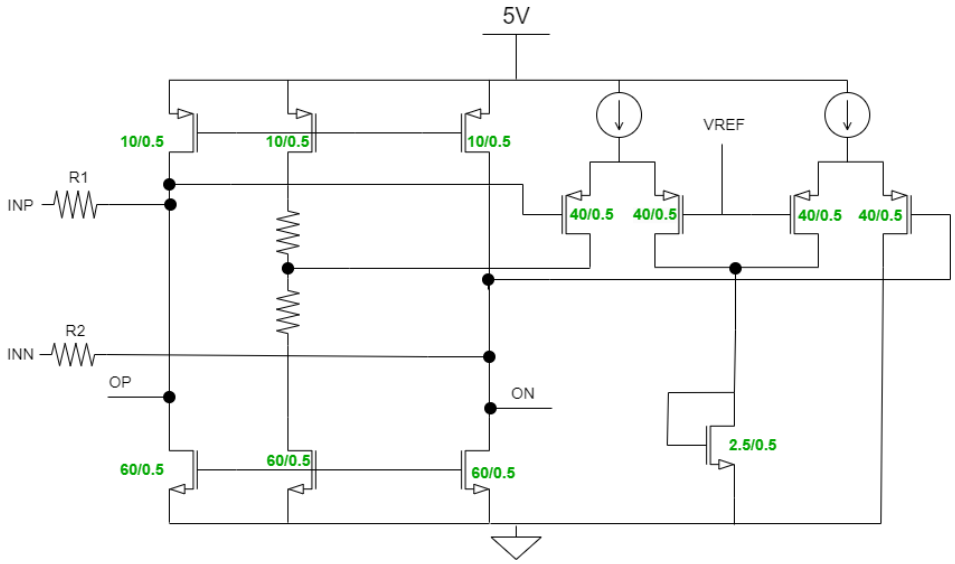

Figure 4. Schematic of the Voltage Shifter

Note: INP = Tx_out_plus, INN = Tx_out_minus, OP = Rx_in_plus, ON = Rx_in_minus

The receiver may need to achieve the common mode voltage conversion to operate in a wide input common mode voltage range. The simplistic circuit of a pre-stage common mode voltage shifter includes a current regulator and an error amplifier. The error amplifier detects the common mode voltage difference between input data (INP and INN) and reference voltage (VREF) and amplifies the voltage difference to control the current regulator by injecting or extracting currents from resistors R1 and R2. As a result, voltage drops across R1 and R2 are generated, and the common mode voltage is shifted.

Rail-to-Rail Comparator

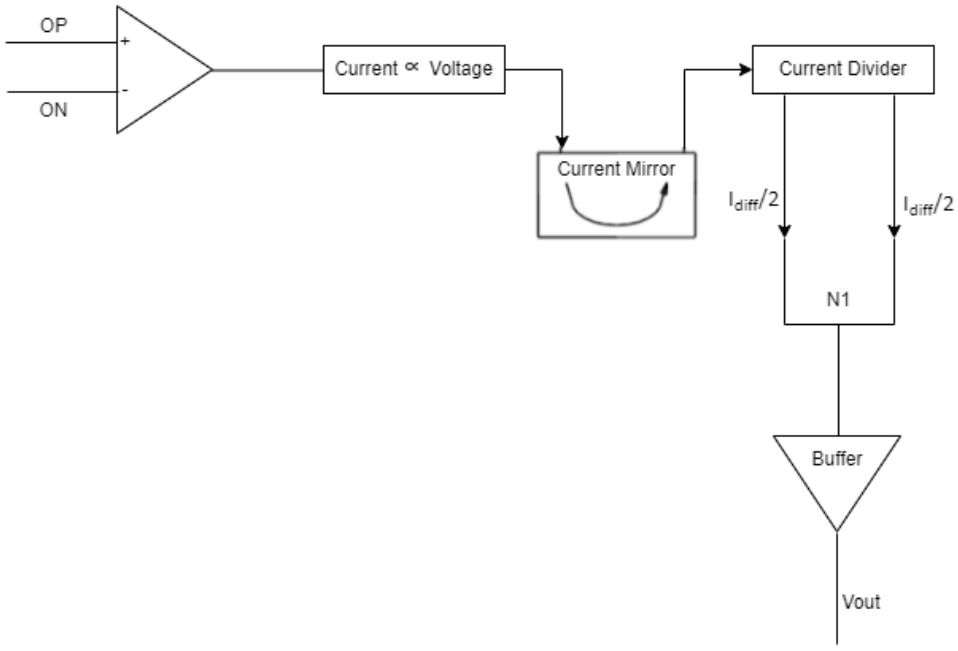

Figure 5. Architectural Block Diagram of Rail-to-Rail Comparator

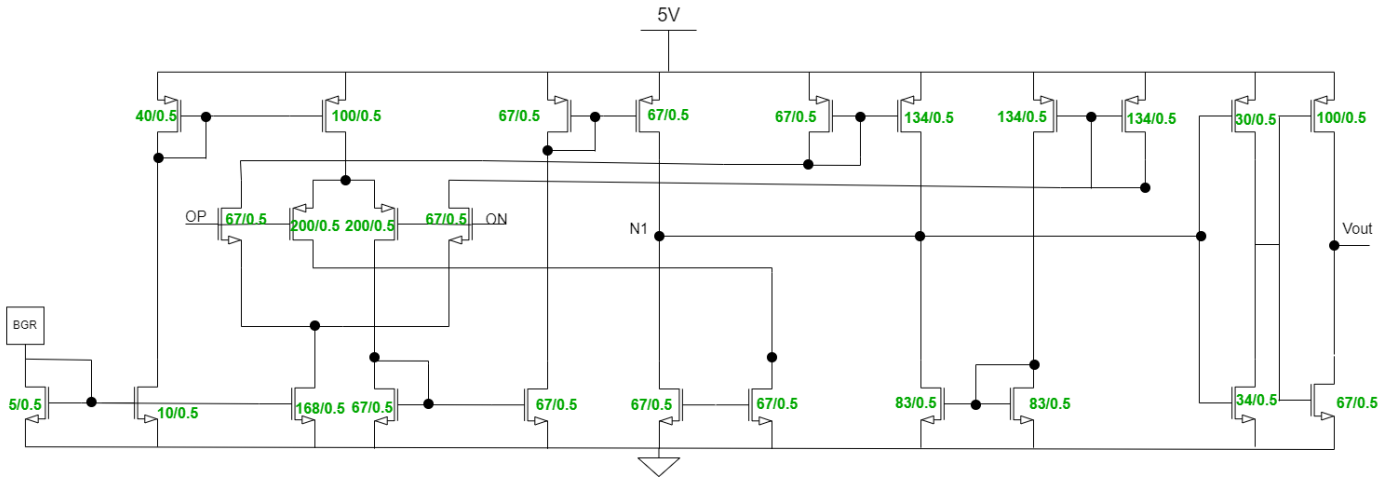

Figure 6. Schematic of Rail-to-Rail Comparator

Note:

1. OP = Rx_in_plus, ON = Rx_in_minus, Vout = Rx_out
2. For our Design, the Bandgap Reference Voltage source was taken to be 3.3V, with the current source as 500 uA

A simple rail-to-rail comparator is constructed as a composite of P and NMOS pairs. The output of the common mode voltage shifter is fed to the Rail-to-Rail Comparator. The amplifier with rail-to-rail input identifies the voltage difference from the input data and converts them into currents through the input trans-conductor cell. After this, the currents are both mirrored and summed up at the node N1, before the data is reinstituted and reshaped by the last stage shaping buffer.

5.2 Transmitter

The transmitter contains three parts: a high-speed level shifter, a pre-emphasis driver, and an output driver.

High-Speed Level Shifter:

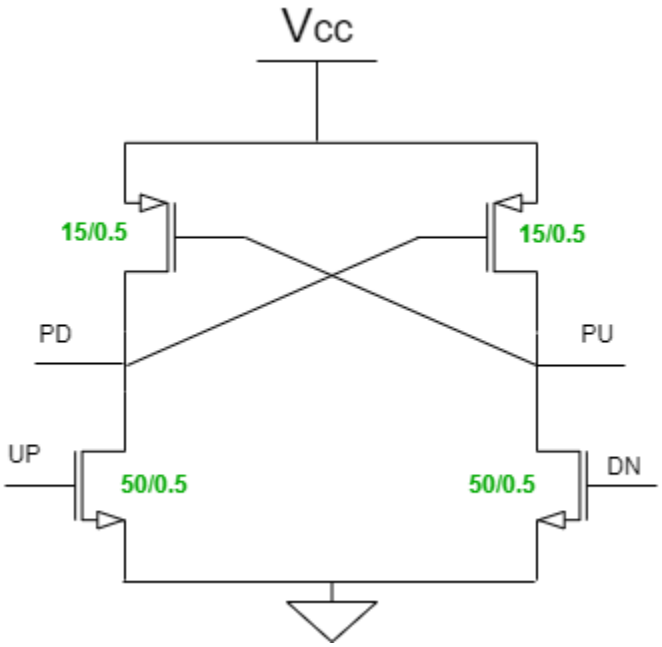

Figure 7. Schematic of High-Speed Level Shifter

The high-speed level shifter reinforces and reshapes the input. A pair of NMOS devices receive the input signals (UP and DN), reshape and make them robust through the positive feedback transistors and output the pulses (PD and PU).

Output Driver:

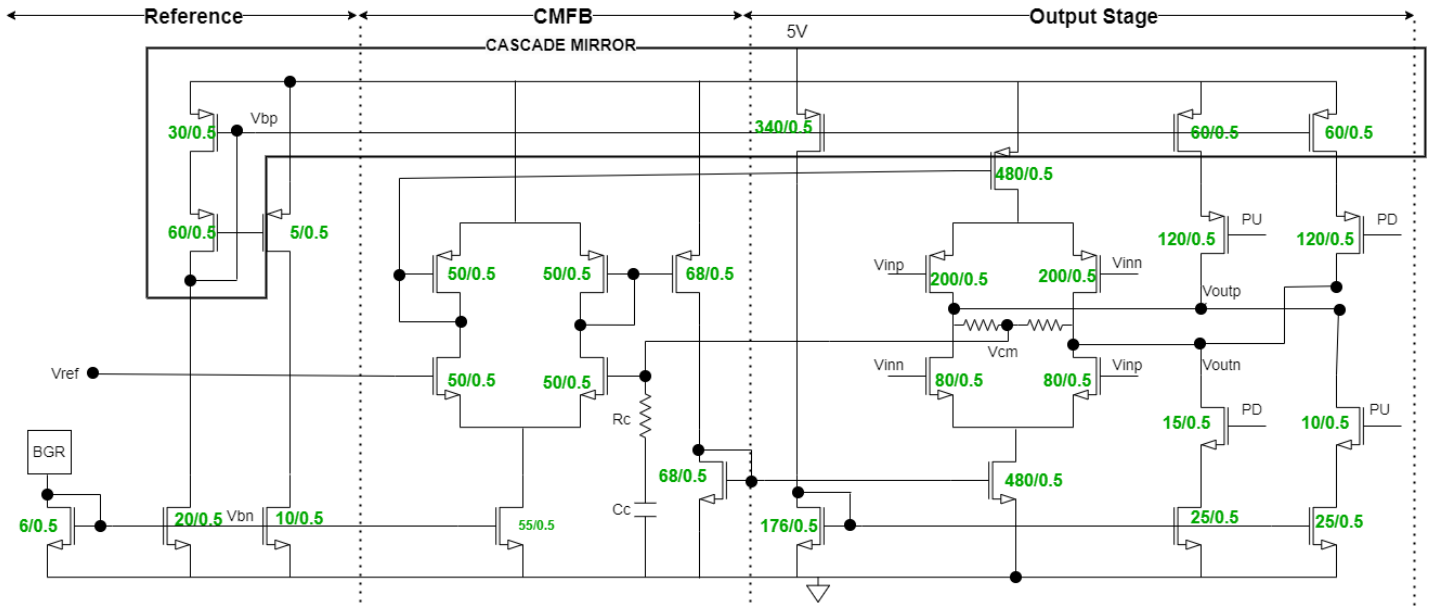

Figure 8. Schematic of Output Driver

Note:

1. Vinp = Tx_in_plus, Vinn=Tx_in_minus, Voutp=Tx_out_plus, Voutn = Tx_out_minus
2. For our design, the Reference voltage was taken as 3V

The figure shows the proposed transmitter output driver based on the CMOS H-bridge structure. A simple common mode feedback (CMFB) circuit is used to stabilize the output common mode voltage (Vcm), and is less dependent on PVT. The two differential output voltages (Voutp and Voutn) are averaged to form a common mode voltage (Vcm) by two resistors, which is compared with the designed reference common mode voltage (Vref). The difference is then amplified and converted into the common mode current to adjust the common mode voltage (Vcm). In addition, a Rc and Cc pole-zero compensation network is exploited to obtain an adequate phase margin of CMFB under the conditions created by the PVT variations. Meanwhile, a cascade current mirror is utilized to provide high precision current bias at the voltage supply.

Pre-Emphasis Driver

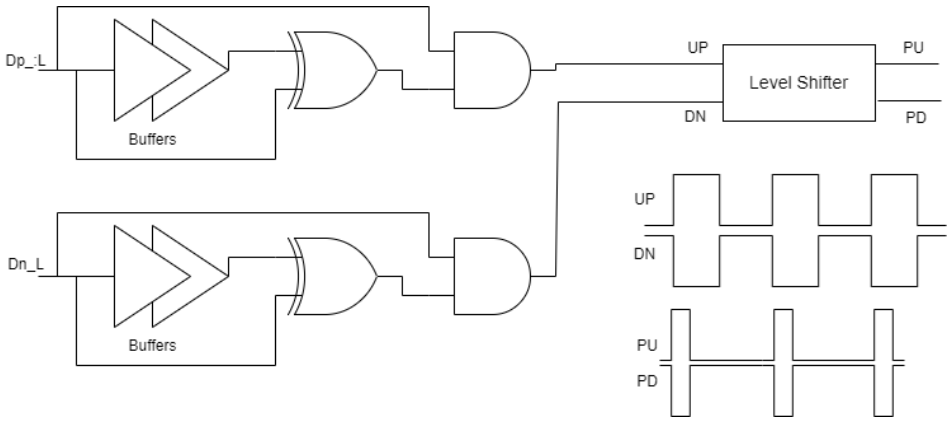

Figure 9. High level schematic of Pre-Emphasis Driver

Lower level (1.8 V) voltage pulses are fed as the input of the Pre-Emphasis Driver. Pulse Width Modulation is applied to these pulses by the gating circuit shown. These pulses (UP and DN) are then amplified and reinforced before applying them (PU and PD) to the Output Driver. The duty cycle of these pulses is such that they just enable injection and extraction of currents from the output nodes of the driver, during the rise and fall of driver output voltages. This decreases the rise and fall times of the driver outputs.

6. References

[1]. X. Bai, J. Zhao, S. Zuo, and Y. Zhou, “A 2.5 Gbps, 10-Lane, Low-Power, LVDS Transceiver in 28 nm CMOS Technology,” *Electronics*, vol. 8, no. 3, pp. 350–350, Mar. 2019, doi: https://doi.org/10.3390/electronics8030350.

[2]. “LVDS Lectures - YouTube,” *www.youtube.com*. https://www.youtube.com/playlist?list=PL2OY4oaCu4Bj8WJjveunbnvQ9mzQ45yuy (accessed Nov. 09, 2023).