1. Description

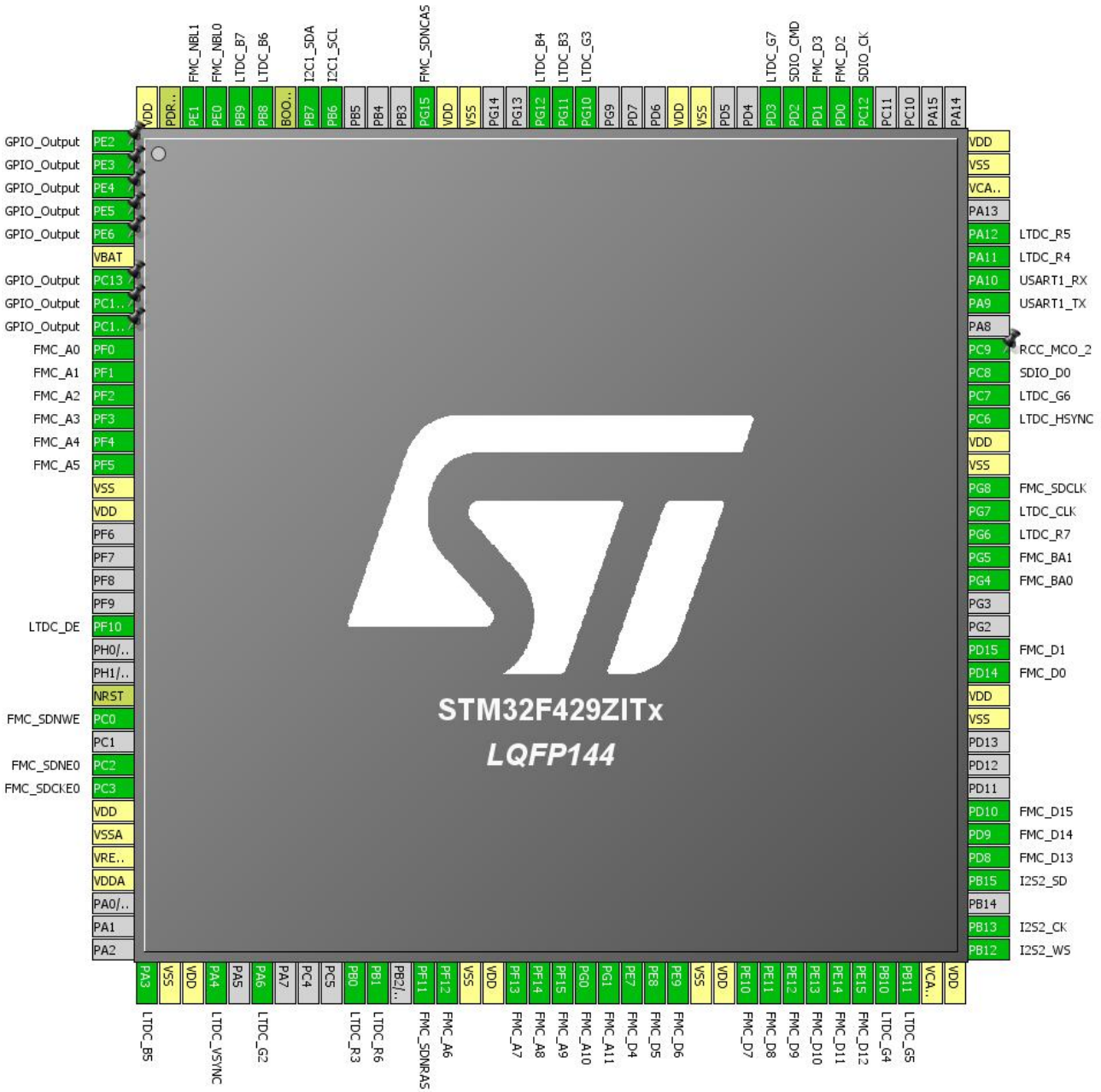
1.1. Project

Project Name	SLSF4
Board Name	SLSF4
Generated with:	STM32CubeMX 4.11.0
Date	12/20/2015

1.2. MCU

MCU Series	STM32F4
MCU Line	STM32F429/439
MCU name	STM32F429ZITx
MCU Package	LQFP144
MCU Pin number	144

2. Pinout Configuration



3. Pins Configuration

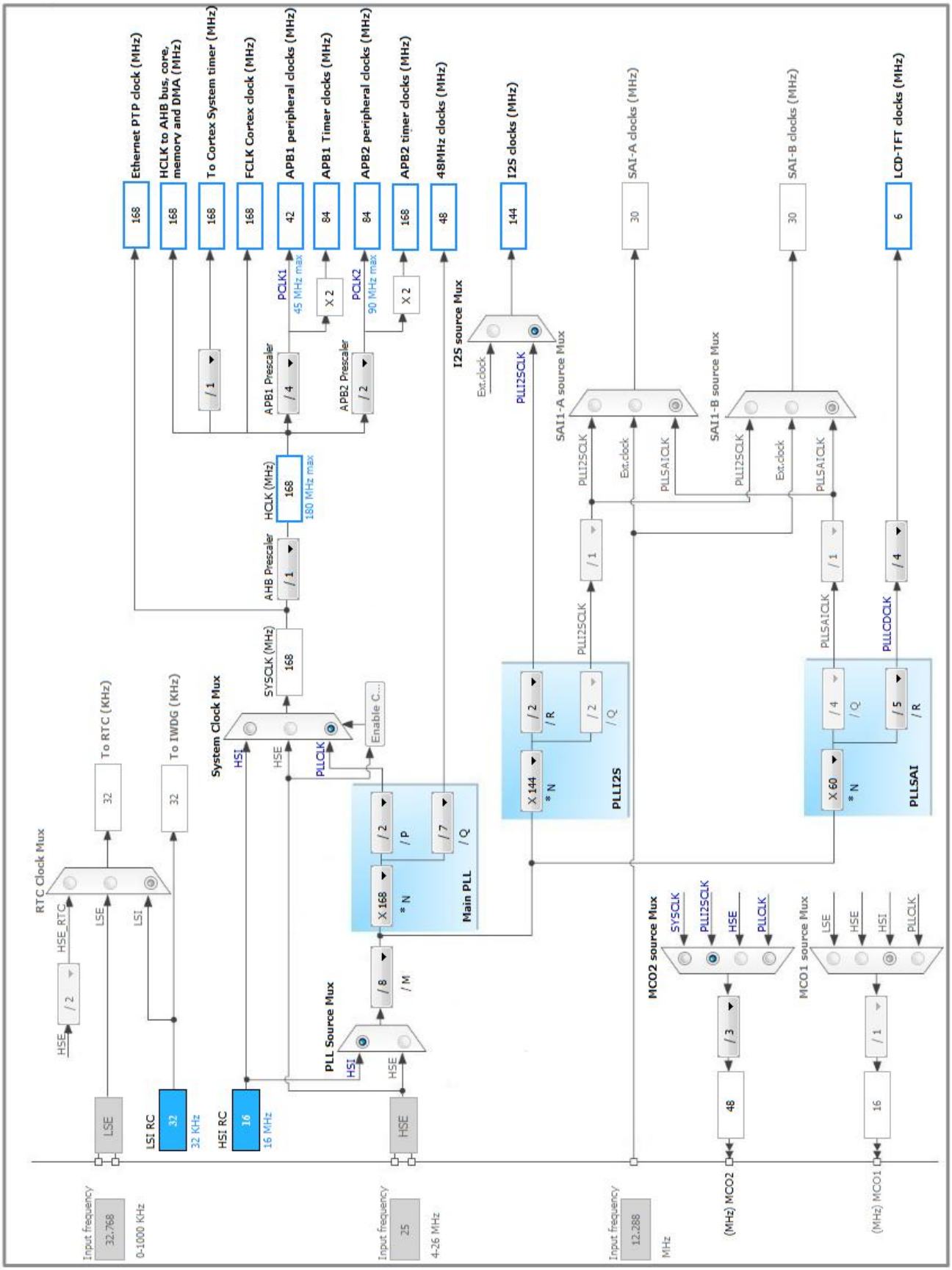
Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	PE2 *	I/O	GPIO_Output	
2	PE3 *	I/O	GPIO_Output	
3	PE4 *	I/O	GPIO_Output	
4	PE5 *	I/O	GPIO_Output	
5	PE6 *	I/O	GPIO_Output	
6	VBAT	Power		
7	PC13 *	I/O	GPIO_Output	
8	PC14/OSC32_IN *	I/O	GPIO_Output	
9	PC15/OSC32_OUT *	I/O	GPIO_Output	
10	PF0	I/O	FMC_A0	
11	PF1	I/O	FMC_A1	
12	PF2	I/O	FMC_A2	
13	PF3	I/O	FMC_A3	
14	PF4	I/O	FMC_A4	
15	PF5	I/O	FMC_A5	
16	VSS	Power		
17	VDD	Power		
22	PF10	I/O	LTDC_DE	
25	NRST	Reset		
26	PC0	I/O	FMC_SDNWE	
28	PC2	I/O	FMC_SDNE0	
29	PC3	I/O	FMC_SDCKE0	
30	VDD	Power		
31	VSSA	Power		
32	VREF+	Power		
33	VDDA	Power		
37	PA3	I/O	LTDC_B5	
38	VSS	Power		
39	VDD	Power		
40	PA4	I/O	LTDC_VSYNC	
42	PA6	I/O	LTDC_G2	
46	PB0	I/O	LTDC_R3	
47	PB1	I/O	LTDC_R6	
49	PF11	I/O	FMC_SDNRAS	
50	PF12	I/O	FMC_A6	
51	VSS	Power		

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
52	VDD	Power		
53	PF13	I/O	FMC_A7	
54	PF14	I/O	FMC_A8	
55	PF15	I/O	FMC_A9	
56	PG0	I/O	FMC_A10	
57	PG1	I/O	FMC_A11	
58	PE7	I/O	FMC_D4	
59	PE8	I/O	FMC_D5	
60	PE9	I/O	FMC_D6	
61	VSS	Power		
62	VDD	Power		
63	PE10	I/O	FMC_D7	
64	PE11	I/O	FMC_D8	
65	PE12	I/O	FMC_D9	
66	PE13	I/O	FMC_D10	
67	PE14	I/O	FMC_D11	
68	PE15	I/O	FMC_D12	
69	PB10	I/O	LTDC_G4	
70	PB11	I/O	LTDC_G5	
71	VCAP_1	Power		
72	VDD	Power		
73	PB12	I/O	I2S2_WS	
74	PB13	I/O	I2S2_CK	
76	PB15	I/O	I2S2_SD	
77	PD8	I/O	FMC_D13	
78	PD9	I/O	FMC_D14	
79	PD10	I/O	FMC_D15	
83	VSS	Power		
84	VDD	Power		
85	PD14	I/O	FMC_D0	
86	PD15	I/O	FMC_D1	
89	PG4	I/O	FMC_BA0	
90	PG5	I/O	FMC_BA1	
91	PG6	I/O	LTDC_R7	
92	PG7	I/O	LTDC_CLK	
93	PG8	I/O	FMC_SDCLK	
94	VSS	Power		
95	VDD	Power		
96	PC6	I/O	LTDC_HSYNC	

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
97	PC7	I/O	LTDC_G6	
98	PC8	I/O	SDIO_D0	
99	PC9	I/O	RCC_MCO_2	
101	PA9	I/O	USART1_TX	
102	PA10	I/O	USART1_RX	
103	PA11	I/O	LTDC_R4	
104	PA12	I/O	LTDC_R5	
106	VCAP_2	Power		
107	VSS	Power		
108	VDD	Power		
113	PC12	I/O	SDIO_CK	
114	PD0	I/O	FMC_D2	
115	PD1	I/O	FMC_D3	
116	PD2	I/O	SDIO_CMD	
117	PD3	I/O	LTDC_G7	
120	VSS	Power		
121	VDD	Power		
125	PG10	I/O	LTDC_G3	
126	PG11	I/O	LTDC_B3	
127	PG12	I/O	LTDC_B4	
130	VSS	Power		
131	VDD	Power		
132	PG15	I/O	FMC_SDNCAS	
136	PB6	I/O	I2C1_SCL	
137	PB7	I/O	I2C1_SDA	
138	BOOT0	Boot		
139	PB8	I/O	LTDC_B6	
140	PB9	I/O	LTDC_B7	
141	PE0	I/O	FMC_NBL0	
142	PE1	I/O	FMC_NBL1	
143	PDR_ON	Reset		
144	VDD	Power		

* The pin is affected with an I/O function

4. Clock Tree Configuration



5. IPs and Middleware Configuration

5.1. FMC

SDRAM 2

Clock and chip enable: SDCKE0+SDNE0

Internal bank number: 4 banks

Address: 12 bits

Data: 16 bits

Byte enable: set

5.1.1. SDRAM 2:

SDRAM control:	
Bank	SDRAM bank 1
Column bit number	8 bits
Row bit number	**12 bits ***
CAS latency	**3 memory clock cycles ***
Write protection	Disabled
SDRAM common clock	**2 HCLK clock cycles ***
SDRAM common burst read	Disabled
SDRAM common read pipe delay	**1 HCLK clock cycle ***
SDRAM timing in memory clock cycles:	
Load mode register to active delay	**2 ***
Exit self-refresh delay	**7 ***
Self refresh time	**4 ***
SDRAM common row cycle delay	**7 ***
Write recovery time	**3 ***
SDRAM common row precharge delay	**2 ***
Row to column delay	**2 ***

5.2. I2C1

I2C: I2C

5.2.1. Parameter Settings:

Master Features:

I2C Speed Mode	Standard Mode
I2C Clock Speed (Hz)	100000

Slave Features:

Clock No Stretch Mode	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0
General Call address detection	Disabled

5.3. I2S2

Mode: Half-Duplex Master

5.3.1. Parameter Settings:

Generic Parameters:

Transmission Mode	Mode Master Transmit
Communication Standard	I2S Philips
Data and Frame Format	**24 Bits Data on 32 Bits Frame ***
Selected Audio Frequency	192 KHz
Real Audio Frequency	**187.5 KHz ***
Error between Selected and Real	**-2.34 % ***

Clock Parameters:

Clock Source	I2S PLL Clock
Clock Polarity	Low

5.4. LTDC

Display Type: RGB565 (16 bits)

5.4.1. Parameter Settings:

Synchronization for Width:

Horizontal Synchronization Width	**10 ***
Horizontal Back Porch	

	20 *
Active Width	**240 ***
Horizontal Front Porch	**10 ***
HSync Width	9
Accumulated Horizontal Back Porch Width	29
Accumulated Active Width	269
Total Width	279

Synchronization for Height:

Vertical Synchronization Height	**2 ***
Vertical Back Porch	2
Active Height	**320 ***
Vertical Front Porch	**4 ***
VSync Height	1
Accumulated Vertical Back Porch Height	3
Accumulated Active Height	323
Total Height	327

Signal Polarity:

Horizontal Synchronization Polarity	Active Low
Vertical Synchronization Polarity	Active Low
Data Enable Polarity	Active Low
Pixel Clock Polarity	Normal Input

BackGround Color:

Red	0
Green	0
Blue	0

5.4.2. Layer Settings:

BackGround Color:

Layer 0 - Blue	0
Layer 0 - Green	0
Layer 0 - Red	0
Layer 1 - Blue	0
Layer 1 - Green	0
Layer 1 - Red	0

Windows Position:

Layer 0 - Window Horizontal Start	0
Layer 0 - Window Horizontal Stop	**240 ***
Layer 0 - Window Vertical Start	0
Layer 0 - Window Vertical Stop	**160 ***

Layer 1 - Window Horizontal Start	0
Layer 1 - Window Horizontal Stop	**240 ***
Layer 1 - Window Vertical Start	**160 ***
Layer 1 - Window Vertical Stop	**320 ***

Pixel Parameters:

Layer 0 - Pixel Format	RGB565
Layer 1 - Pixel Format	RGB565

Blending:

Layer 0 - Alpha constant for blending	**255 ***
Layer 0 - Default Alpha value	0
Layer 0 - Blending Factor1	**Alpha constant x Pixel Alpha ***
Layer 0 - Blending Factor2	**Alpha constant x Pixel Alpha ***
Layer 1 - Alpha constant for blending	**200 ***
Layer 1 - Default Alpha value	0
Layer 1 - Blending Factor1	**Alpha constant x Pixel Alpha ***
Layer 1 - Blending Factor2	**Alpha constant x Pixel Alpha ***

Frame Buffer:

Layer 0 - Color Frame Buffer Start Adress	0
Layer 0 - Color Frame Buffer Line Length (Image Width)	0
Layer 0 - Color Frame Buffer Number of Lines (Image Height)	0
Layer 1 - Color Frame Buffer Start Adress	0
Layer 1 - Color Frame Buffer Line Length (Image Width)	0
Layer 1 - Color Frame Buffer Number of Lines (Image Height)	0

5.5. RCC

mode: Master Clock Output 2

5.5.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Instruction Cache	Enabled
Prefetch Buffer	Enabled
Data Cache	Enabled
Flash Latency(WS)	5 WS (6 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
TIM Prescaler Selection	Disabled

Power Parameters:

Power Regulatror Voltage Scale	Power Regulator Voltage Scale 1
Power Over Drive	Disabled

5.6. SDIO

Mode: SD 1 bit

5.6.1. Parameter Settings:

SDIO parameters:

SDIOCLK clock divide factor	0

5.7. USART1

Mode: Asynchronous

5.7.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples

5.8. FATFS

mode: SD Card

5.8.1. Set Defines:

Version:

FATFS version	R0.11

Function Parameters:

FS_TINY (Tiny mode)	Disabled
FS_READONLY (Read-only mode)	Disabled
FS_MINIMIZE (Minimization level)	Disabled
USE_STRFUNC (String functions)	Enabled with LF -> CRLF conversion
USE_FIND (Find functions)	Disabled
USE_MKFS (Make filesystem function)	Enabled
USE_FORWARD (Forward function)	Disabled
USE_LABEL (Volume label functions)	Disabled
USE_FASTSEEK (Fast seek function)	Enabled

Locale and Namespace Parameters:

CODE_PAGE (Code page on target)	Latin 1 (Windows)
USE_LFN (Use Long Filename)	Enabled with dynamic working buffer on the HEAP
MAX_LFN (Max Long Filename)	255
LFN_UNICODE (Enable Unicode)	ANSI/OEM
STRF_ENCODE (Character encoding)	UTF-8
FS_RPATH (Relative Path)	Disabled

Physical Drive Parameters:

VOLUMES (Logical drives)	1
MAX_SS (Maximum Sector Size)	512
MIN_SS (Minimum Sector Size)	512
MULTI_PARTITION (Volume partitions feature)	Disabled
USE_TRIM (Erase feature)	Disabled
FS_NOFSINFO (Force full FAT scan)	0

System Parameters:

FS_NORTC (Timestamp feature)	Dynamic timestamp
NORTC_YEAR (Year for timestamp)	2015
NORTC_MON (Month for timestamp)	6
NORTC_MDAY (Day for timestamp)	4
WORD_ACCESS (Platform dependent access option)	Byte access
FS_REENTRANT (Re-Entrancy)	Enabled
FS_TIMEOUT (Timeout ticks)	1000
SYNC_t (O/S sync object)	osSemaphoreId
FS_LOCK (Number of files opened simultaneously)	2

5.8.2. IPs instances:

SDIO/SDMMC:

SDIO instance	SDIO1

5.9. FREERTOS

mode: Enabled

5.9.1. Config parameters:

Versions:

CMSIS-RTOS version	1.02
FreeRTOS version	8.2.1

Kernel settings:

USE_PREEMPTION	Enabled
CPU_CLOCK_HZ	SystemCoreClock
TICK_RATE_HZ	1000
MAX_PRIORITIES	7
MINIMAL_STACK_SIZE	128
MAX_TASK_NAME_LEN	16
USE_16_BIT_TICKS	Disabled
IDLE_SHOULD_YIELD	Enabled
USE_MUTEXES	Enabled
USE_RECURSIVE_MUTEXES	Enabled
USE_COUNTING_SEMAPHORES	Enabled
QUEUE_REGISTRY_SIZE	8
USE_APPLICATION_TASK_TAG	Disabled
TOTAL_HEAP_SIZE	15360
Memory Management scheme	heap_4
USE_ALTERNATIVE_API	Disabled
ENABLE_BACKWARD_COMPATIBILITY	Enabled
USE_PORT_OPTIMISED_TASK_SELECTION	Disabled
USE_TICKLESS_IDLE	Disabled

Hook function related definitions:

USE_IDLE_HOOK	Disabled
USE_TICK_HOOK	Disabled
USE_MALLOC_FAILED_HOOK	Disabled
CHECK_FOR_STACK_OVERFLOW	Disabled

Run time and task stats gathering related definitions:

USE_TRACE_FACILITY	Enabled
GENERATE_RUN_TIME_STATS	Disabled

Co-routine related definitions:

USE_CO_ROUTINES	Disabled
MAX_CO_ROUTINE_PRIORITIES	2

Software timer definitions:

USE_TIMERS	Disabled
TIMER_TASK_PRIORITY	2
TIMER_QUEUE_LENGTH	10

Interrupt nesting behaviour configuration:

LIBRARY_LOWEST_INTERRUPT_PRIORITY	15
LIBRARY_MAX_SYSCALL_INTERRUPT_PRIORITY	5

5.9.2. Include parameters:

Include definitions:

vTaskPrioritySet	Enabled
uxTaskPriorityGet	Enabled
vTaskDelete	Enabled
vTaskCleanUpResources	Disabled
vTaskSuspend	Enabled
vTaskDelayUntil	Disabled
vTaskDelay	Enabled
xTaskGetSchedulerState	Enabled
xTaskResumeFromISR	Enabled
xQueueGetMutexHolder	Disabled
xSemaphoreGetMutexHolder	Disabled
pcTaskGetTaskName	Disabled
uxTaskGetStackHighWaterMark	Disabled
xTaskGetCurrentTaskHandle	Disabled
eTaskGetState	Disabled
xEventGroupSetBitFromISR	Disabled
xTimerPendFunctionCall	Disabled

*** User modified value**

6. System Configuration

6.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
FMC	PF0	FMC_A0	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PF1	FMC_A1	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PF2	FMC_A2	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PF3	FMC_A3	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PF4	FMC_A4	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PF5	FMC_A5	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PC0	FMC_SDNWE	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PC2	FMC_SDNE0	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PC3	FMC_SDCKE0	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PF11	FMC_SDNRAS	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PF12	FMC_A6	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PF13	FMC_A7	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PF14	FMC_A8	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PF15	FMC_A9	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PG0	FMC_A10	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PG1	FMC_A11	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PE7	FMC_D4	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PE8	FMC_D5	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PE9	FMC_D6	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PE10	FMC_D7	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PE11	FMC_D8	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PE12	FMC_D9	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PE13	FMC_D10	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PE14	FMC_D11	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PE15	FMC_D12	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PD8	FMC_D13	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PD9	FMC_D14	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PD10	FMC_D15	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PD14	FMC_D0	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PD15	FMC_D1	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PG4	FMC_BA0	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PG5	FMC_BA1	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PG8	FMC_SDCLK	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PD0	FMC_D2	Alternate Function Push Pull	No pull-up and no pull-down	High	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PD1	FMC_D3	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PG15	FMC_SDNCAS	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PE0	FMC_NBL0	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PE1	FMC_NBL1	Alternate Function Push Pull	No pull-up and no pull-down	High	
I2C1	PB6	I2C1_SCL	Alternate Function Open Drain	Pull-up	**High ***	
	PB7	I2C1_SDA	Alternate Function Open Drain	Pull-up	**High ***	
I2S2	PB12	I2S2_WS	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB13	I2S2_CK	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB15	I2S2_SD	Alternate Function Push Pull	No pull-up and no pull-down	Low	
LTDC	PF10	LTDC_DE	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA3	LTDC_B5	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA4	LTDC_VSYNC	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA6	LTDC_G2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB0	LTDC_R3	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB1	LTDC_R6	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB10	LTDC_G4	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB11	LTDC_G5	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PG6	LTDC_R7	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PG7	LTDC_CLK	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PC6	LTDC_HSYNC	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PC7	LTDC_G6	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA11	LTDC_R4	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA12	LTDC_R5	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PD3	LTDC_G7	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PG10	LTDC_G3	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PG11	LTDC_B3	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PG12	LTDC_B4	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB8	LTDC_B6	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB9	LTDC_B7	Alternate Function Push Pull	No pull-up and no pull-down	Low	
RCC	PC9	RCC_MCO_2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
SDIO	PC8	SDIO_D0	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PC12	SDIO_CK	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PD2	SDIO_CMD	Alternate Function Push Pull	No pull-up and no pull-down	High	
USART1	PA9	USART1_TX	Alternate Function Push Pull	Pull-up	**High ***	
	PA10	USART1_RX	Alternate Function Push Pull	Pull-up	**High ***	
GPIO	PE2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PE3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PE4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PE5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PE6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PC13	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PC14/OSC32_IN	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PC15/OSC32_OUT	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	

6.2. DMA configuration

DMA request	Stream	Direction	Priority
SPI2_TX	DMA1_Stream4	Memory To Peripheral	**High ***

SPI2_TX: DMA1_Stream4 DMA request Settings:

Mode:	Normal
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	**Half Word ***
Memory Data Width:	**Half Word ***

6.3. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority
System tick timer	true	0	0
DMA1 stream4 global interrupt	true	5	0
SPI2 global interrupt	true	5	0
USART1 global interrupt	true	5	0
FMC global interrupt	true	5	0
Non maskable interrupt	unused		
Memory management fault	unused		
Pre-fetch fault, memory access fault	unused		
Undefined instruction or illegal state	unused		
Debug monitor	unused		
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
I2C1 event interrupt	unused		
I2C1 error interrupt	unused		
SDIO global interrupt	unused		
LTDC global interrupt	unused		
LTDC global error interrupt	unused		

*** User modified value**

7. Power Plugin report

7.1. Microcontroller Selection

Series	STM32F4
Line	STM32F429/439
MCU	STM32F429ZITx
Datasheet	024030_Rev5

7.2. Parameter Selection

Temperature	25
Vdd	null

8. Software Project

8.1. Project Settings

Name	Value
Project Name	SLSF4
Project Folder	C:\Users\Terry\Desktop\SLSF4\SLSF4
Toolchain / IDE	MDK-ARM V4
Firmware Package Name and Version	STM32Cube FW_F4 V1.9.0

8.2. Code Generation Settings

Name	Value
STM32Cube Firmware Library Package	Copy all used libraries into the project folder
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No