1. **标识符：**

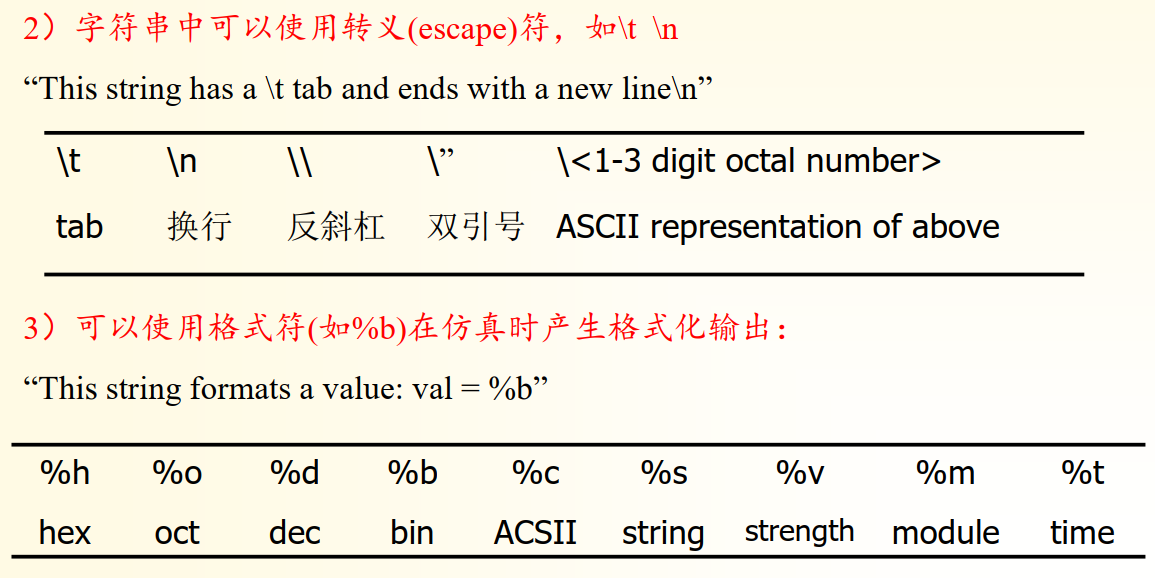
区分大小写，必须以字母（a-z，A-Z）或（\_）开头，后面可以是字母、数字、或\_。

1. **科学表示法：**

<尾数><e或E><指数>，表示：尾数X。

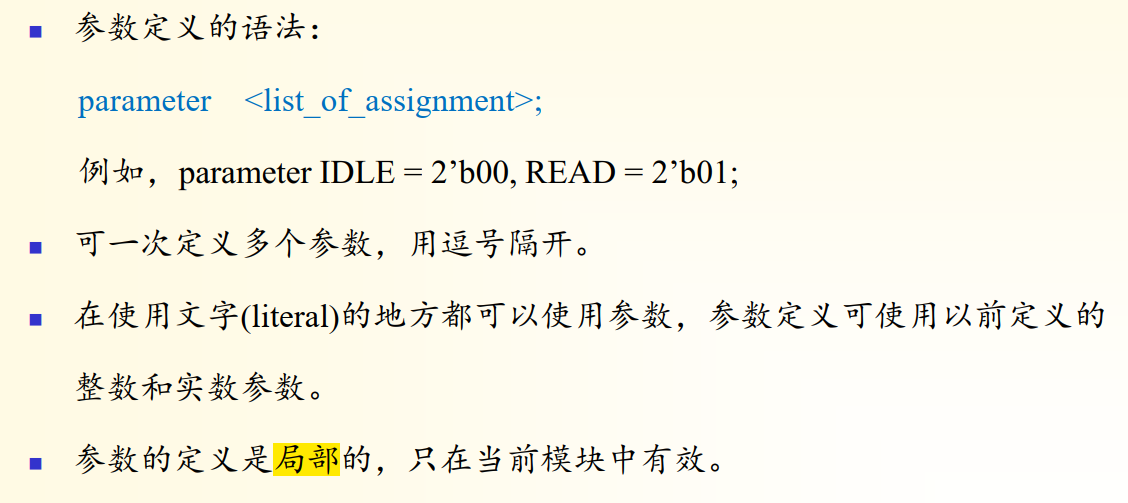
1. **字符串：**

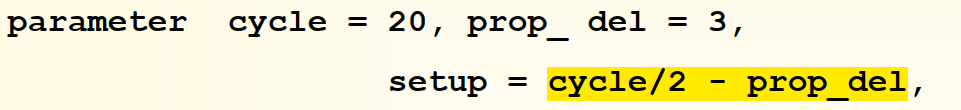
在一行中用双引号括起来，不能跨行。可以使用转义符。



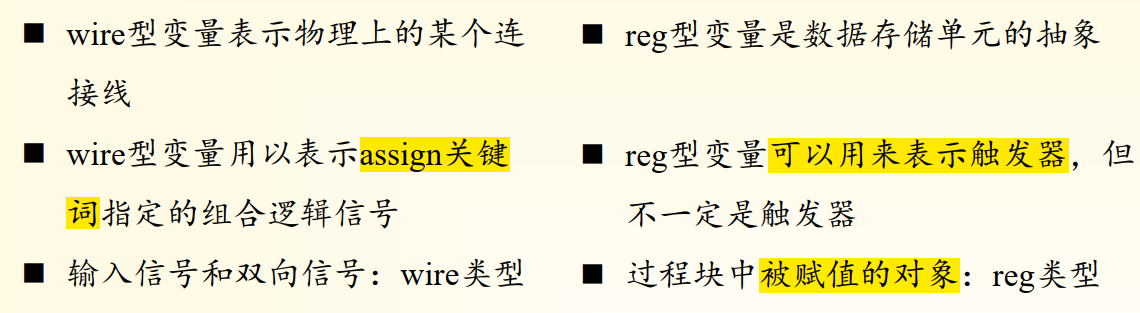
1. **Parameter：**

·声明一个可变常量，常用于定义延时及宽度变量。

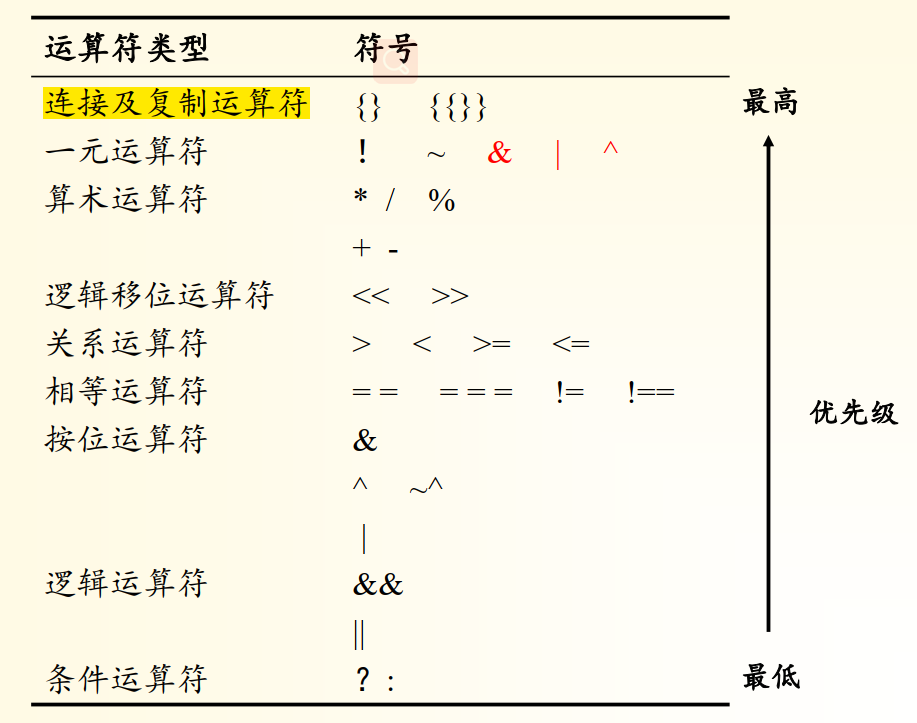




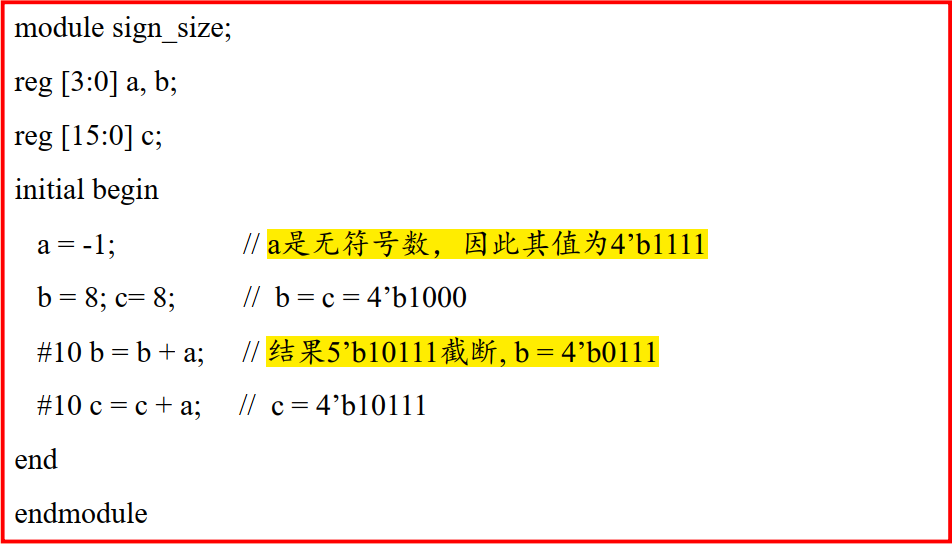
1. **Wire & reg：**



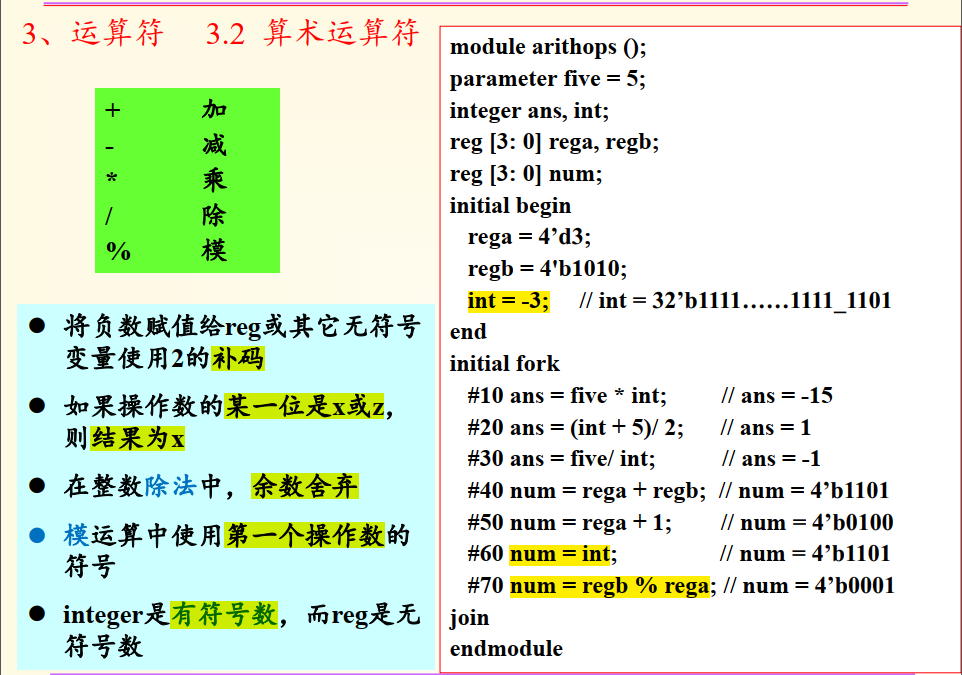
1. **运算符优先级：**







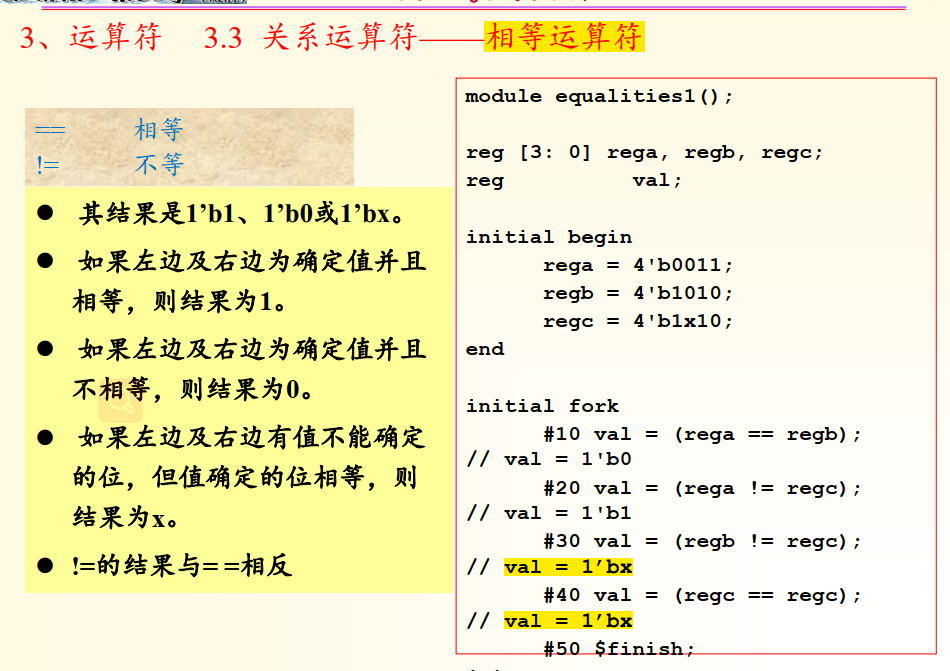
1. **算数运算符：**



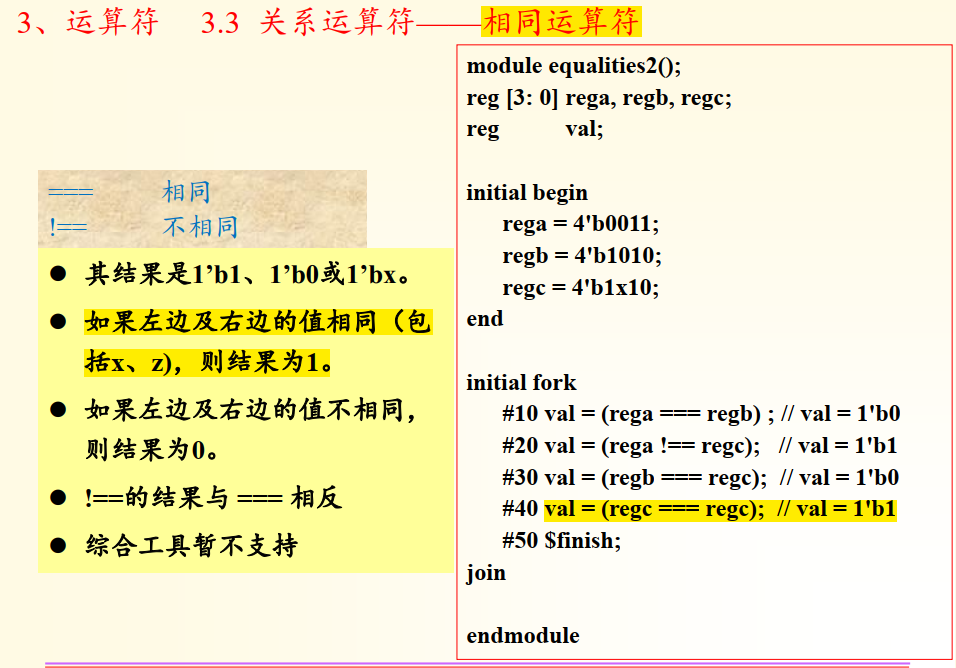
1. **关系运算符：**

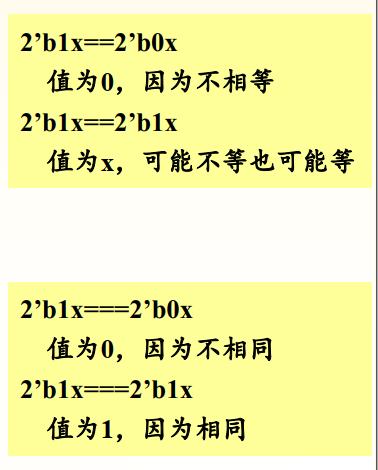
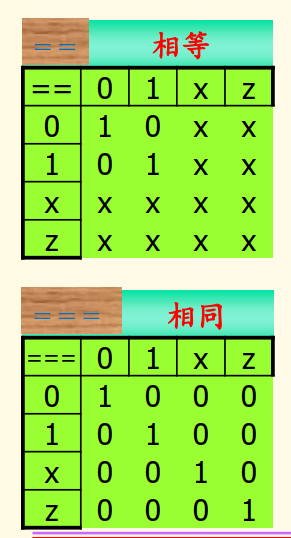


1. **相等运算符：**

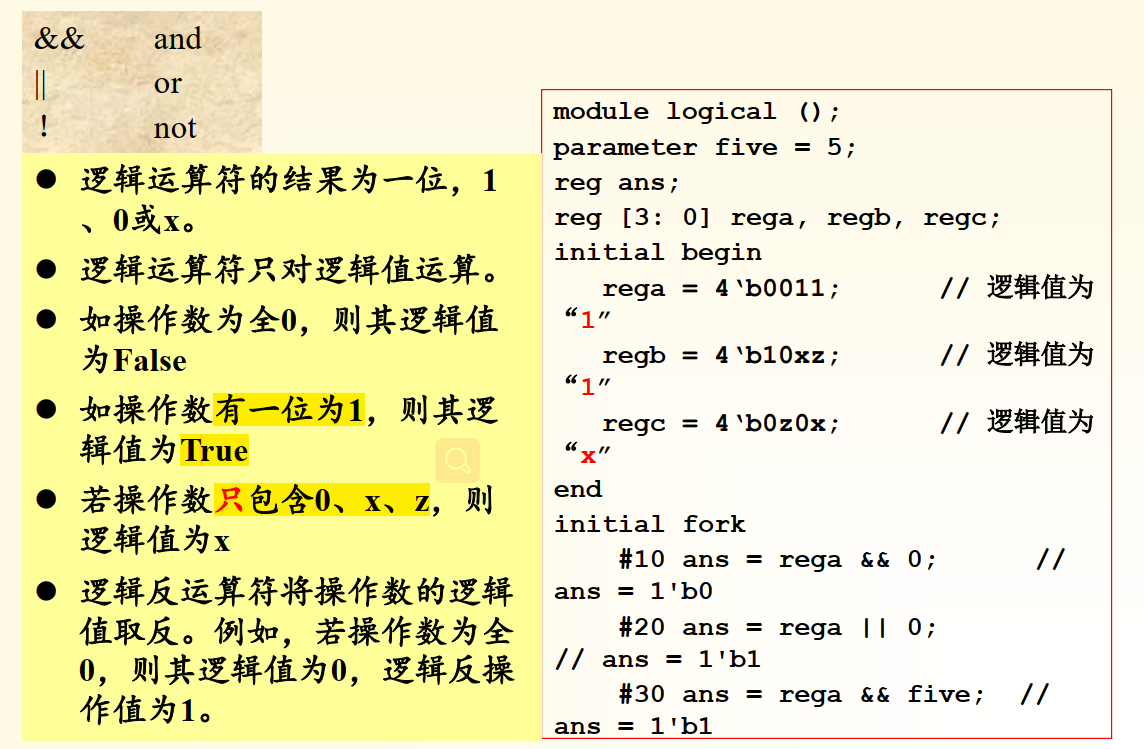


1. **相同运算符：**





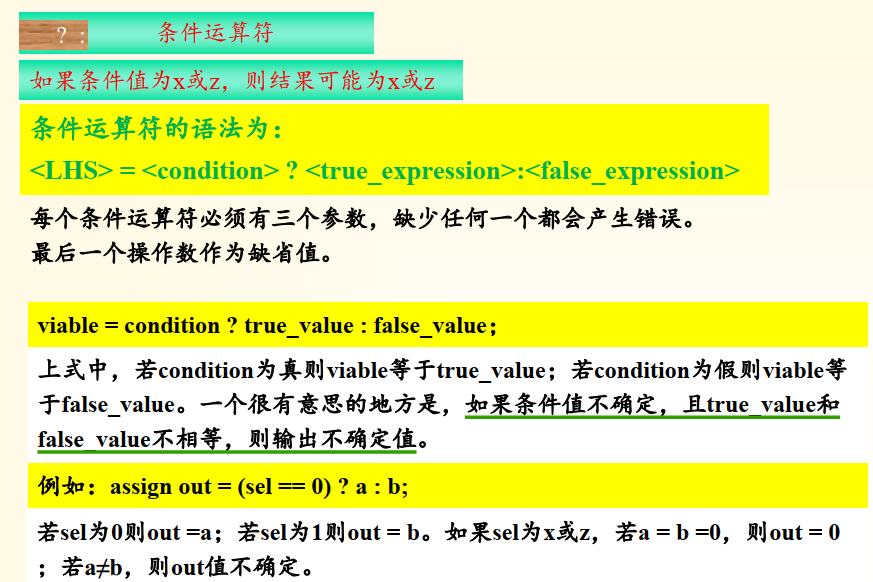
1. **逻辑操作符（注意和位运算符区分）**



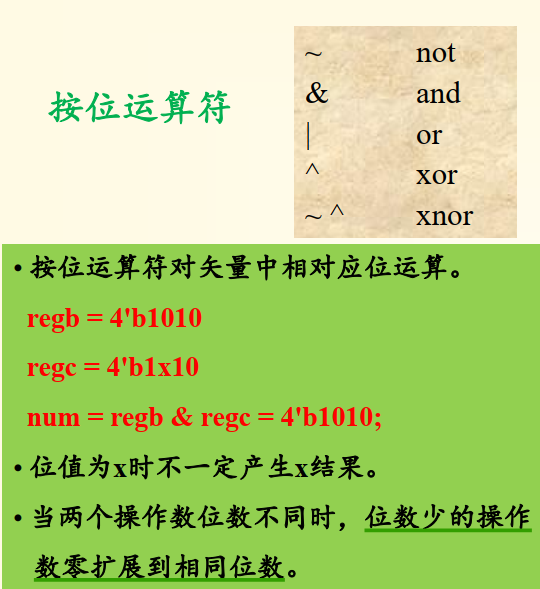
1. **移位运算符**



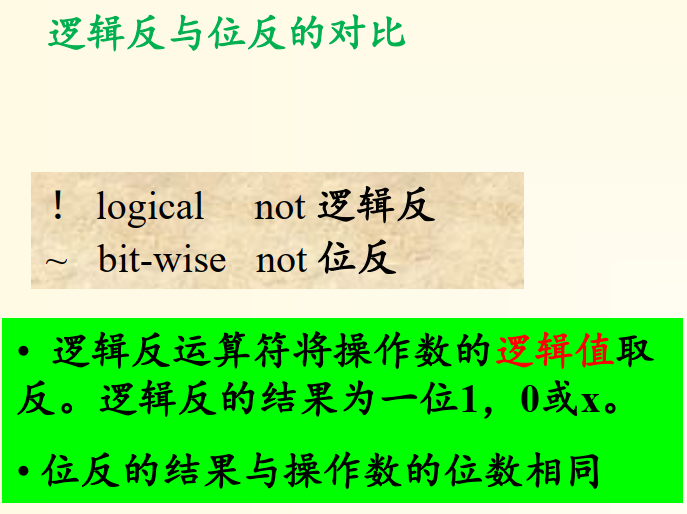
1. **条件运算符**



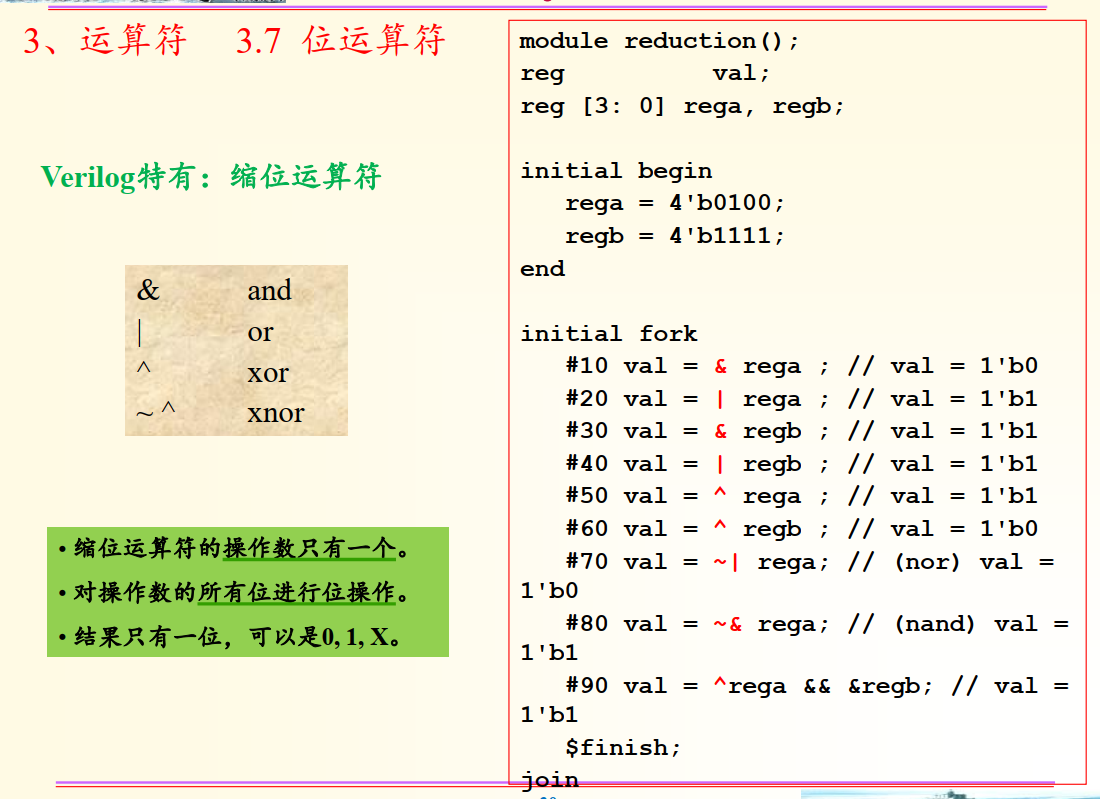
1. **位运算符**



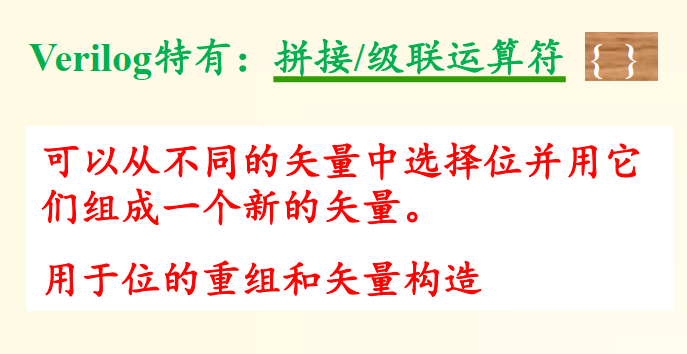
1. **逻辑反与位反**

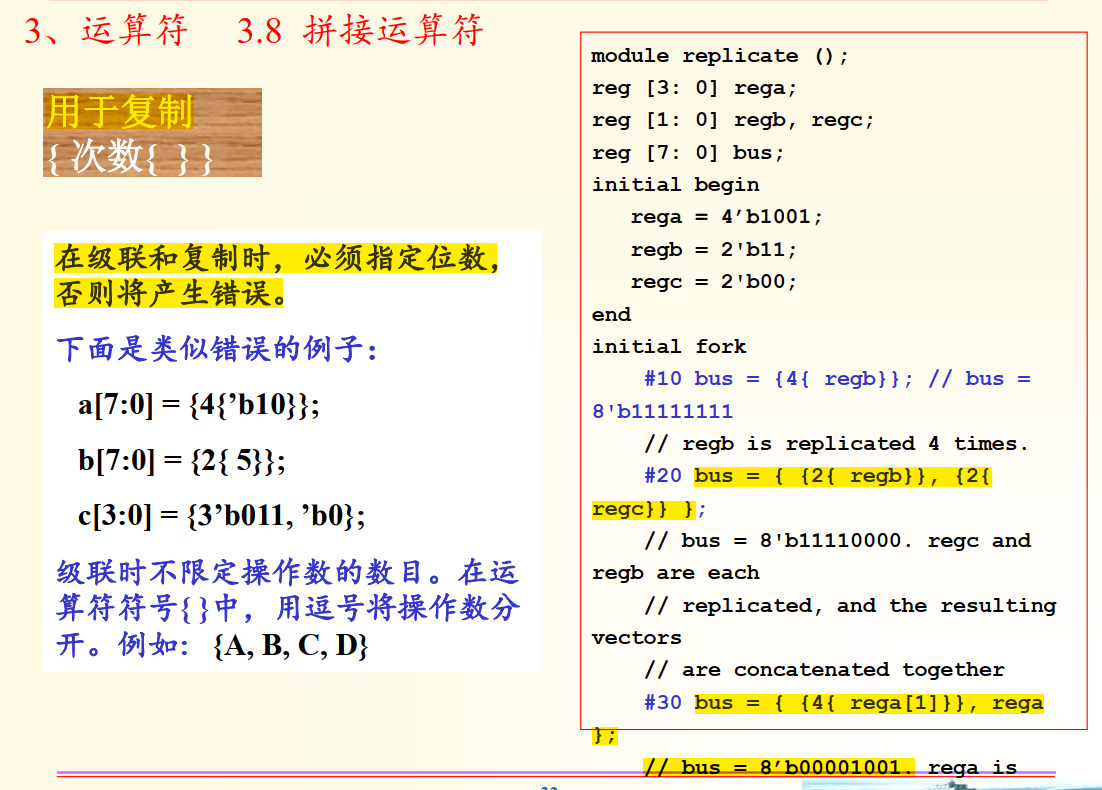


1. **缩位运算符**

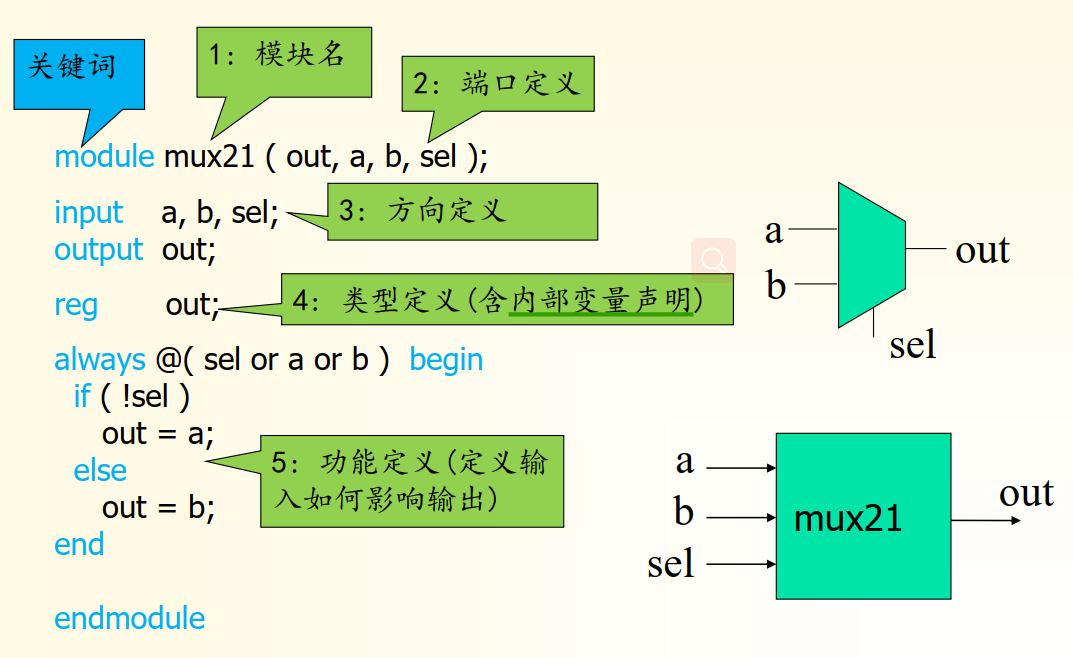


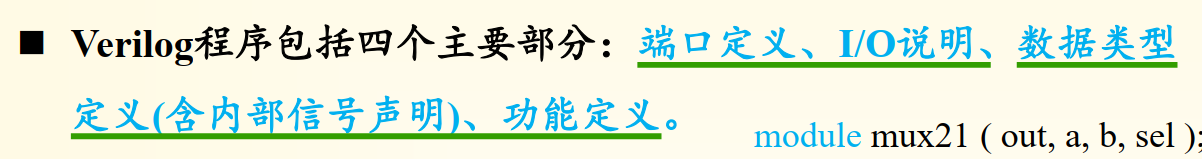
1. **拼接运算符**

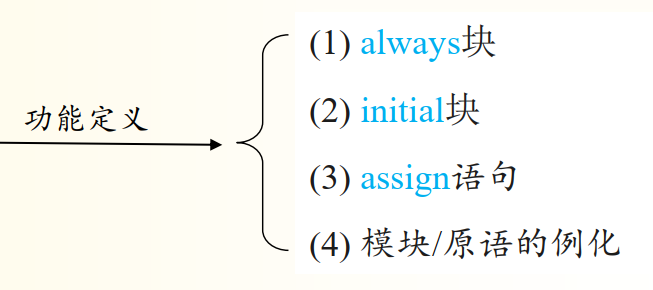




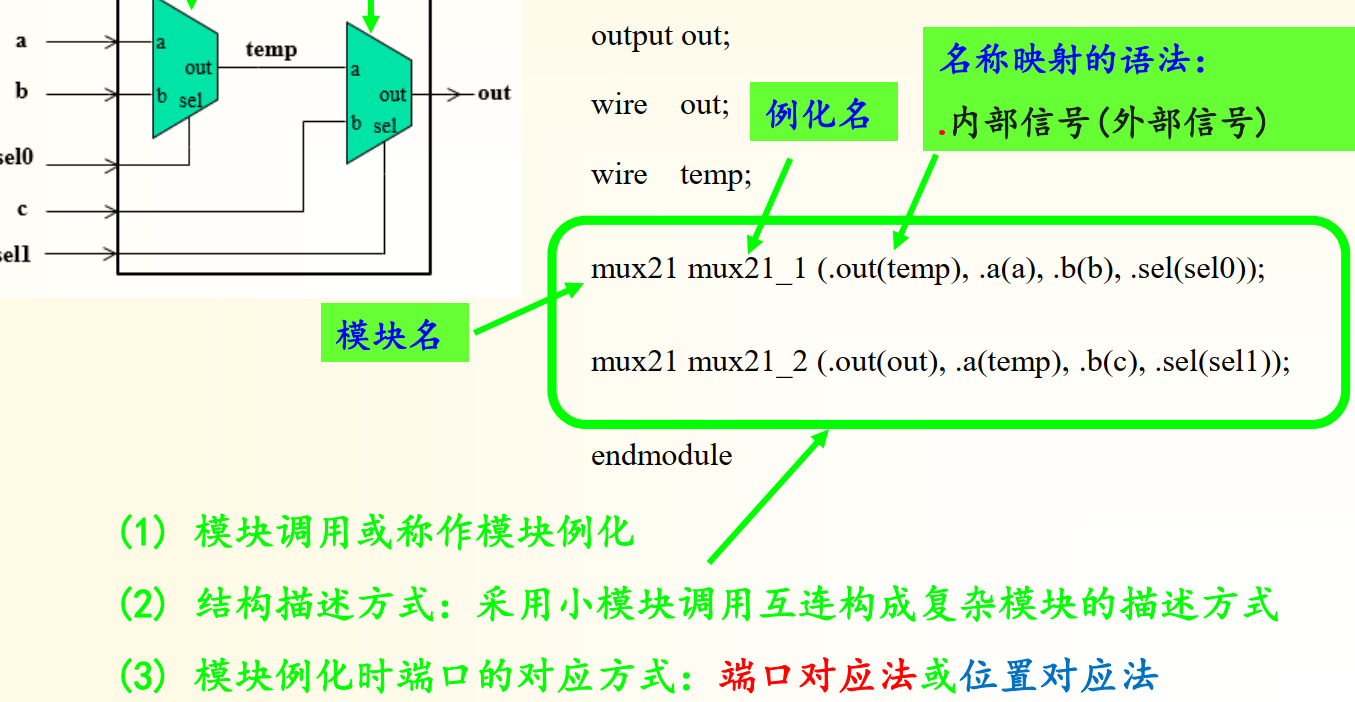
1. **模块化**

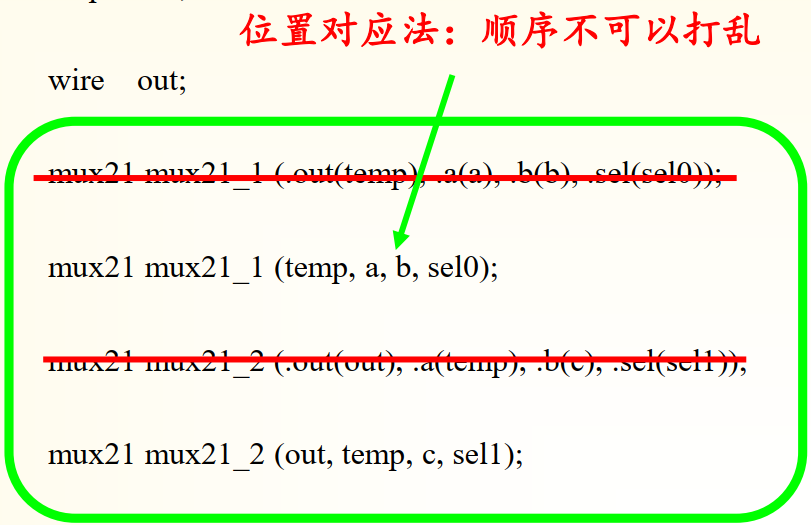




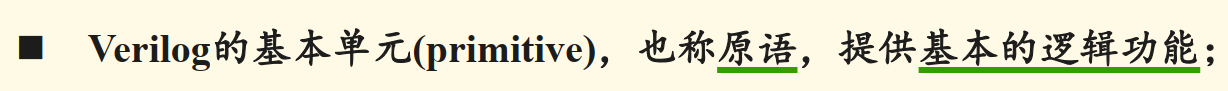


1. **模块例化**





1. **原语**

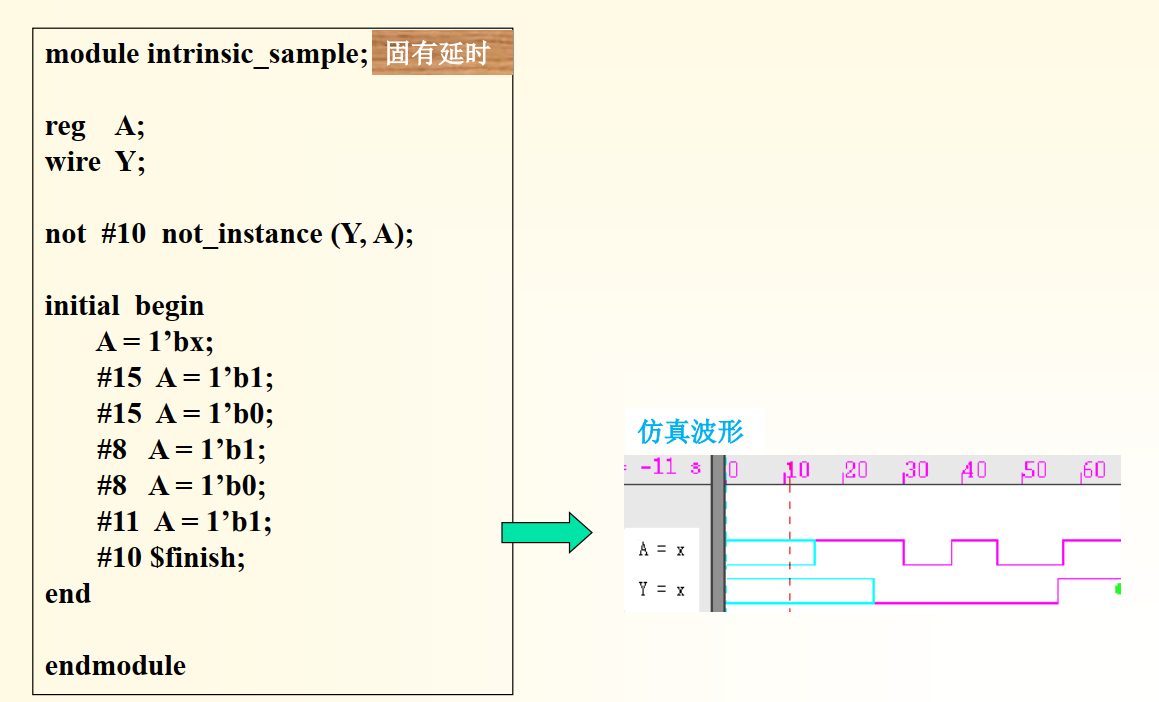


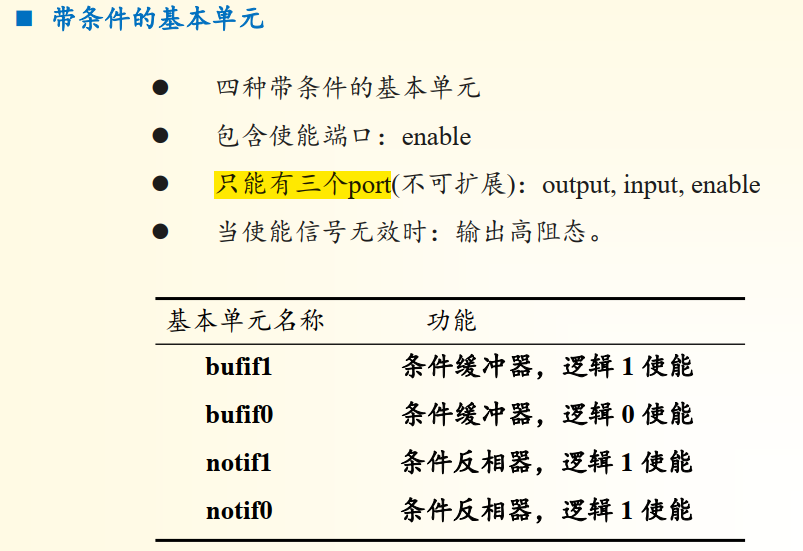


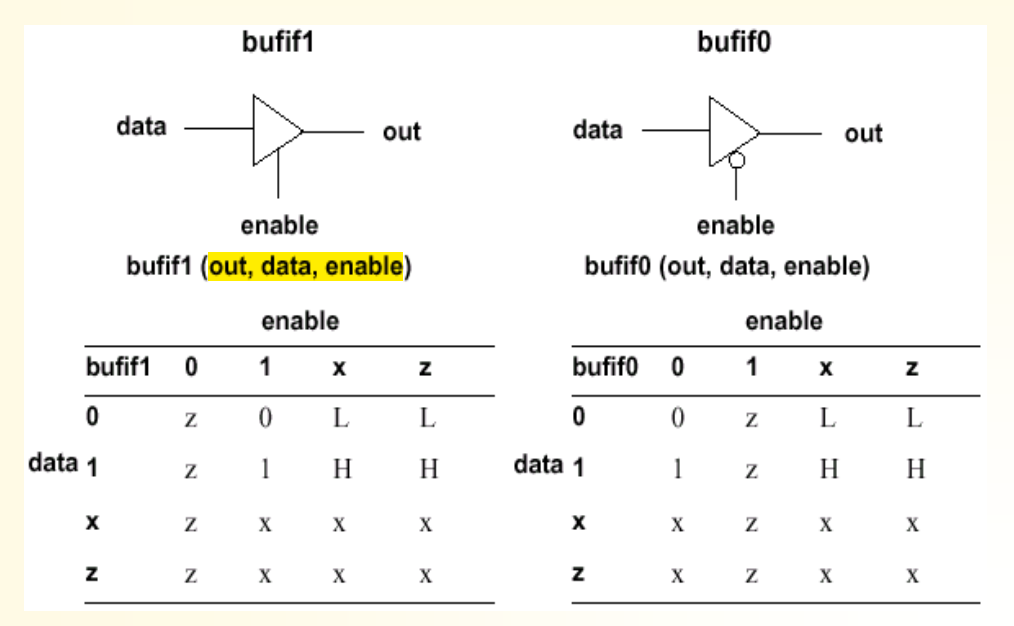


1. **基本单元的调用**

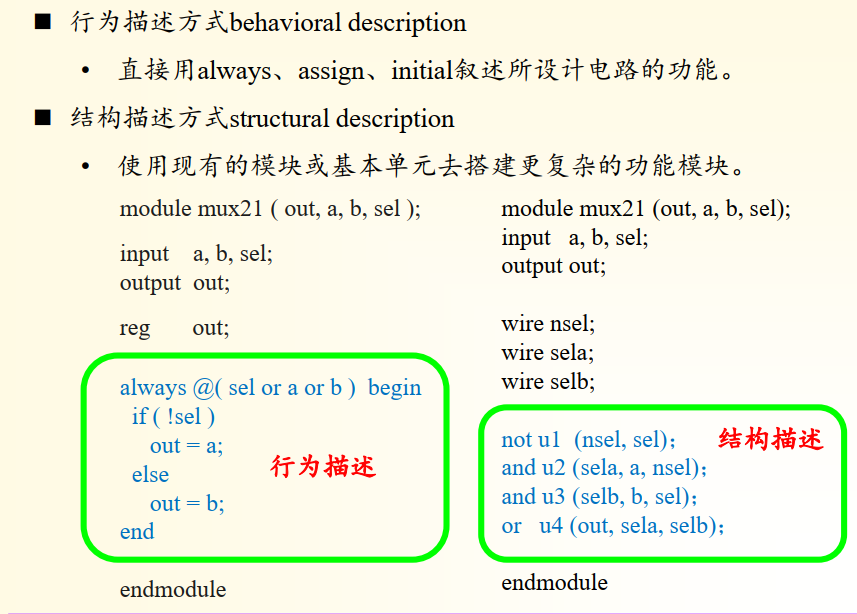




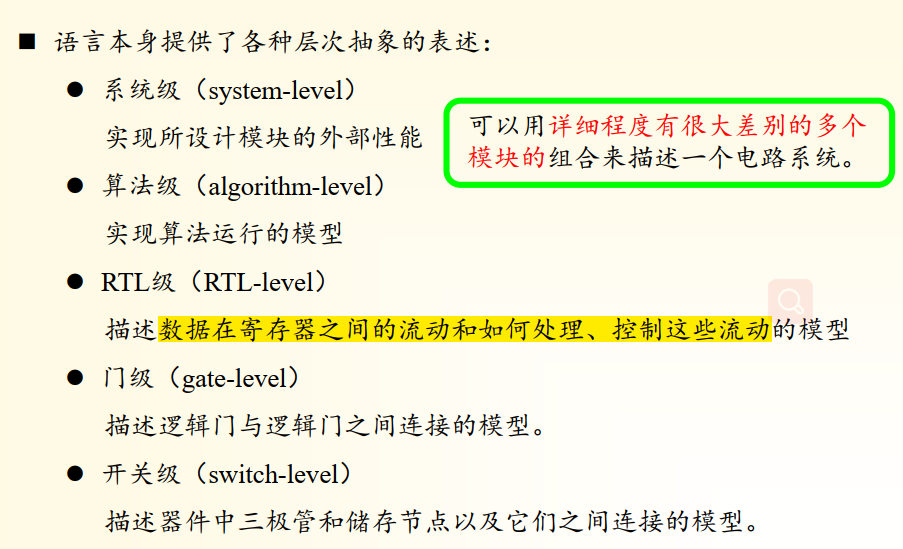




1. **建模的两种描述方式**

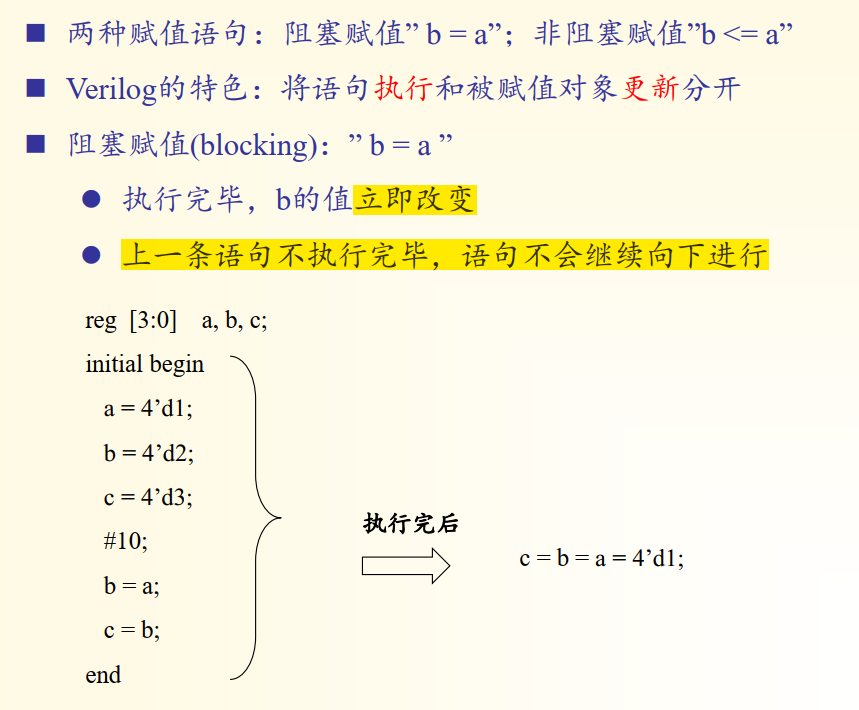


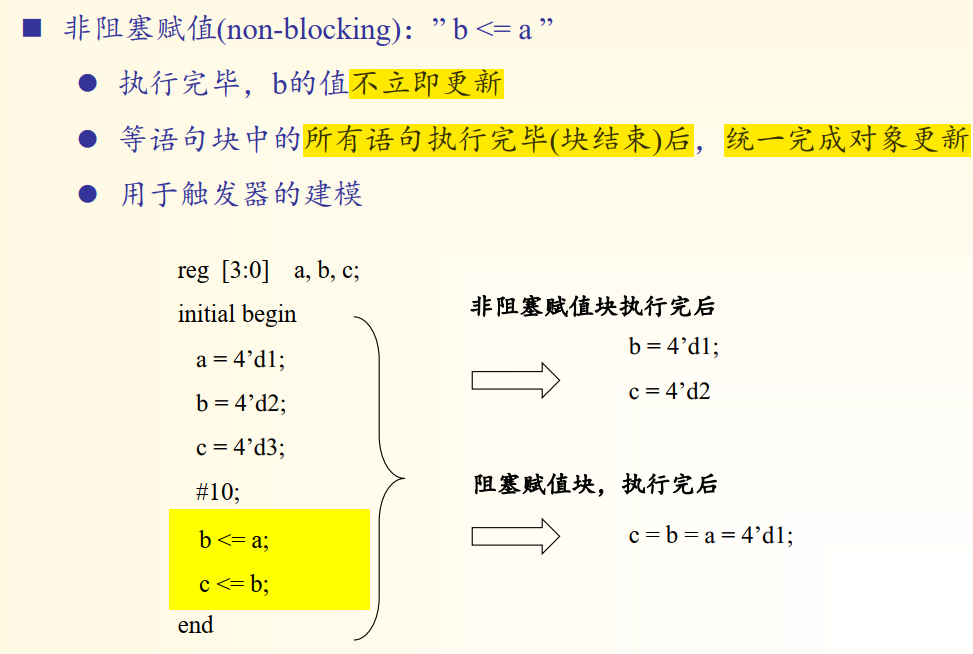
1. **Verilog的抽象级别：**

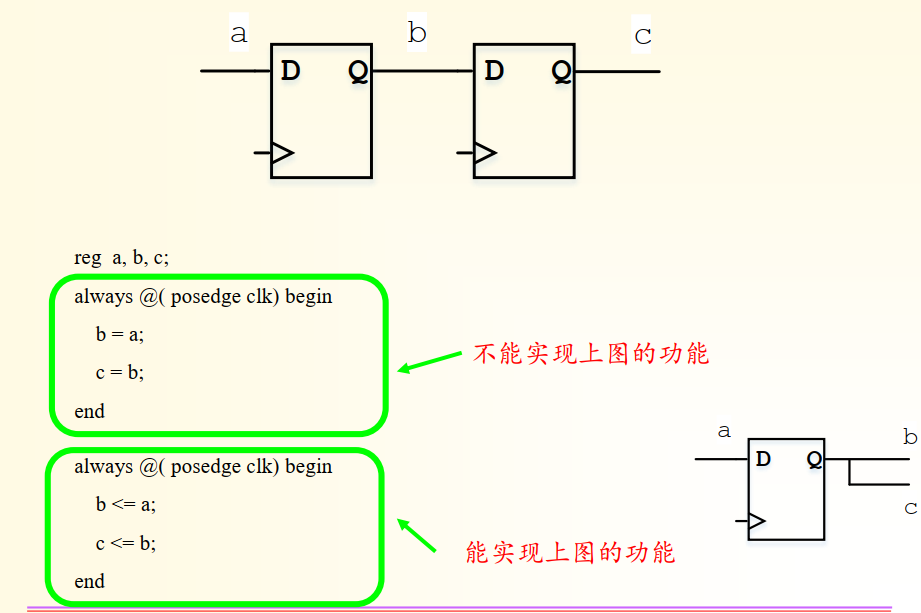


可以用/\*.....\*/和//...对Verilog HDL程序的任何部分作注释

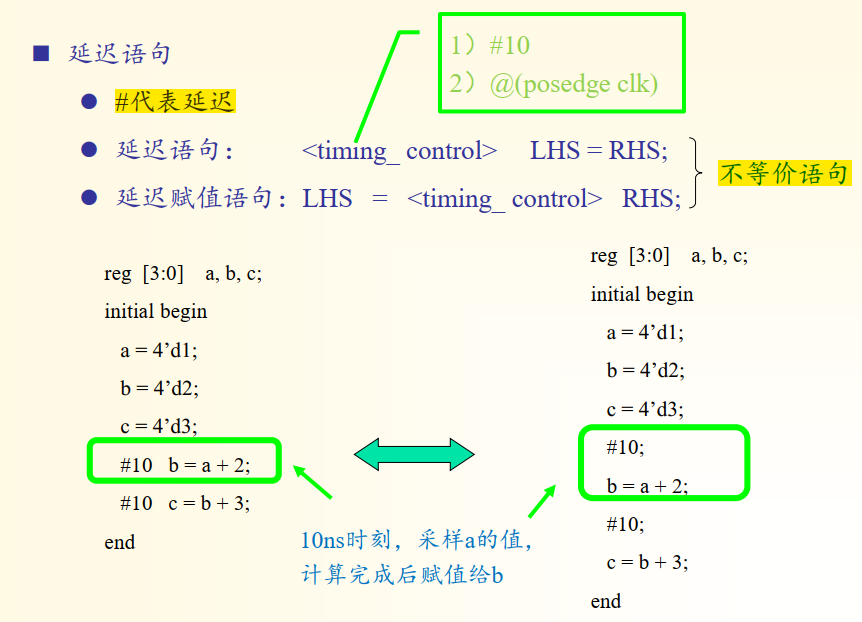
1. **赋值语句**

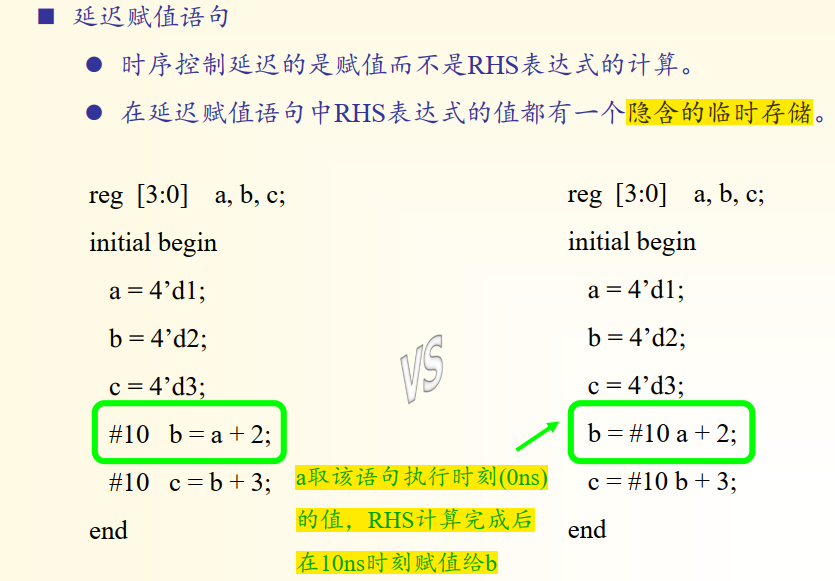


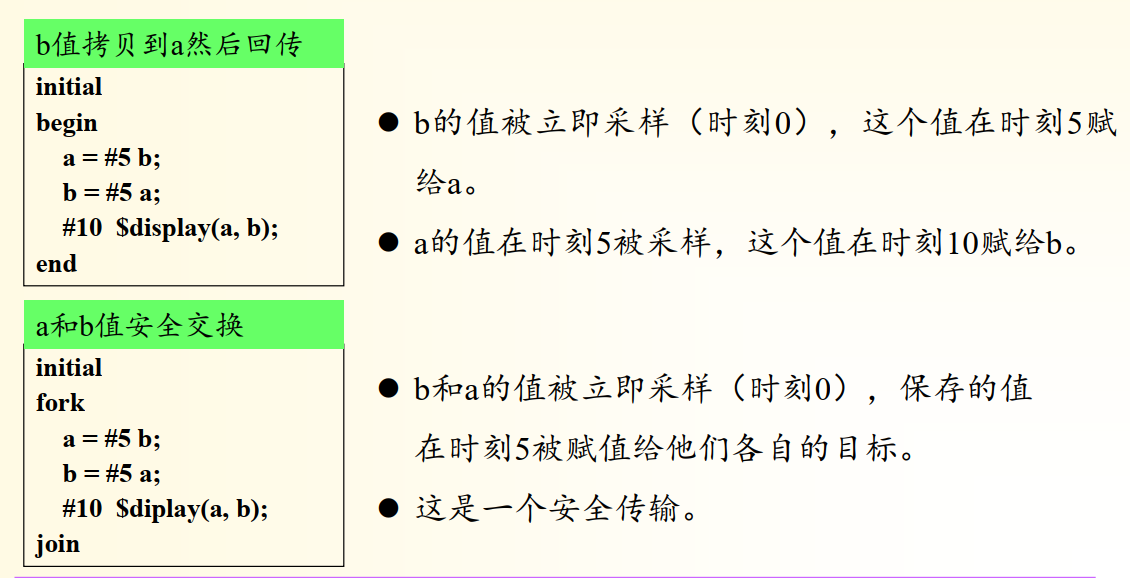




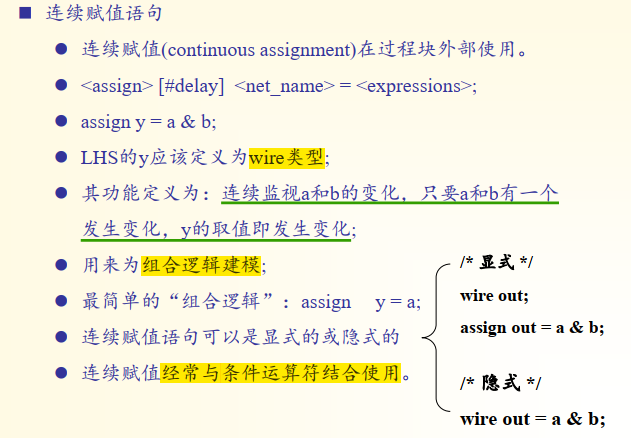
1. **延迟语句**



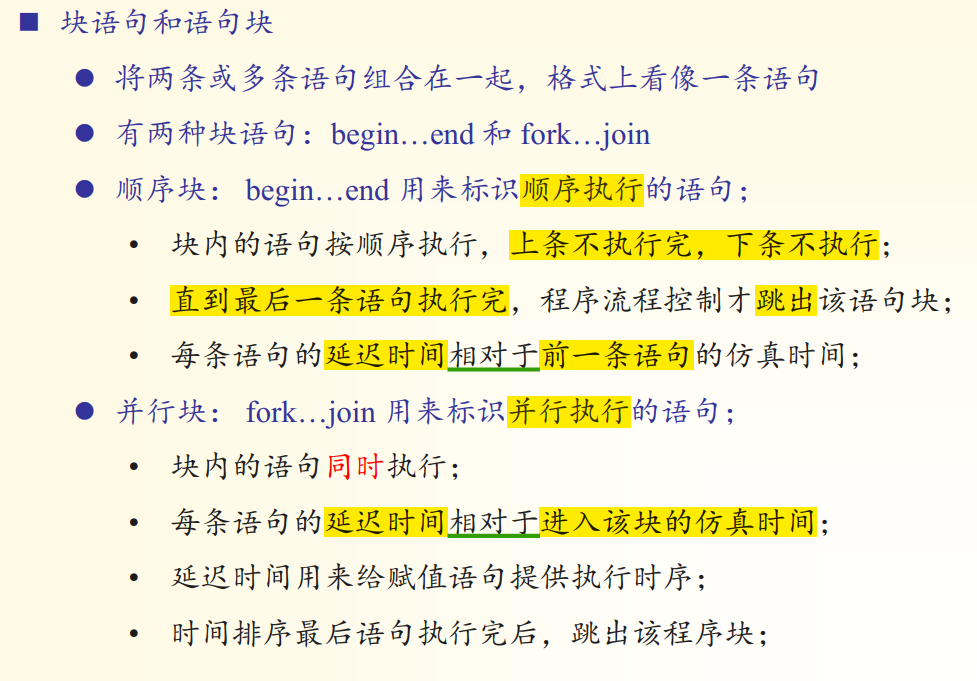


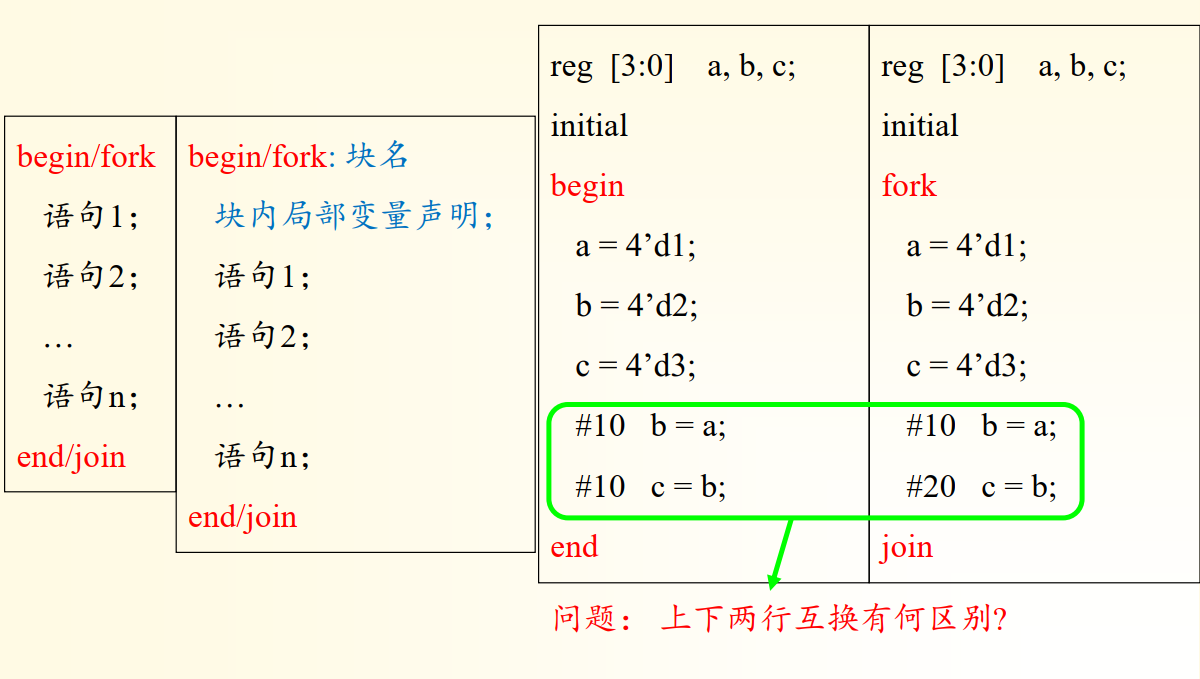


1. **连续赋值语句**

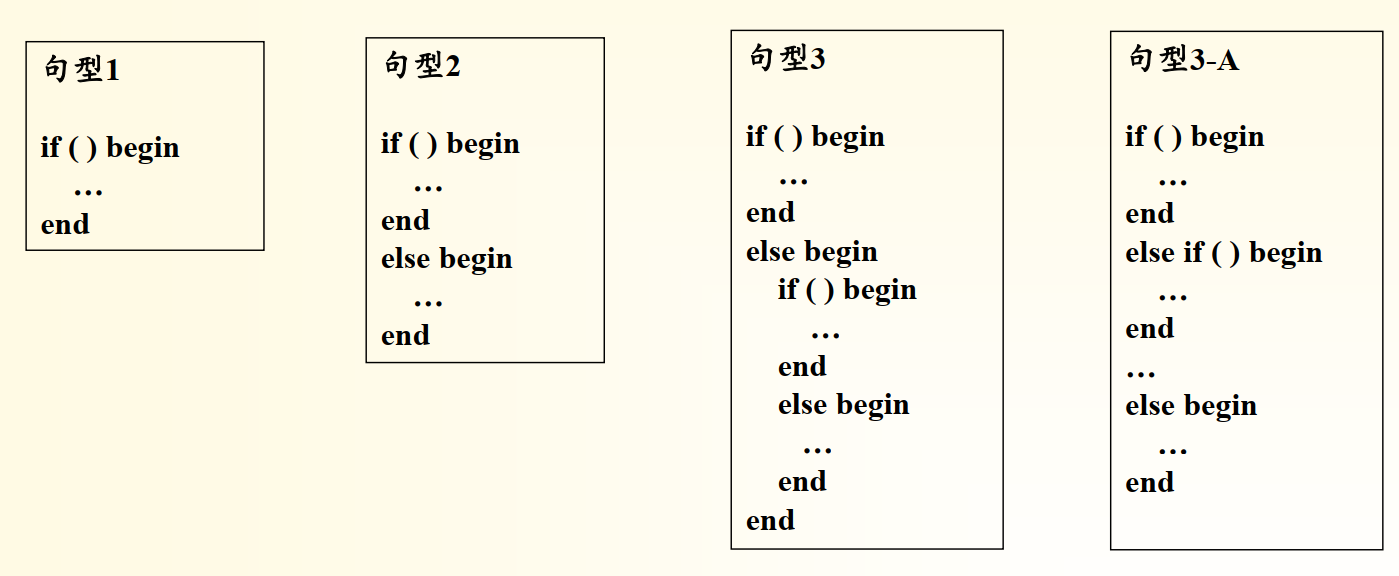


1. **块语句**

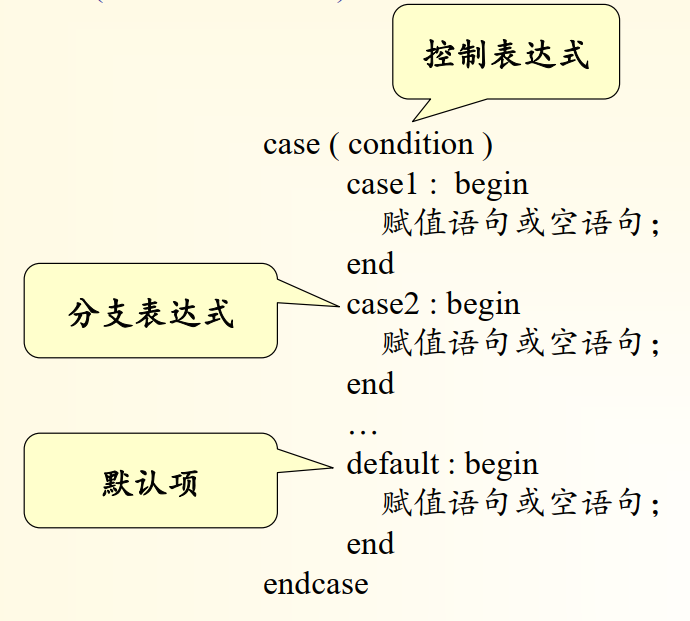


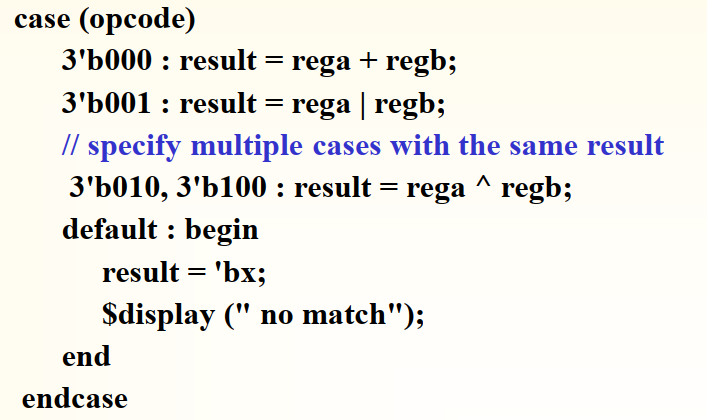


1. **条件语句**



1. **Case语句**





1. **循环语句**

