



深圳职业技术学院
SHENZHEN POLYTECHNIC

国家级精品课程

IC版图设计



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项目任务



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1. Linux基础和Cadence初识

■ Linux基本命令练习：

练习使用下列基本的Linux指令，并且自行学习其他书上提到的Linux指令。

ls ll ls -a

cp

mv

rm

man

mkdir

cd

pwd



- chmod
- top
- kill
- su
- telnet
- ftp
- mount
- tar



■ vi文本编辑器：

练习使用最基础的vi指令，并且参考教材
进行其他指令的练习

- 1.进入vi的办法
- 2.命令模式，指令模式，编辑模式



■ 3. 基本命令：

上下左右

(、}、{

n+

n-

0 (数字零)

ndd

nyy

p



■ 编辑模式：

i

r



■ 指令模式：

: /

/yufei

:w

:wq

:q

:q!

:%s/p1/p2/g

:set nu



- Cadence 软件的启动和基本界面
- library manager的使用



- 2个初始化文件
- 库路径文件
- 技术库文件
- 显示设定文件



- 基本图形编辑
- 热键使用
- 格点吸附的设定



任务

- 1. 在自己班级的目录下建立一个以自己学号命名的文件夹
- 2. 在该文件夹下面建立4个子文件夹，包括happy, introduction, classmate, study
- 3. 在introduction文件夹下面建立一个myself.v的文件，并且写不少于2行的自我介绍，并且把其复制100遍
- 4. 使用U盘mount sd*1 /mnt/usbdisk 的命令，找到U盘，并且拷贝不少于5个同学的自我介绍，并且将其该名字为：“同学名.int”文件，并且放置于classmate文件夹下面
- 5. 在happy下建立两个文件夹，命名为music和movie并且每个文件夹写入不少于3个文件的自己喜欢的音乐以及电影的介绍
- 6. 在study文件夹下建立本学期所有课程名字命名的文件夹，包括本门课程IClauot
- 7. 在IClauot下拷贝cadence的example中初始化文件，技术文件以及显示文件，建立一个版图库，并在该库里建立一个cell，在这个版图cell中画出自己的中文名字。
- 8. 最后把所有的文件夹打包为tar文件。



■ 任务检查方式：

在老师指定的文件夹下面建立指定的目录和文本，提交以后，可以直接找教师检查登记,要记录时间先后顺序。



2. 反相器版图设计与验证

■ 首先建立工作路径：

Shell No. 2 - Konsole

Session Edit View Bookmarks Settings Help

[work@linux_sever ~]\$ ls
CDS.log core.4490 core.4492 core.4496 Desktop
core.4488 core.4491 core.4493 core.4497 libManager.log

[work@linux_sever ~]\$ cd yufei

[work@linux_sever ~/yufei]\$ ls
book_example lab led_driver_half

[work@linux_sever ~/yufei]\$ cd lab/

[work@linux_sever lab]\$ ls
lab1 lab1.tar lab2 lab2.tar

[work@linux_sever lab]\$ ls
lab1 lab1.tar lab2 lab2.tar

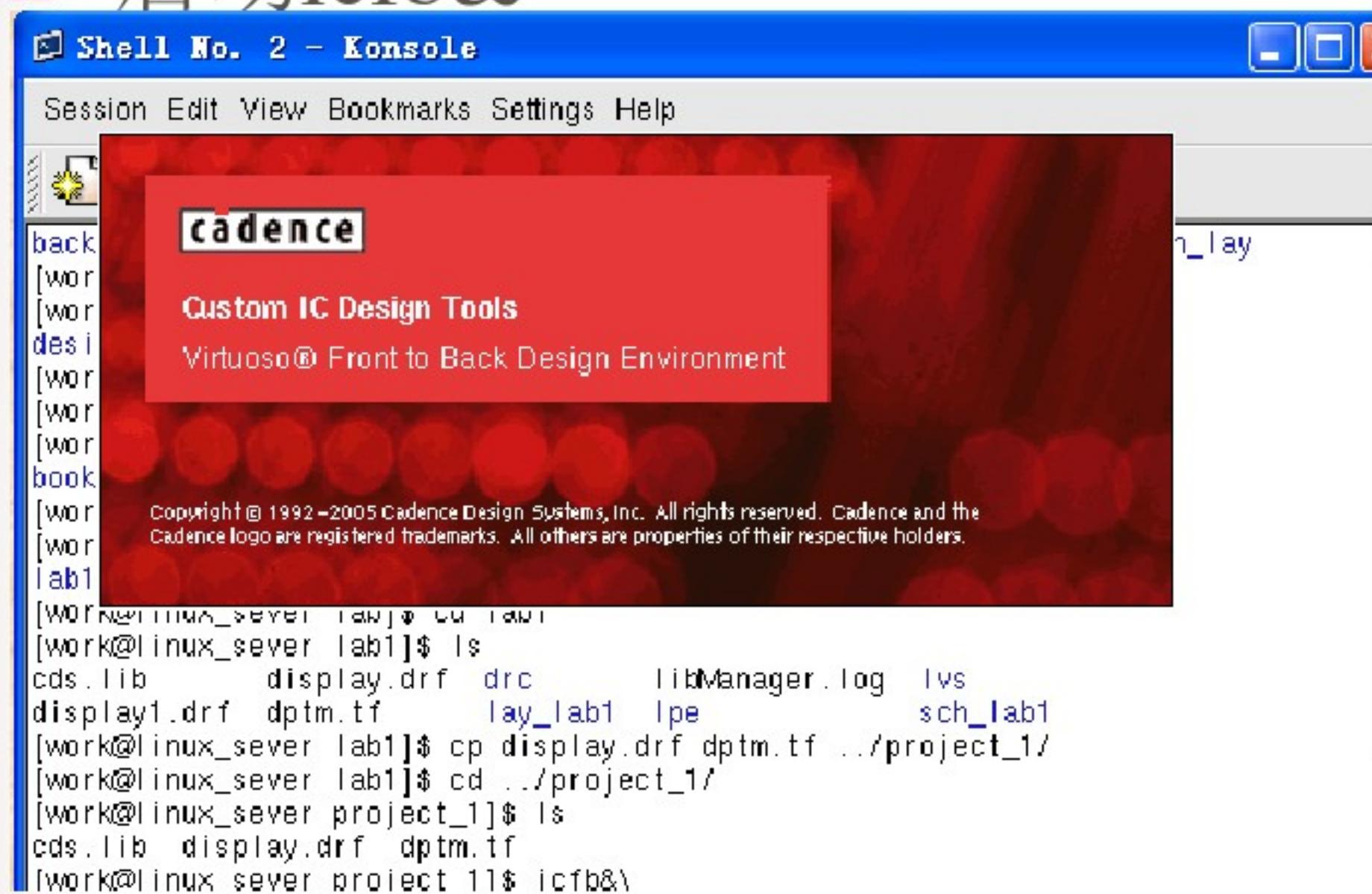
[work@linux_sever lab]\$ mkdir project_1



- cp .cdsenv .cdsinit cds.lib 到你工作的路径下，主要目的是设定快捷键，以及基本的库路径
- 拷贝tf文件以及display.drf文件，确定工艺库以及显示属性
- 5个文件齐全以后，可以开始版图工作

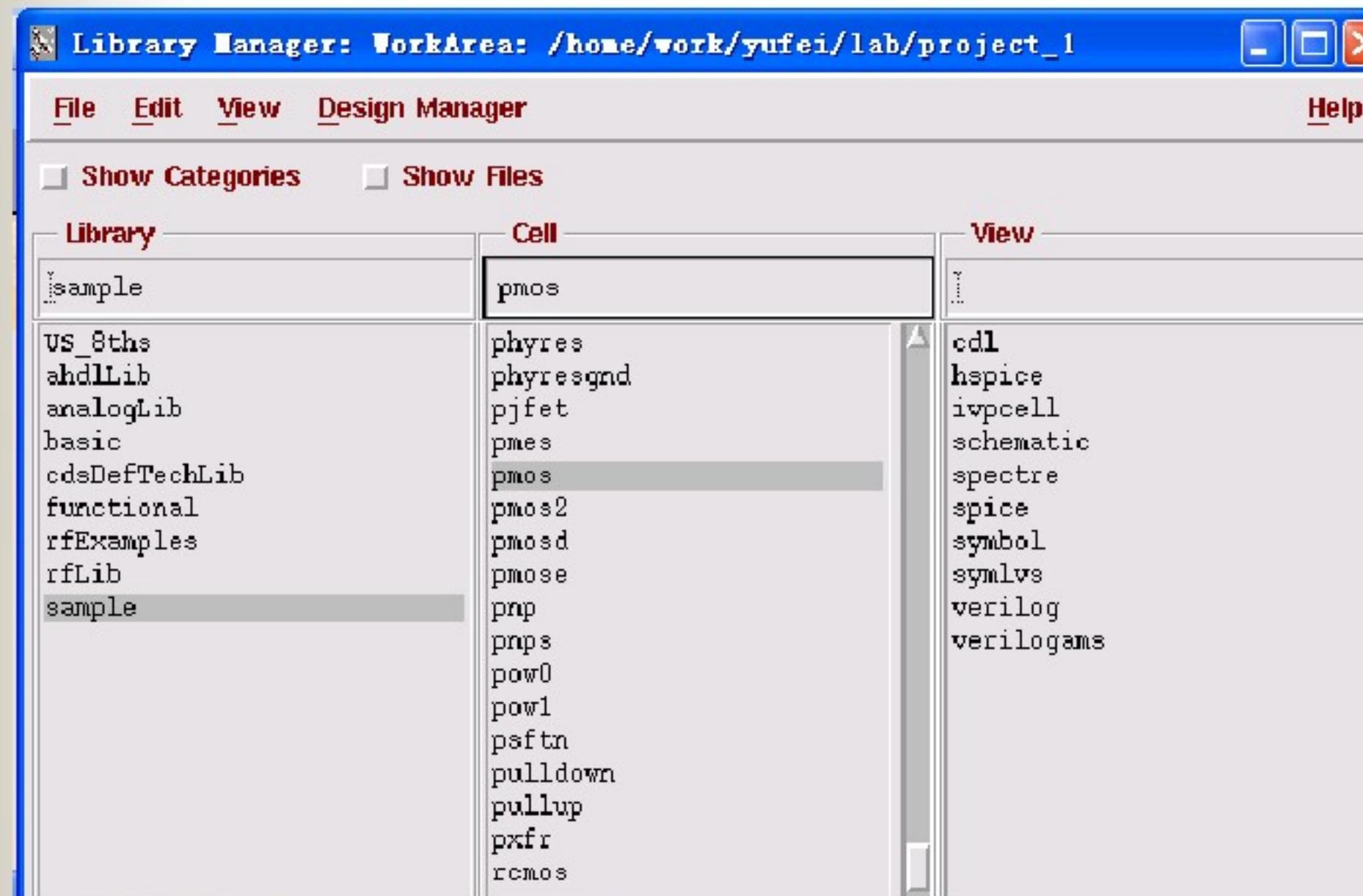


■ 启动icfb&



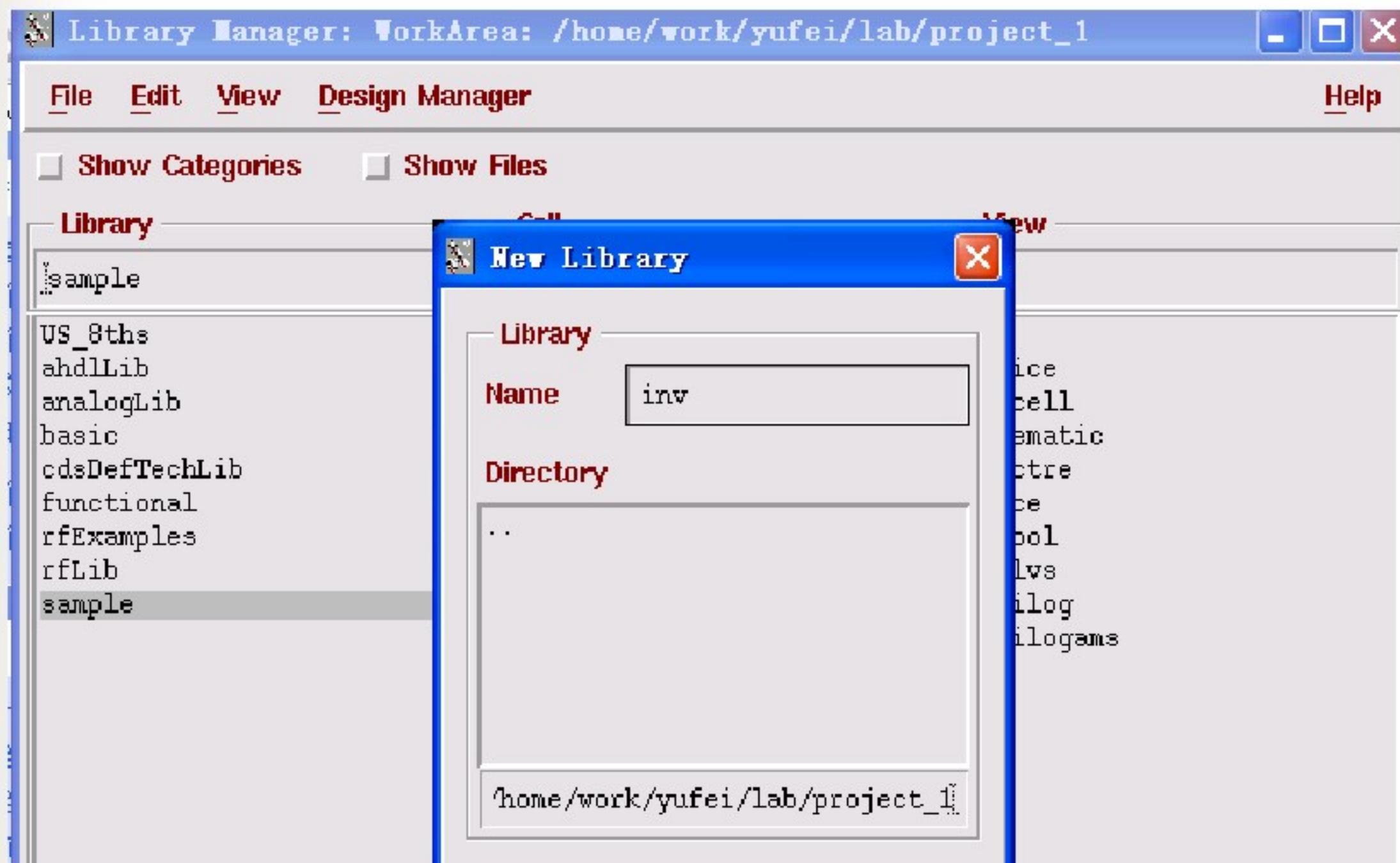


■ 启动library manager



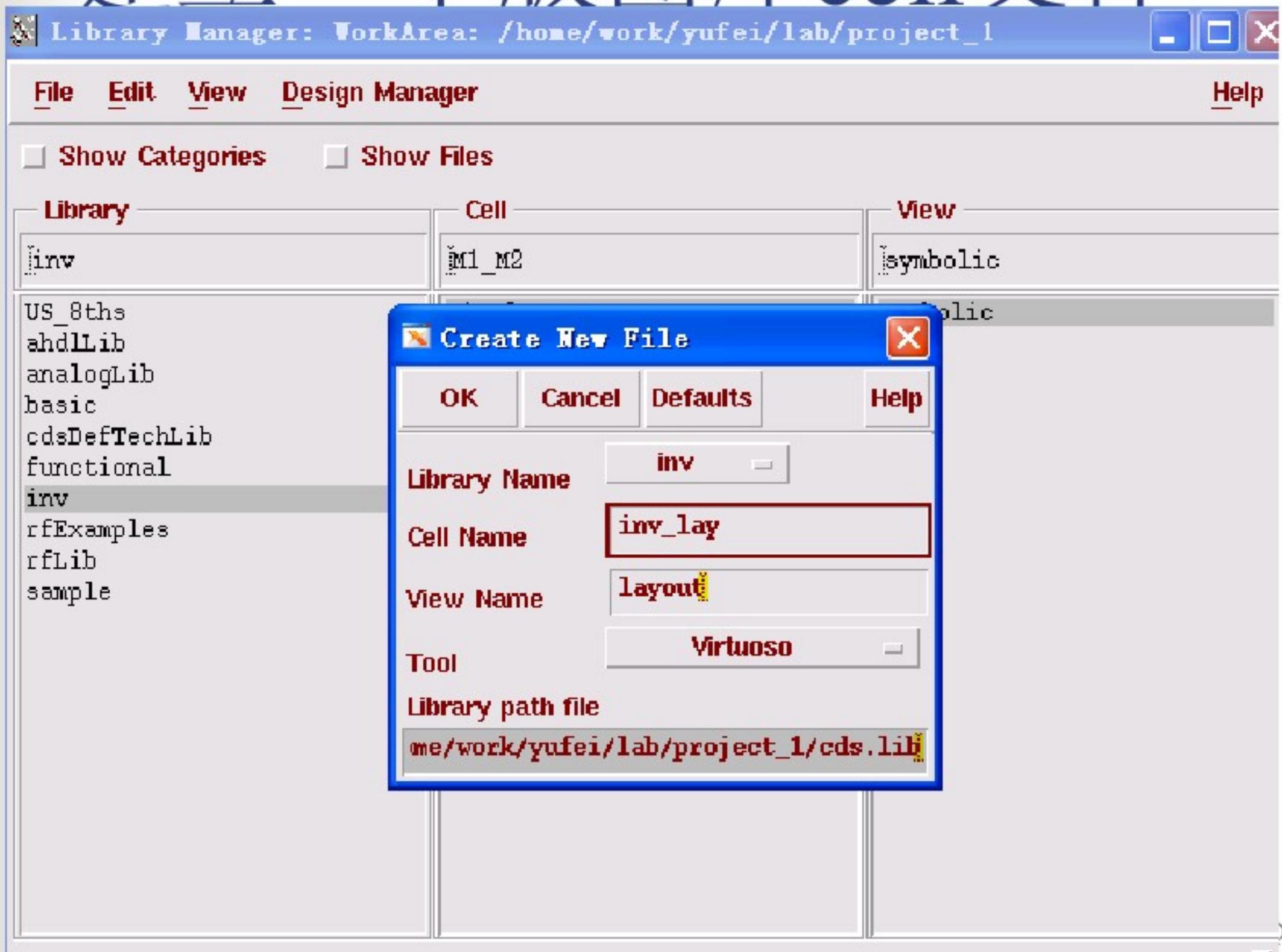


新建一个库，编译tf文件





建立一个版图库cell文件





设定格点性质

X: -4.5

Y: 10.0

(F) Select: 0

DRD: OFF

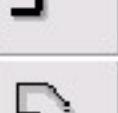
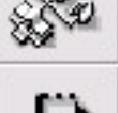
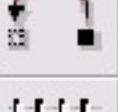
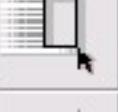
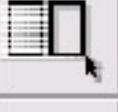
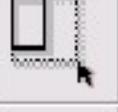
dX: 0.0

dY: 10.5

Dist: 10.50

On

Tools Design Window Create Edit Verify Connectivity Options Routing



Display Options

OK

Cancel

Defaults

Apply

Help

Display Controls

- Open to Stop Level Nets
- Axes Access Edges
- Instance Origins Instance Pins
- EIP Surround Array Icons
- Pin Names Label Origins
- Dot Pins Dynamic Hilight
- Use True BBox Net Expressions
- Cross Cursor Stretch Handles

Grid Controls

Type none dots linesMinor Spacing Major Spacing X Snap Spacing Y Snap Spacing

Filter

Size Style

Path Display

Borders and Centerlines

Show Name Of

 instance master

Array Display

Display Levels

 FullStart BorderStop Source

Snap Modes

Create Edit

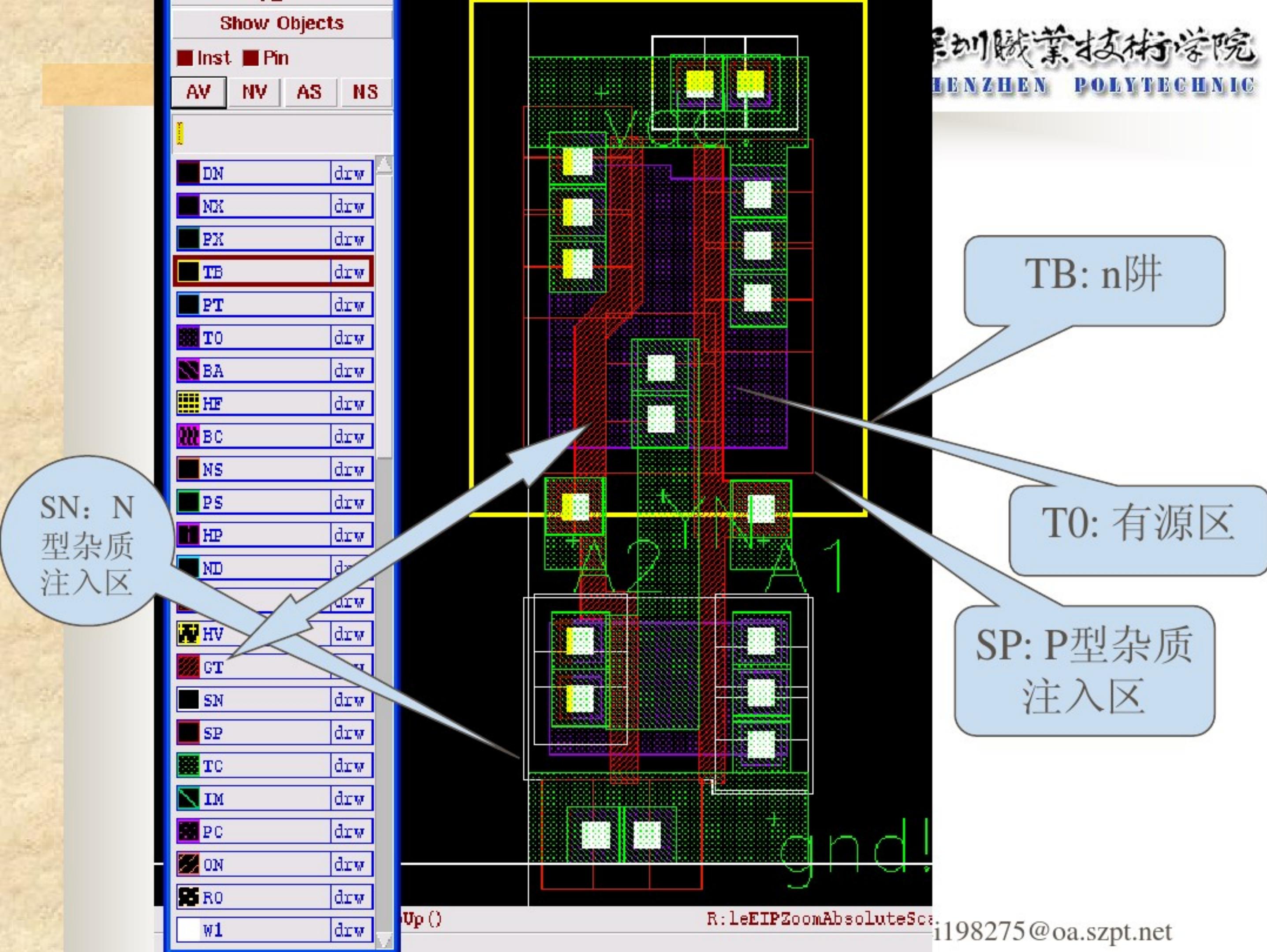


画出反相器的版图

- 1. 熟悉design rule
- 2. 了解图层含义和属性



No.	Mask	Layout Layer	Digitized Area	Digitized Tone	Description
1	TO	Active	Active	Dark	Diffusion & Channel area
2	③	N-well			P channel device substrate
3	PT		N-well	Dark	P-well & N-channel stop implant
4	BC		Generation ①	Dark	Normal threshold voltage NMOS & PMOS channel implant (include ROM region).
5	③	LVN ②			Low threshold voltage NMOS channel implant.
6	PS	LVP ②	LVP	Clear	Low threshold voltage PMOS channel implant.
7	ND	VDN ②	VDN	Clear	Depletion NMOS channel implant.
8	PD	VDP②	VDP	Clear	Depletion PMOS channel implant.
9	BA	P-base	P-base	Clear	Vertical NPN (N+/P-base/Nwell) P-base implant
10	GT	Poly1	Poly1	Dark	Gate of the N & P channel and bottom plate of inter-poly
11	SN		P+	Dark	N-channel source and drain
12	SP	P+	P+	Clear	P-channel source and drain
13	RO	ROM ②	ROM	Clear	ROM code implant
14	IM	High Res ②	High Res	Dark	Poly2 High ohm resistor protection area when poly2 doping .
15	PC	Poly2	Poly2	Dark	Poly2
16	W1	Contact	Contact	Clear	Contact to Metal 1
17	A1	Metall	Metall	Dark	Metal1 interconnect
18	W2	Vial	Vial	Clear	Metal2 to metall contact
19	A2/T2 ④	Metal2	Metal2	Dark	Metal2 interconnect
20	W3	Via2	Via2	Clear	Metal3 to metal2 contact
21	A3/T3 ④	Metal3	Metal3	Dark	Metal3 interconnect
22	CP	Pad	Pad	Clear	Bond pad opening



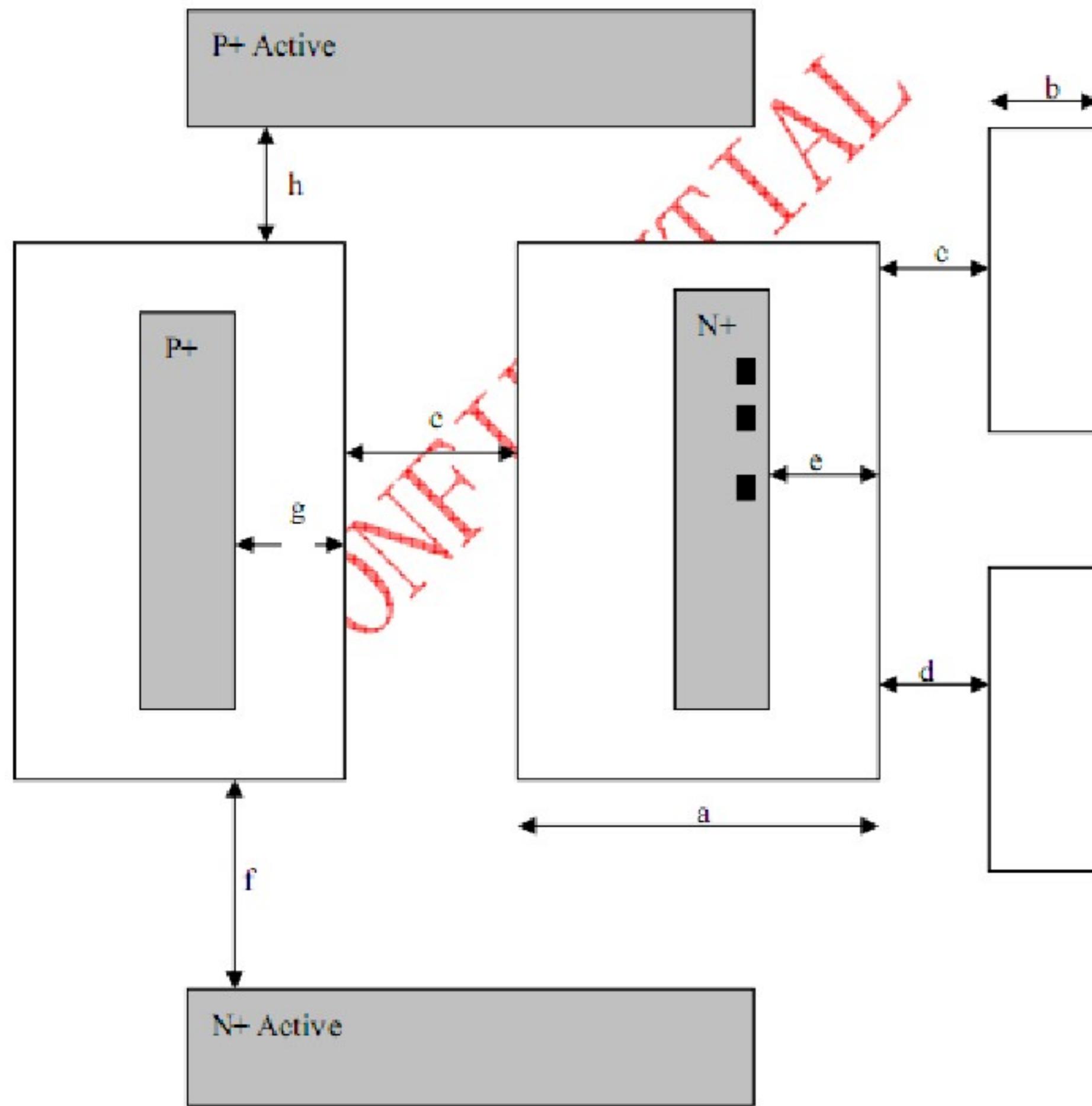


常用设计规则简介

8.1 N WELL (TB):

This mask defines the N-well for P channel devices.

a. N-well width for interconnect	2.5
b. N-well width for resistor	4.0
c. N-well spacing with different potential	4.0
d. N-well spacing with same potential	1.4
(N-well pattern shall be merged if space is less)	
e. Overlap from N-well to N+ inside N-well (pick up)	0.4
f. Space from N-well to N+ outside N-well	2.1
g. Overlap from N-well to P+ inside N-well	1.3
h. Space from N-well to P+ outside N-well (for P-well pick up)	0.8
i. Space to the edge of the scribe line	8.0





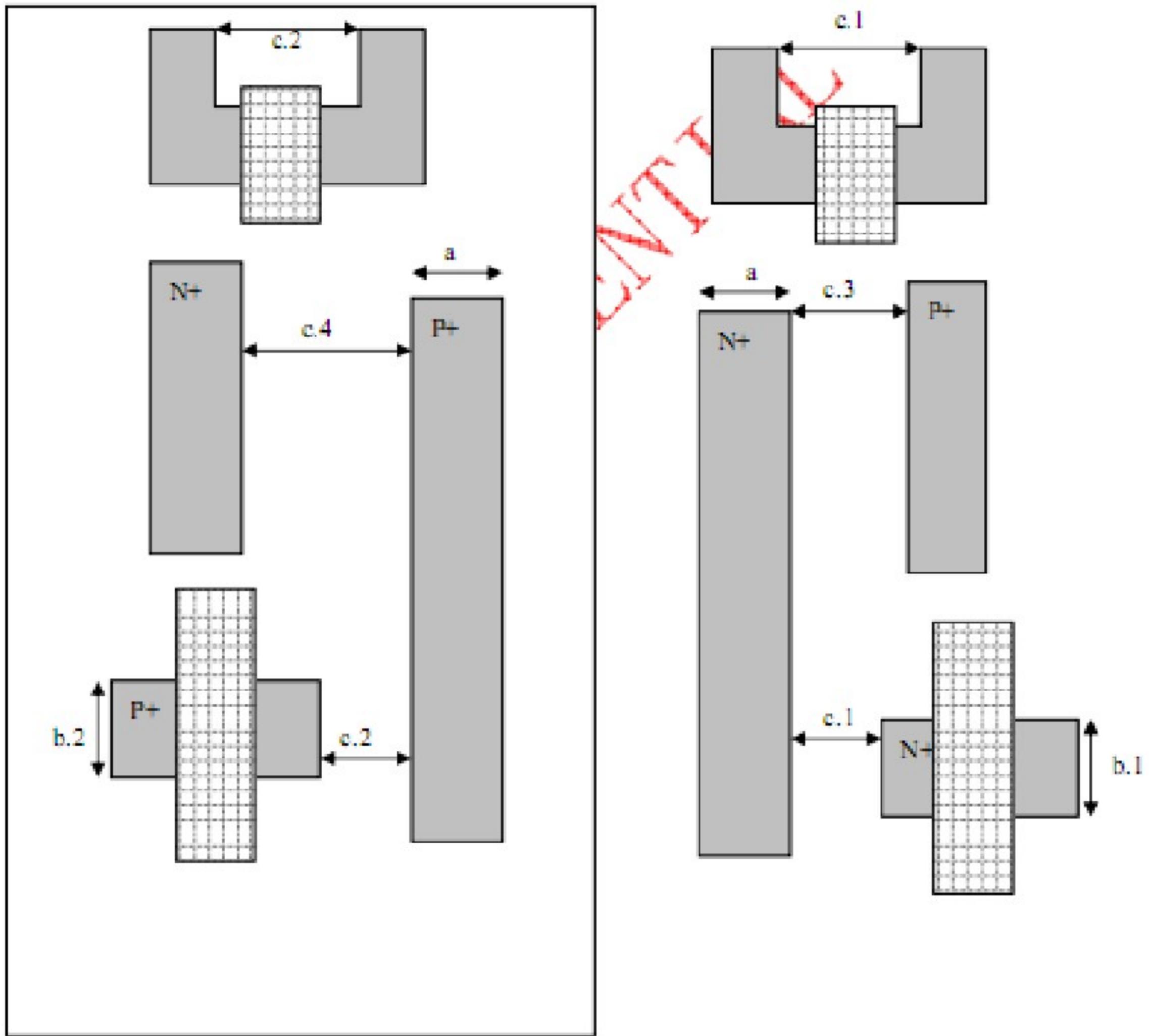
8.2 Active Area (TO):

This mask defines the active areas for N and P channel devices and diffused interconnect. Sometimes it is referred as the LOCOS or thin oxide area

a. Active width for interconnect	0.5
b. Active width for Channel width	
b.1 For NMOS	0.5
b.2 For PMOS	0.6
c. Spacing of Active (in the same well)	
c.1 Spacing between N+ Active to N+ Active	0.8
c.2 Spacing between P+ Active to P+ Active	0.8
c.3 Spacing of N+ Active to P+ Active in Substrate outside N-well	1.0
c.4 Spacing of N+ Active to P+ Active inside N-well	1.0

Notes : (1)Minimum field oxide area $2\mu\text{m}^2$

(2)Minimum active area $1\mu\text{m}^2$





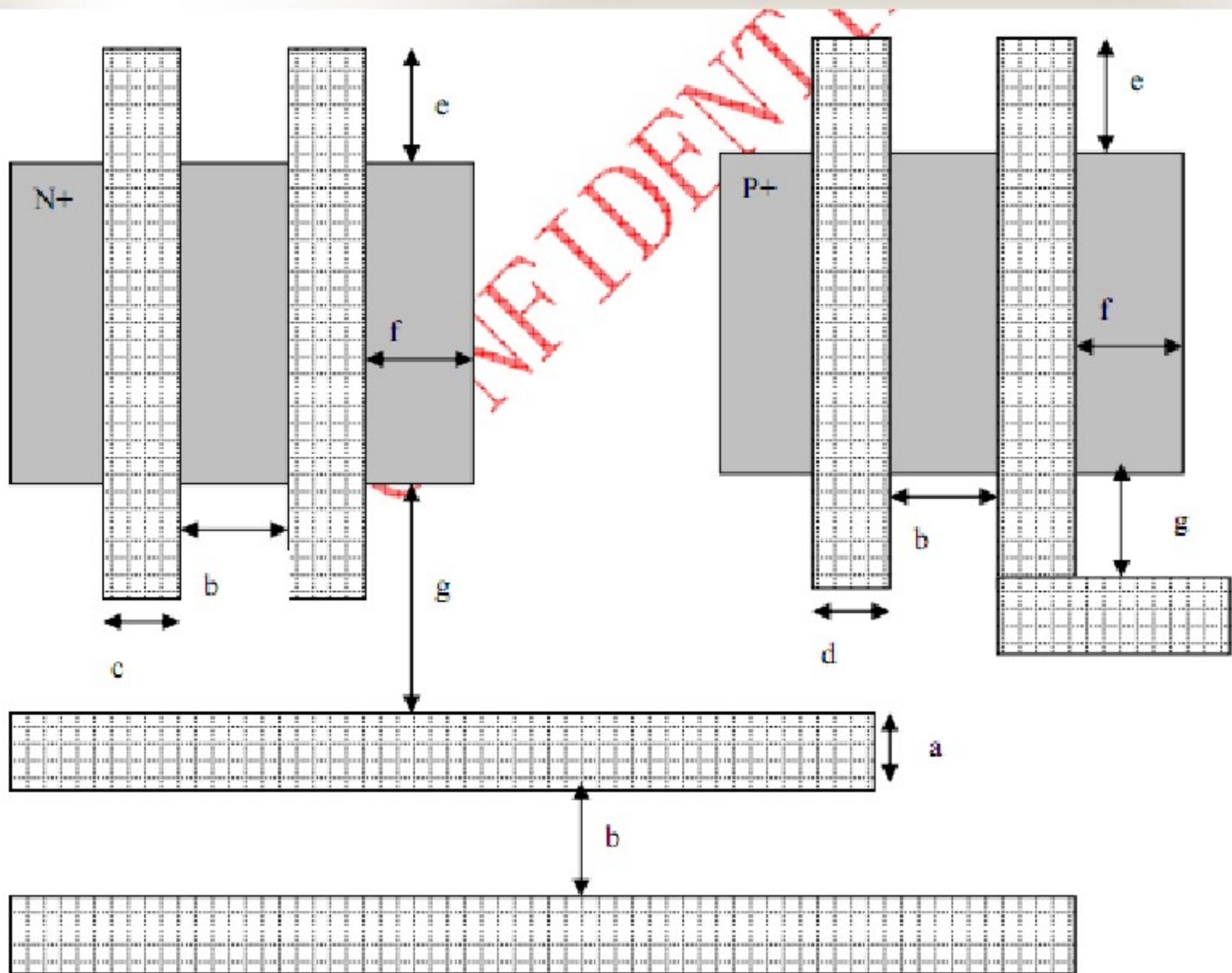
8.3 Poly1 (GT):

This mask defines the areas form the gate, poly interconnects, and poly word lines in the array.

- | | |
|---|------|
| a. Poly1 width for interconnect | 0.5 |
| b. Poly1 space | 0.5 |
| c. Poly1 width for NMOS channel length | |
| c.1 for normal threshold voltage NMOS & ROM code | 0.5 |
| c.2 for low threshold voltage NMOS | 1.0 |
| c.3 for depletion NMOS | 2.0 |
| d. Poly1 width for P channel length | |
| d.1 for normal threshold voltage PMOS | 0.55 |
| d.2 for low threshold voltage PMOS | 1.0 |
| d.3 for depletion PMOS | 2.0 |
| e. Poly1 Overhang out of Active into field (ENDCAP) | 0.55 |
| f. Poly1 gate to related diffusion edge | 0.5 |
| g. Poly1 on field to Active edge | 0.1 |
| h. Poly1 width for resistor | 1.0 |
| i. Poly1 space for resistor | 1.0 |

Notes : Maximum poly area on diffusion $100*100 \mu\text{m}^2$



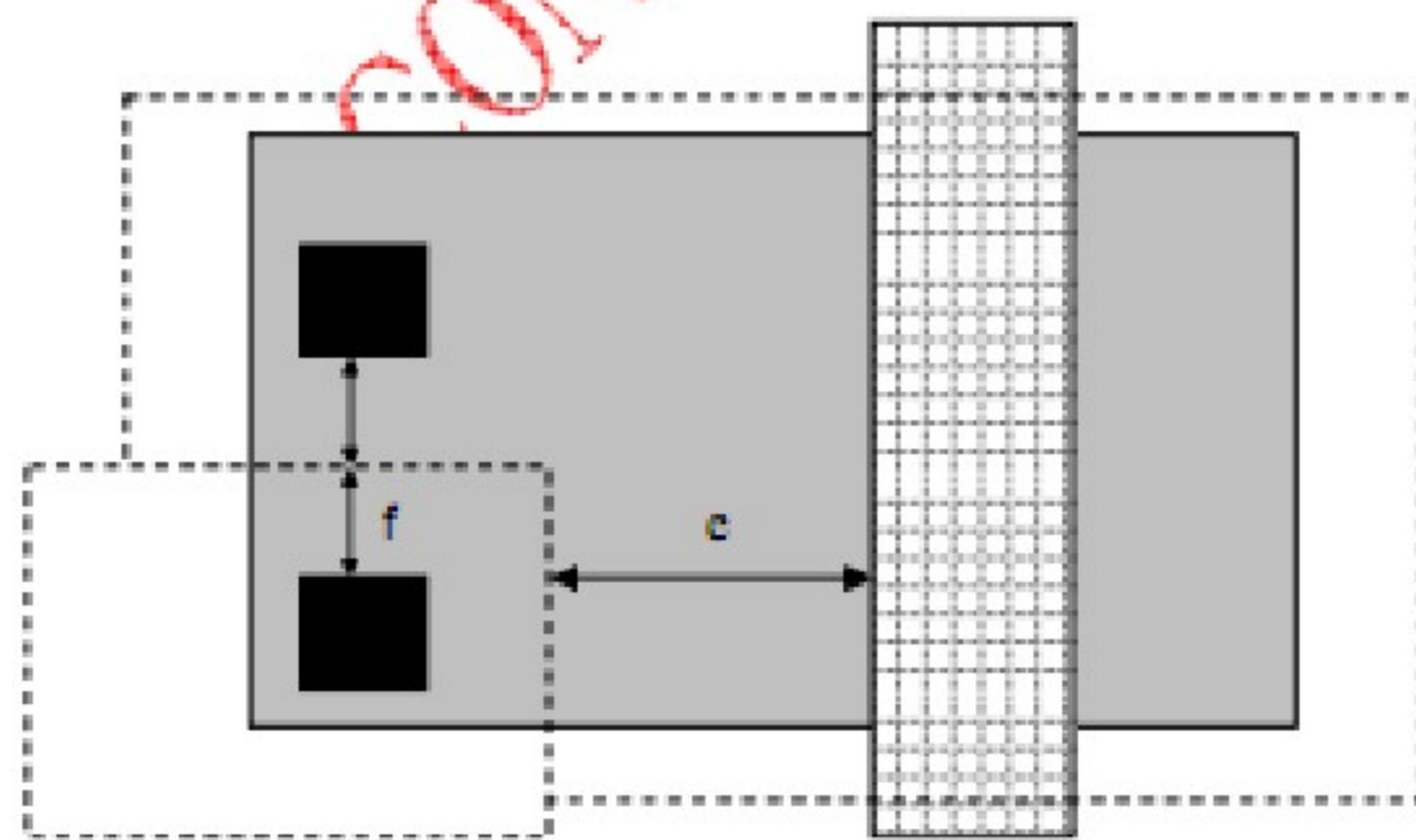
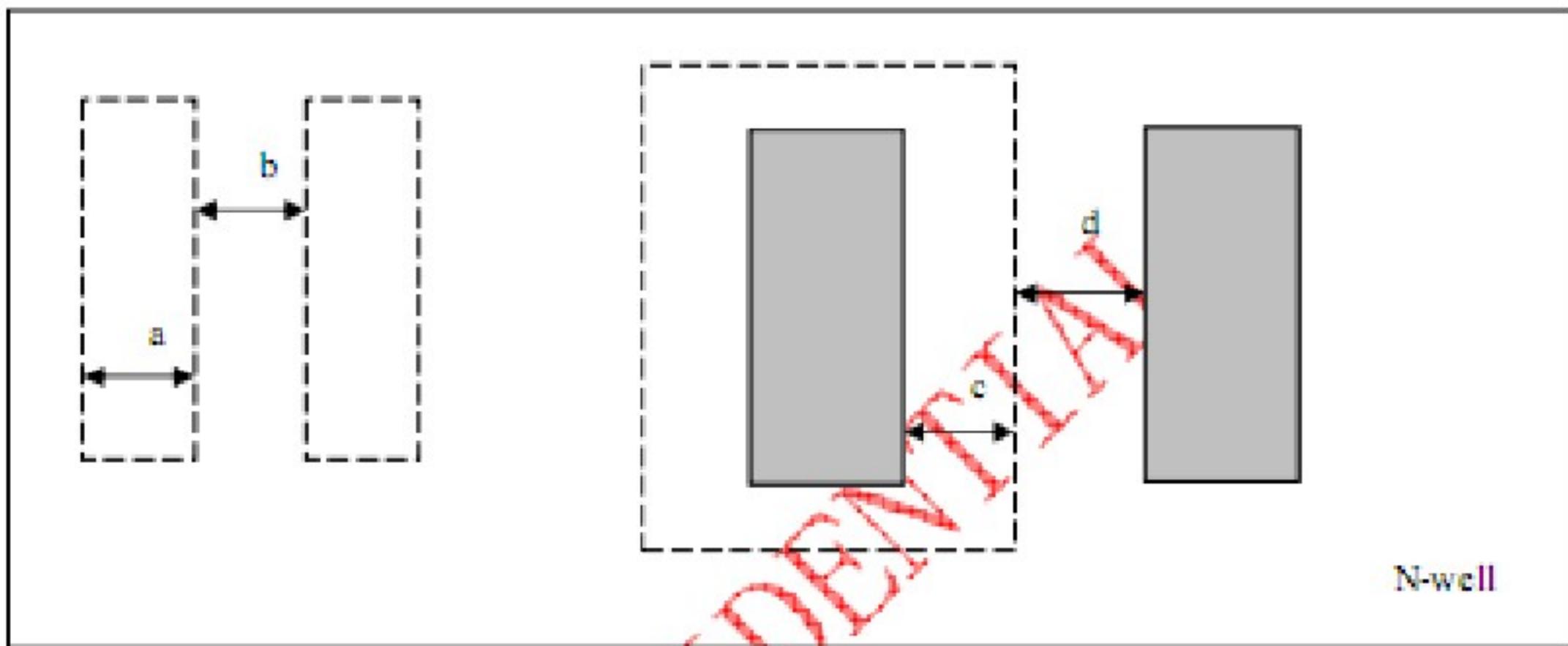




8.6 P+ implant area (SP):

This mask defines the areas of P channel device, P+ impurities are implanted into this region to form P channel source and drain.

a. Min. Width of P+ implant	0.8
b. Min. Space of P+ implant (merge if the space is less)	0.8
c. P+ implant enclose Active	0.5
d. P+ implant to unrelated Active space	0.5
e. Min. clearance from SP to poly gate	0.6
f. Min. extension of SP over contact	0.25
g. For Poly1 Line Resistor	
g-1. Min extension of SP over poly1 line as P-type poly1 resistor	0.5
g-2. Min clearance from SP to poly1 line as N-type poly1 resistor	0.5



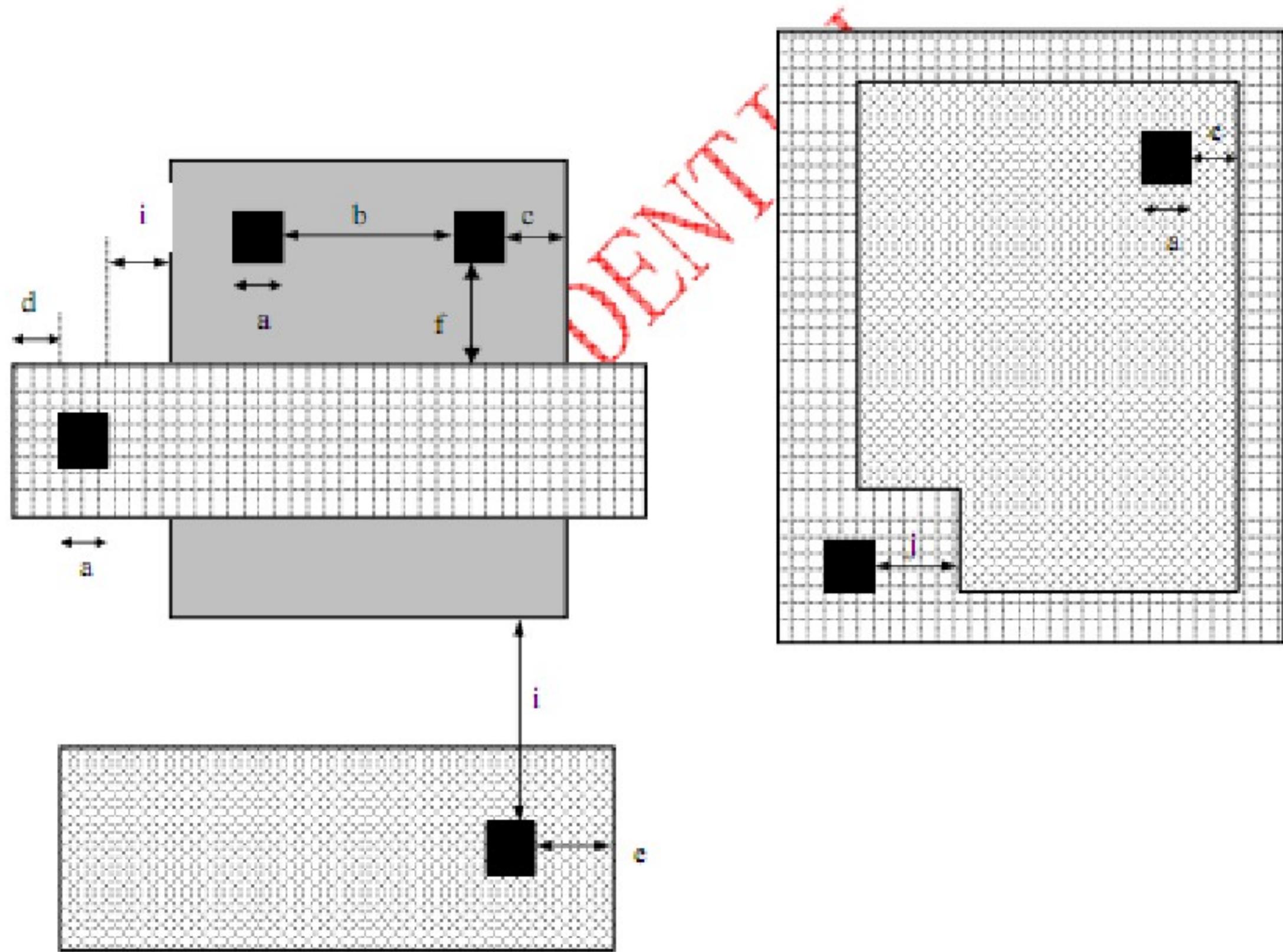


8.9 Contact (W1):

This mask defines the areas where all contacts are made to diffusion, poly1 and poly2.

- a. Min. & Max. Contact size 0.5x0.5
- b. Contact to contact Min. space 0.5
- c. Active overlap contact on Active
 - c.1 P-active overlap contact 0.3
 - c.2 N-active overlap contact 0.15
- d. Poly1 overlap contact on Poly1 0.3
- e. Poly2 overlap contact on Poly2 for interconnect 0.3
- f. Contact on Active to Poly gate space 0.4
- g. No contact on Poly gate in Active area is allowed
- h. No contact to field oxide is allowed.
- i. Poly1 and Poly2 contact to active area space 0.4
- j. Poly1 contact to Poly2 space 1.8

Note: Maximum current density is 1.5 mA/contact





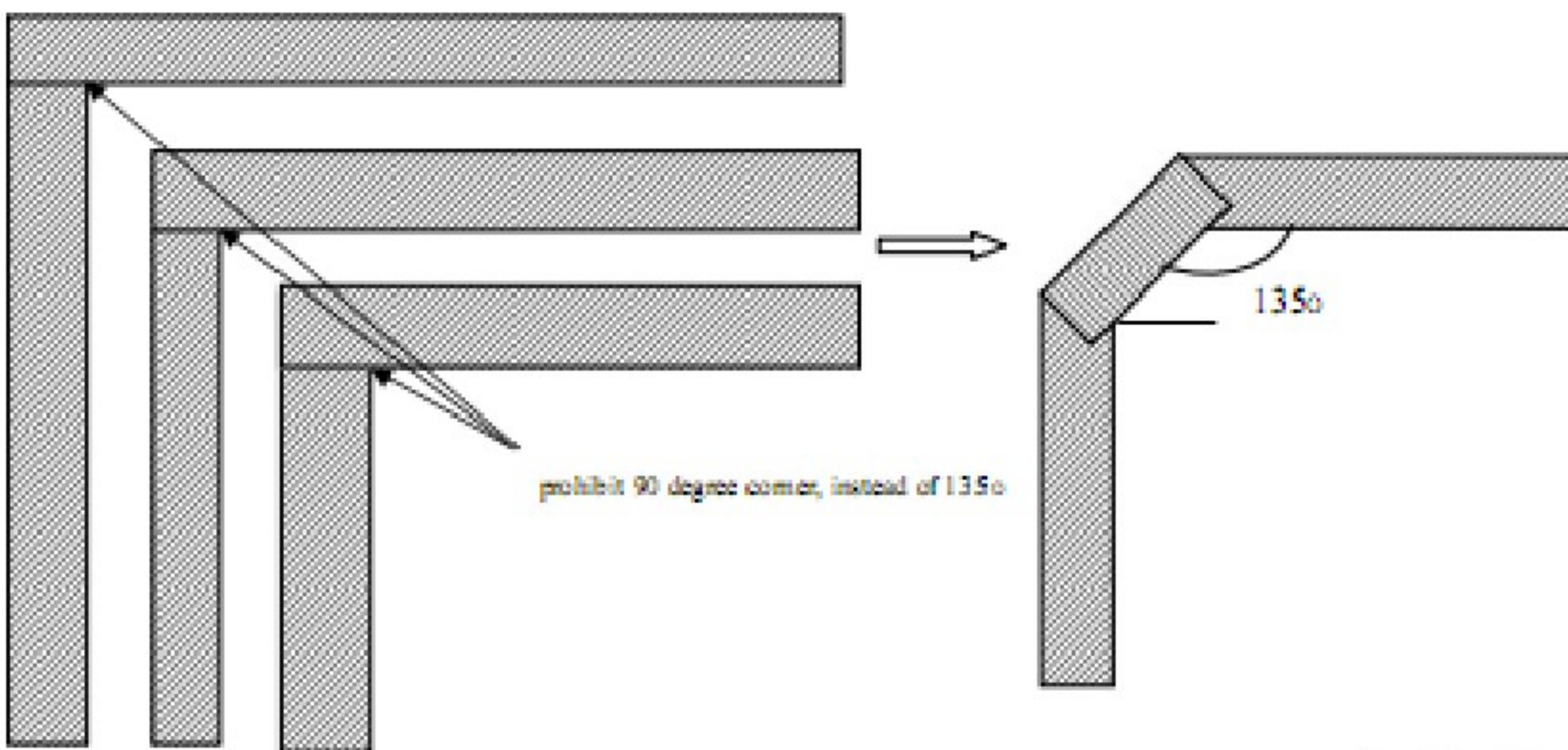
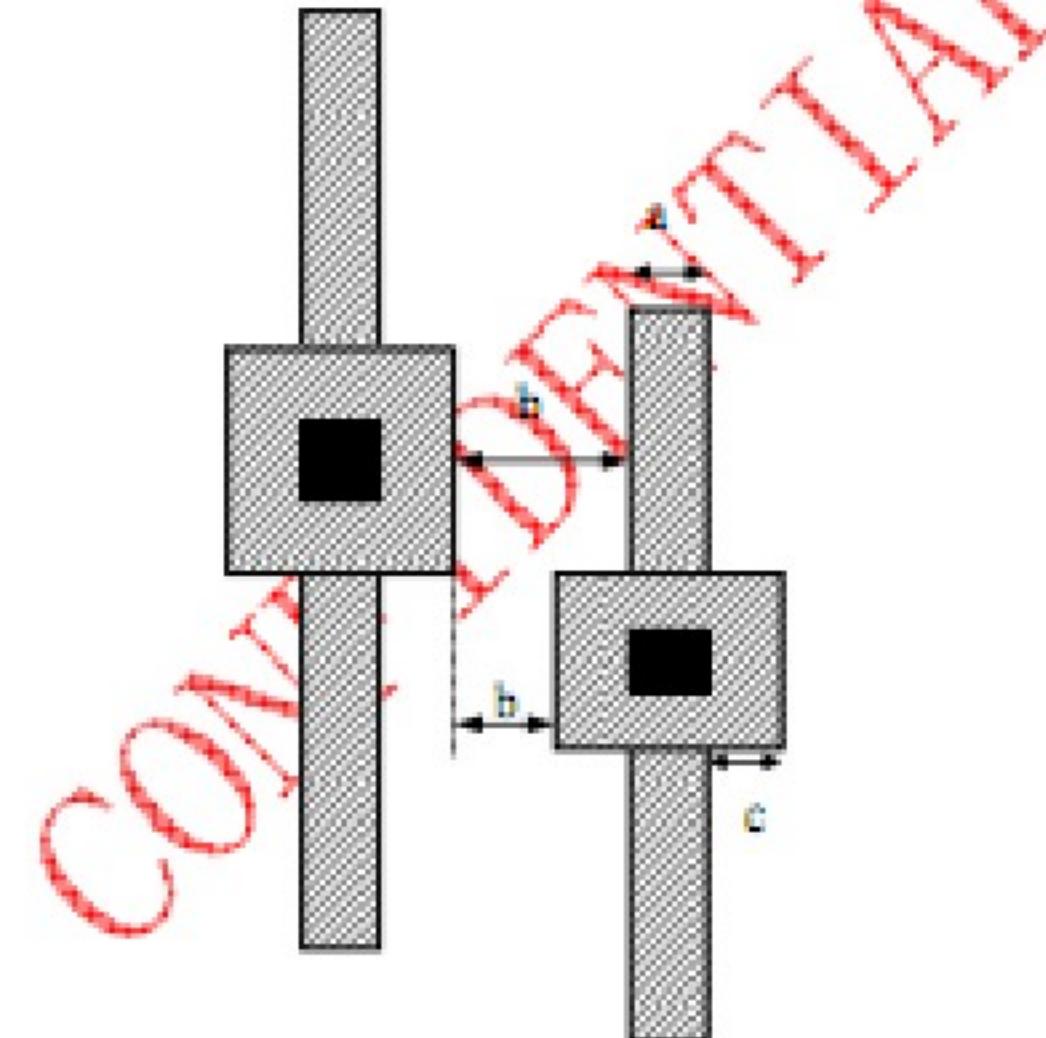
8.10 Metal 1 (A1):

This mask defines the first layer Metal interconnects. Metal1 should be used for local interconnect as much as possible.

- a. Metal1 width 0.6
- b. Metal1 to Metal1 space
 - b.1 Metal1 to Metal1 space (width < 10um) 0.6
 - b.2 Metal1 (width ≥ 10um) to any Metal1 1.1
- c.1 Metal 1 overlap over contact 0.3
- c.2 When metal width equal or larger than 10um 0.8
- d. The separation of two corner and a corner from a 45deg. line must satisfy the minimum spacing.

- Note:
- 1. Maximum current density for 1M 1.5mA/um
 - 2. Maximum current density for 2M/3M 0.8mA/um
 - 3. Avoid 90deg. elbow for parallel metal lines. Use 135deg. bend instead.
 - 4. Metal density, if more than 50% , please inform CSMC ; if less than 30% , please add dummy metal and follow CSMC's another document“ Dummy Metal Rule”.
 - 5. Minimum Isolation metal area 1.1*1.1







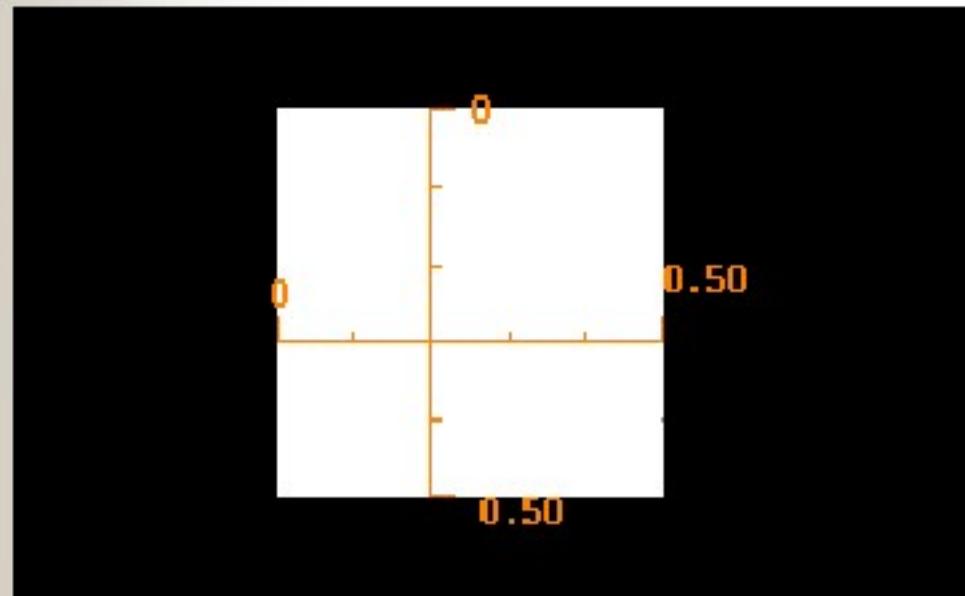
画出完整版图，并保存

- 版图设计是层次化的，**首先**要先在库中建立最基本的通孔，**其次**是基本逻辑门单元，每一级的画图都要保证内容的正确性。
- 我们的设计难度只要求两个层次：
 - 1.通孔（有源区-和金属1， poly和金属1）
 - 2.完整设计

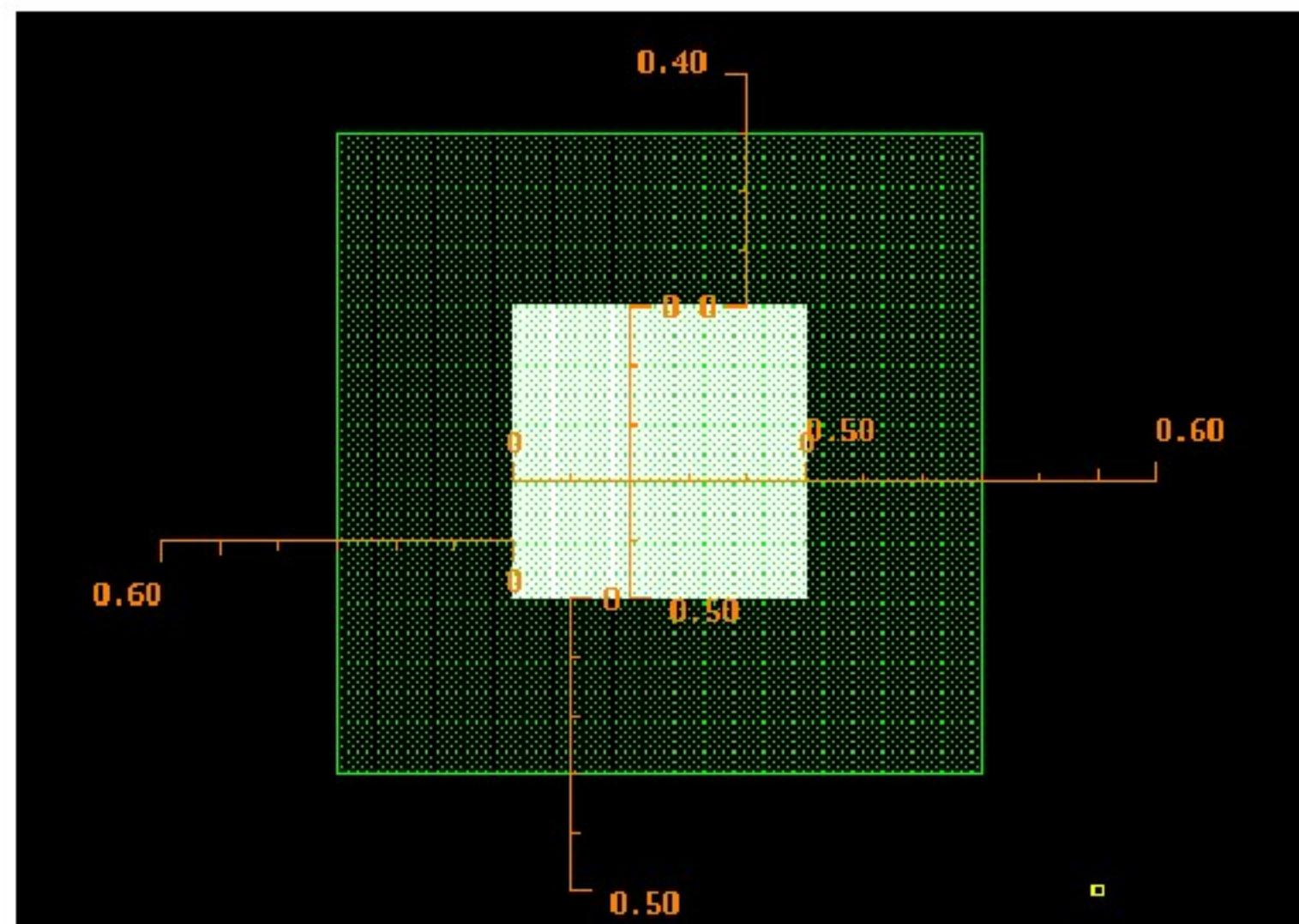


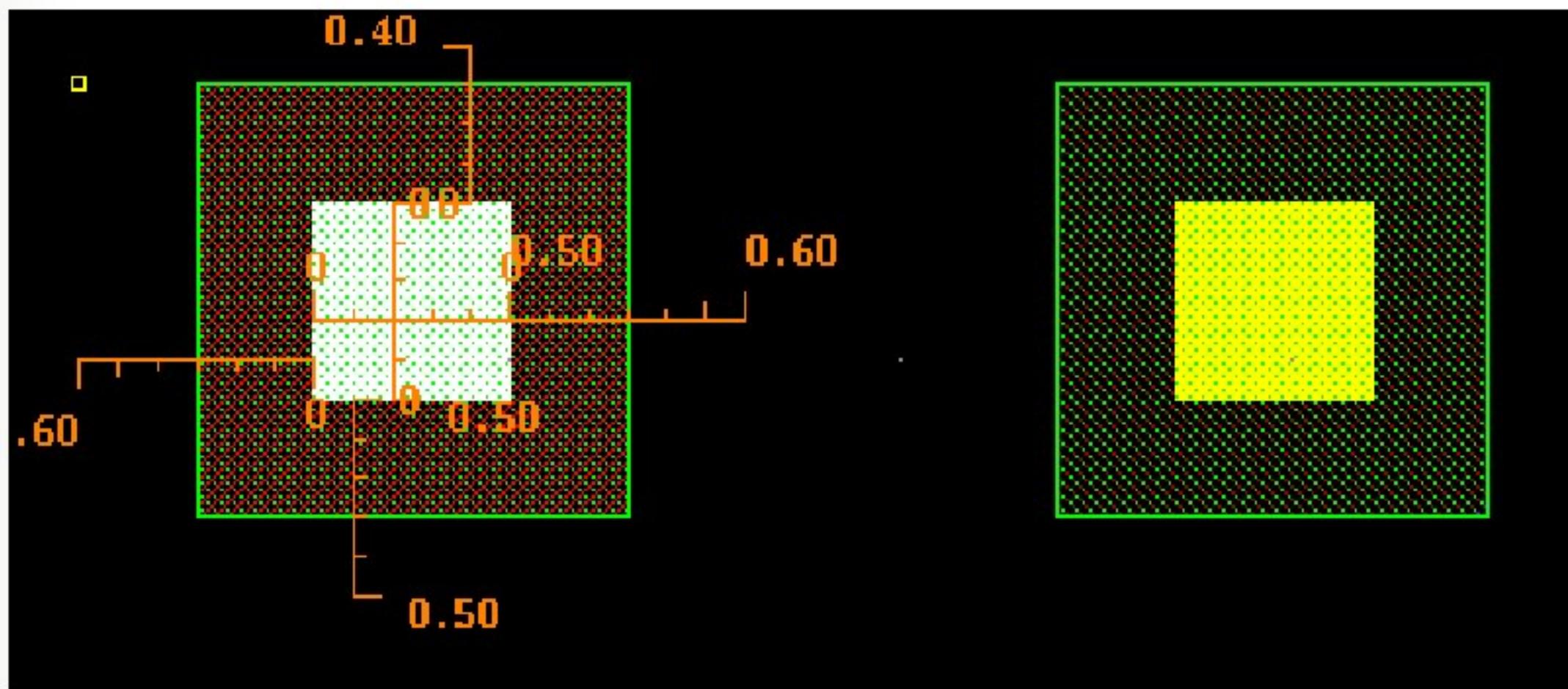
画出完整版图，并保存

■ 通孔的设计



0.5*0.5的孔，
金属有0.3的外
延

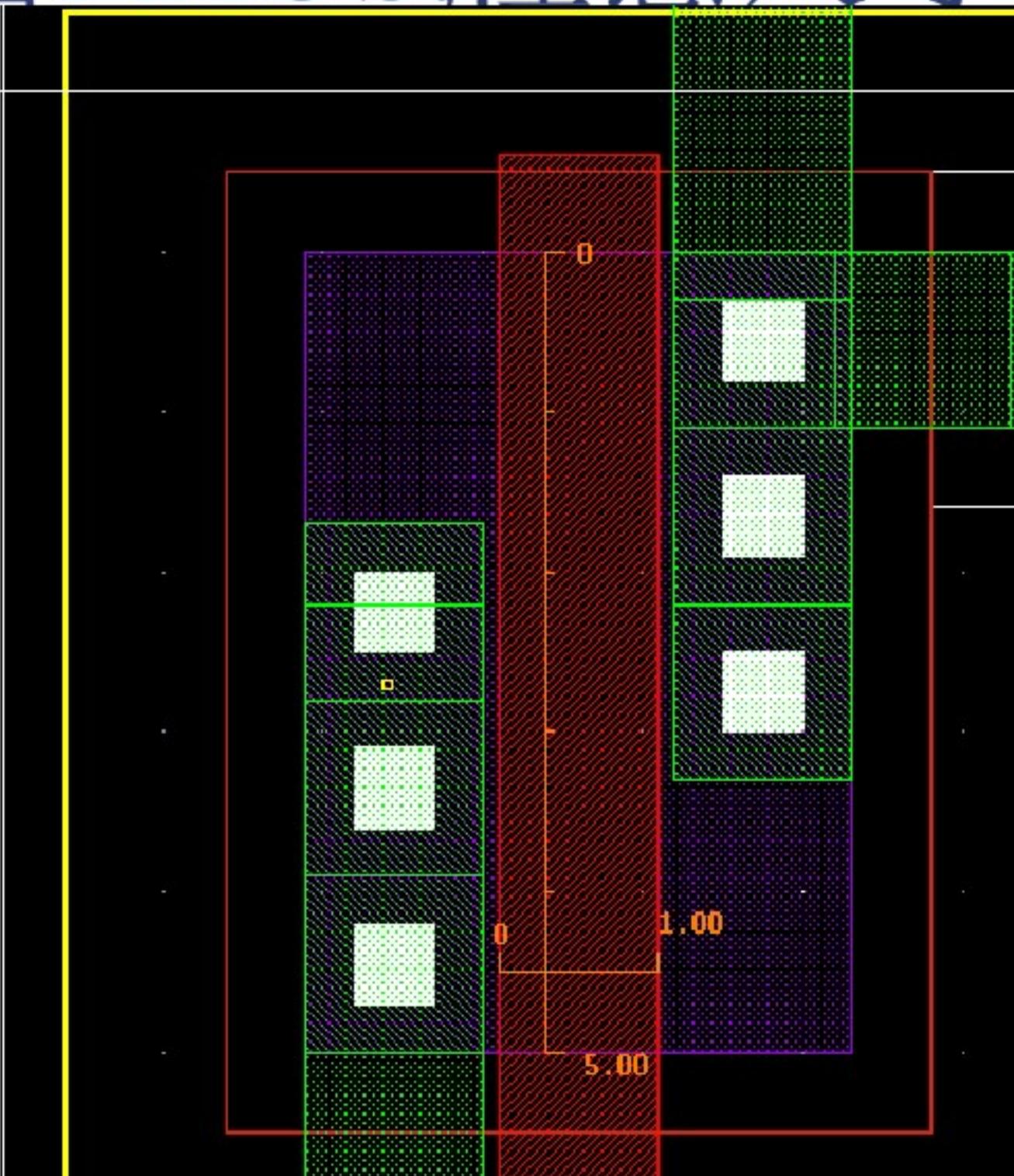




有源区和多晶硅的覆盖大小和金属一样就可以满足DRC

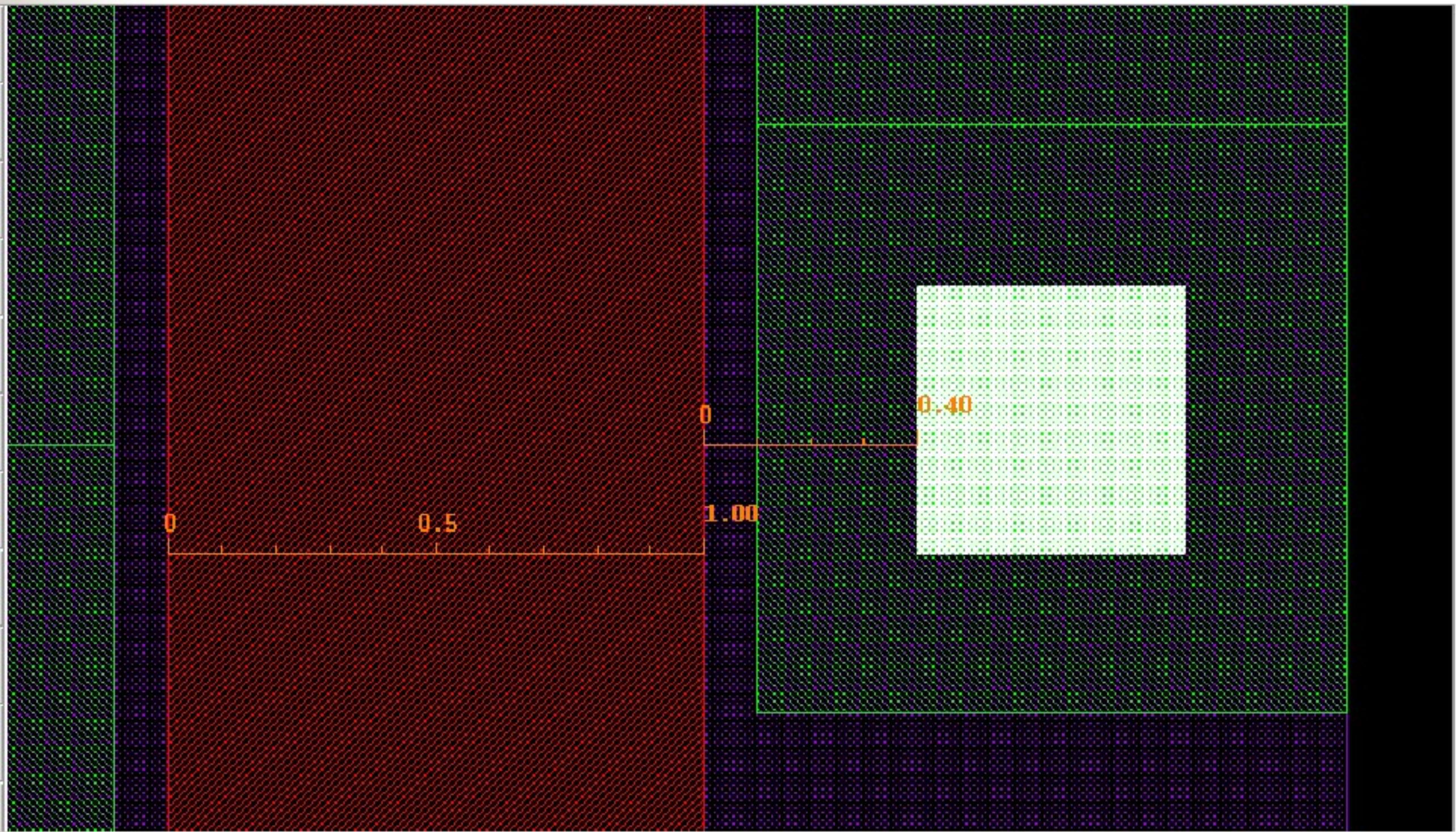


画出PMOS,注意尺寸



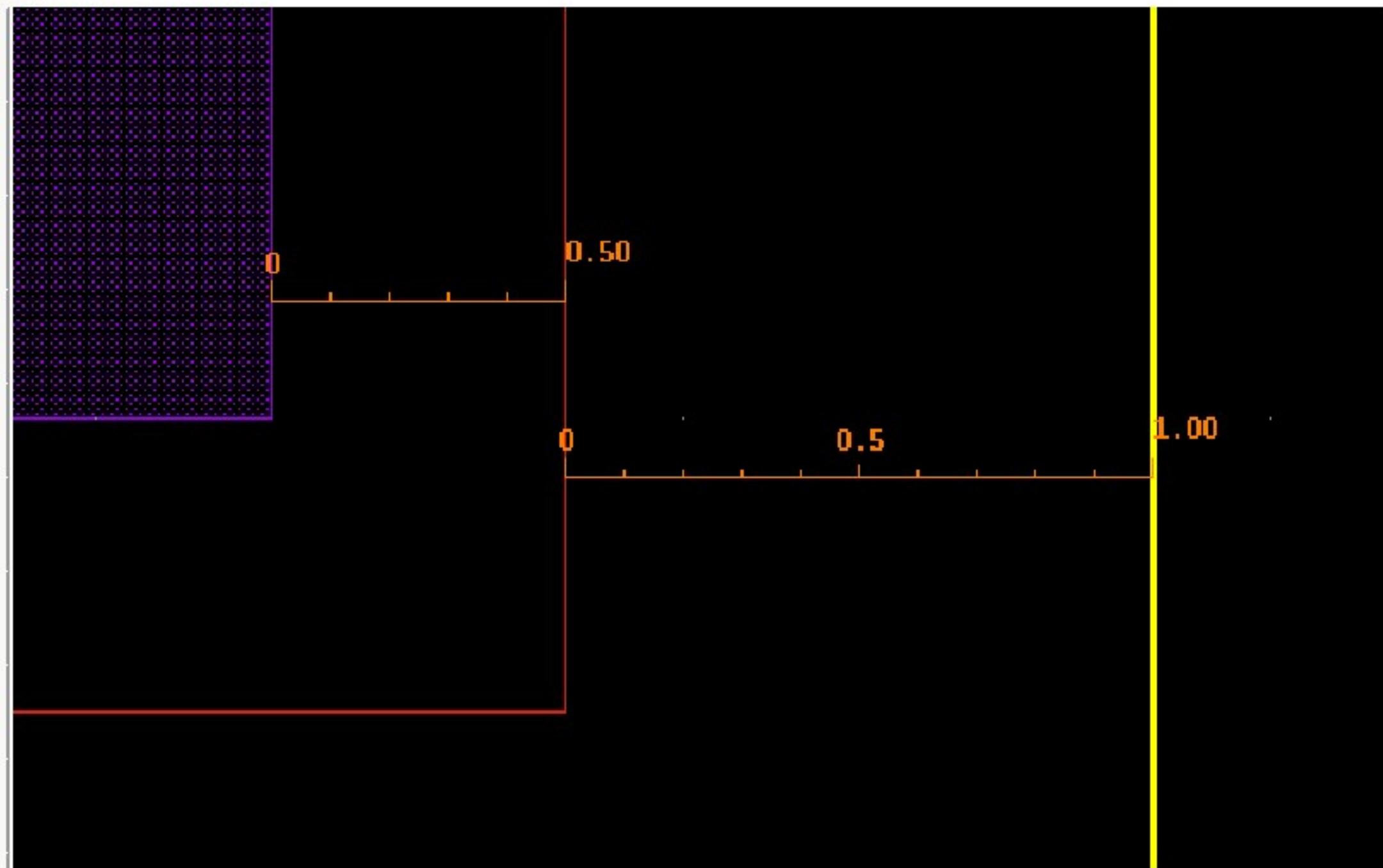


首先是栅宽度和长度，
然后是孔到栅的距离



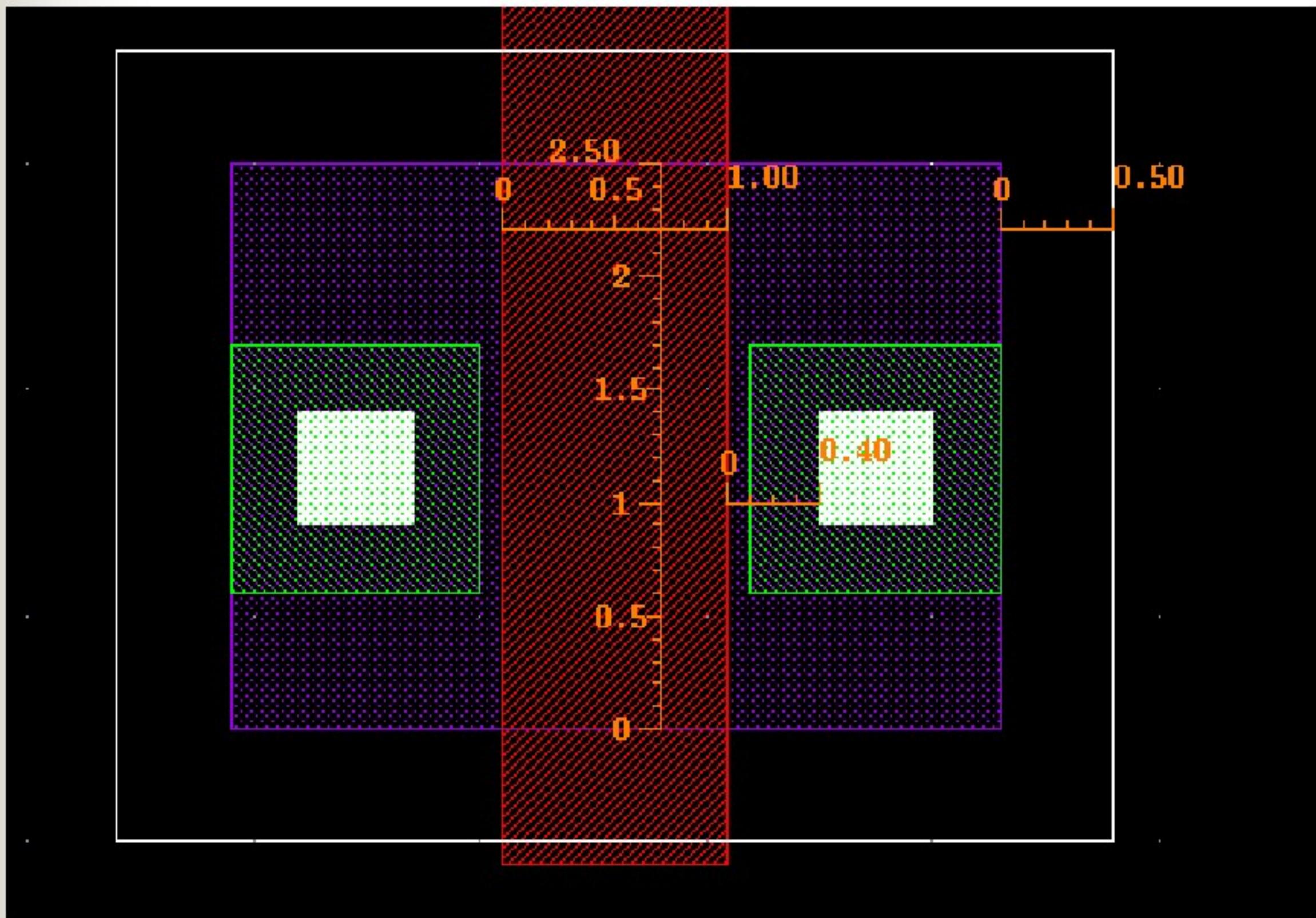


注入框和有源区的覆盖，井和注
入框的覆盖



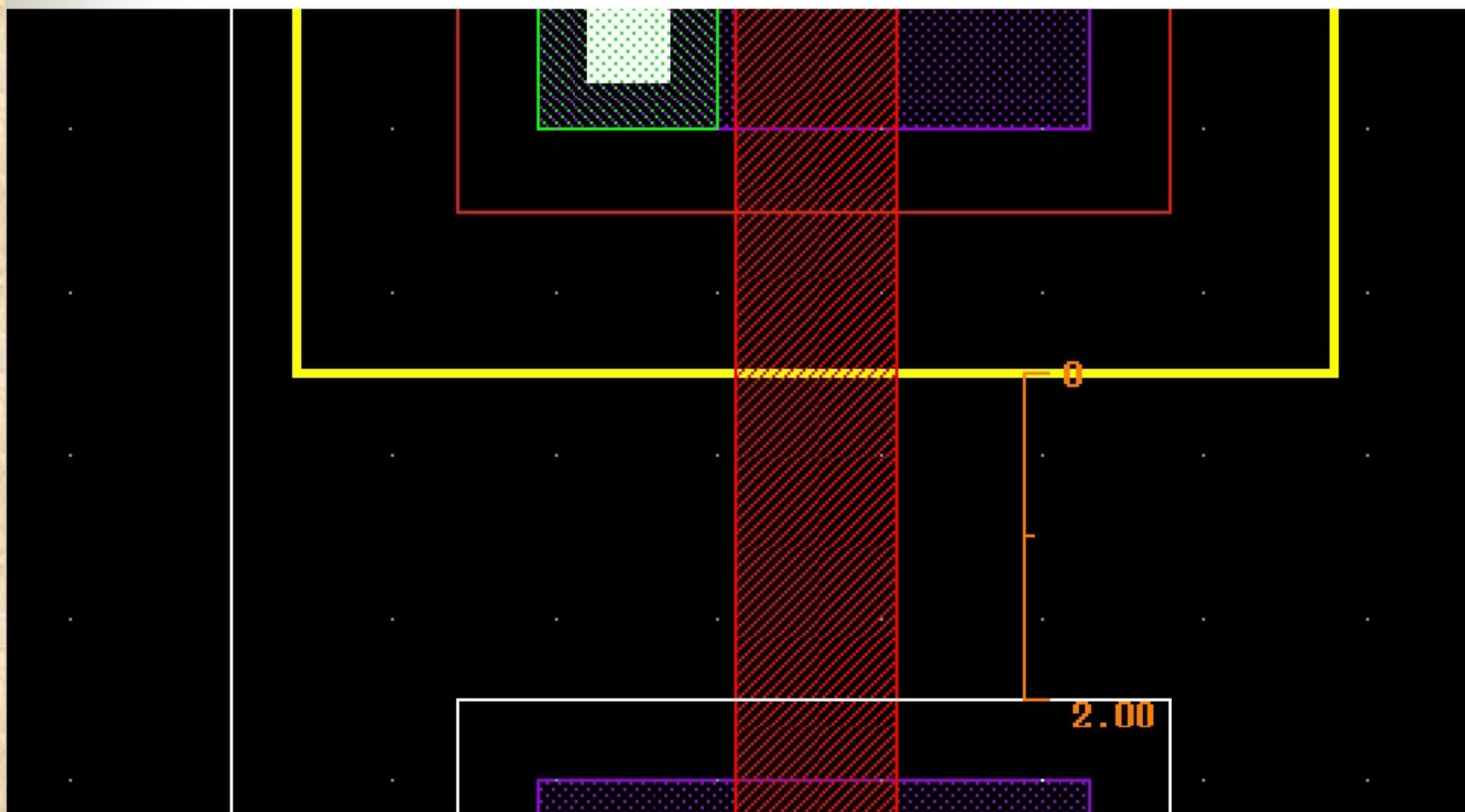


同理画出NMOS



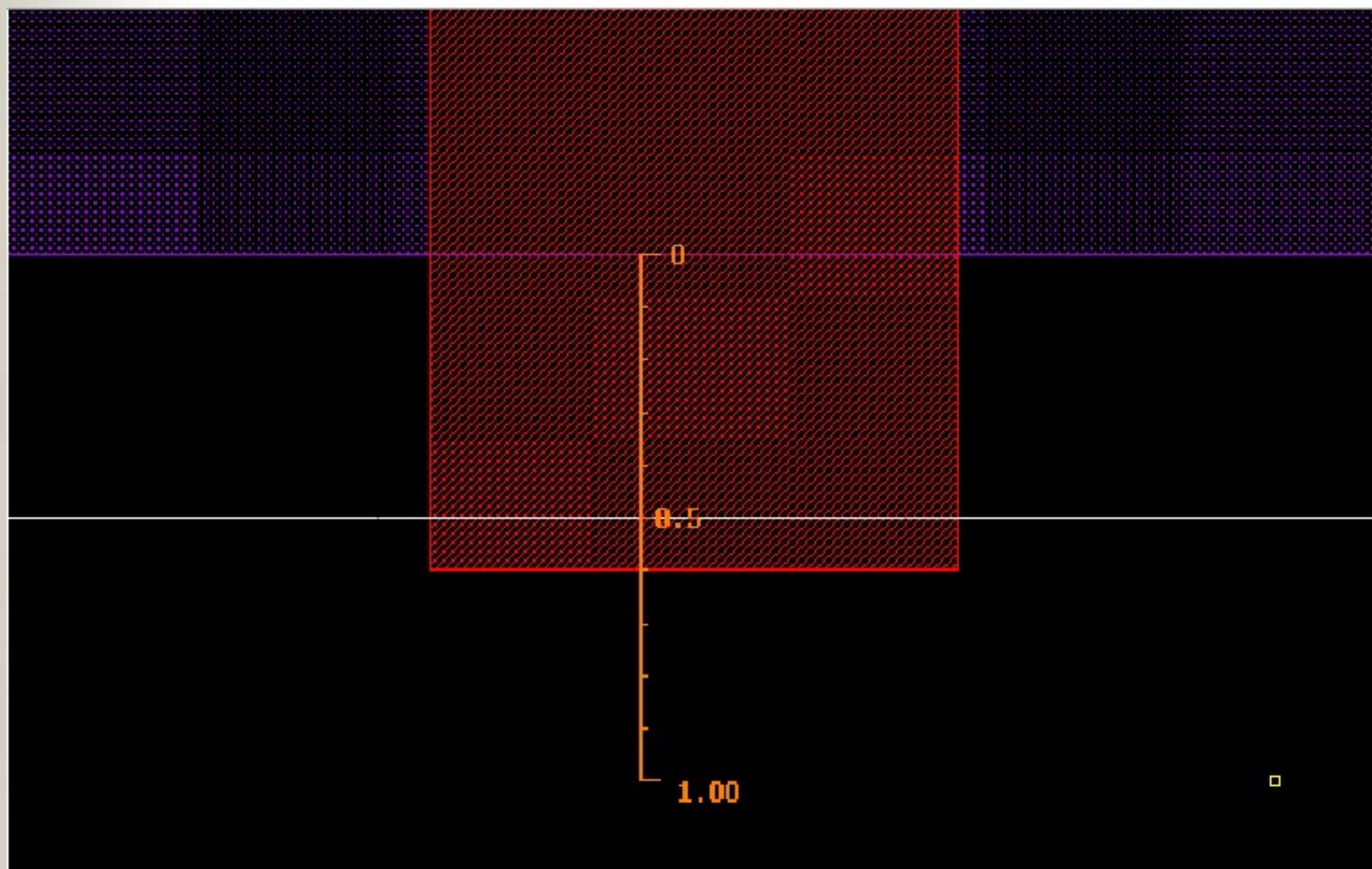


调节一下NMOS, PMOS之间的距离



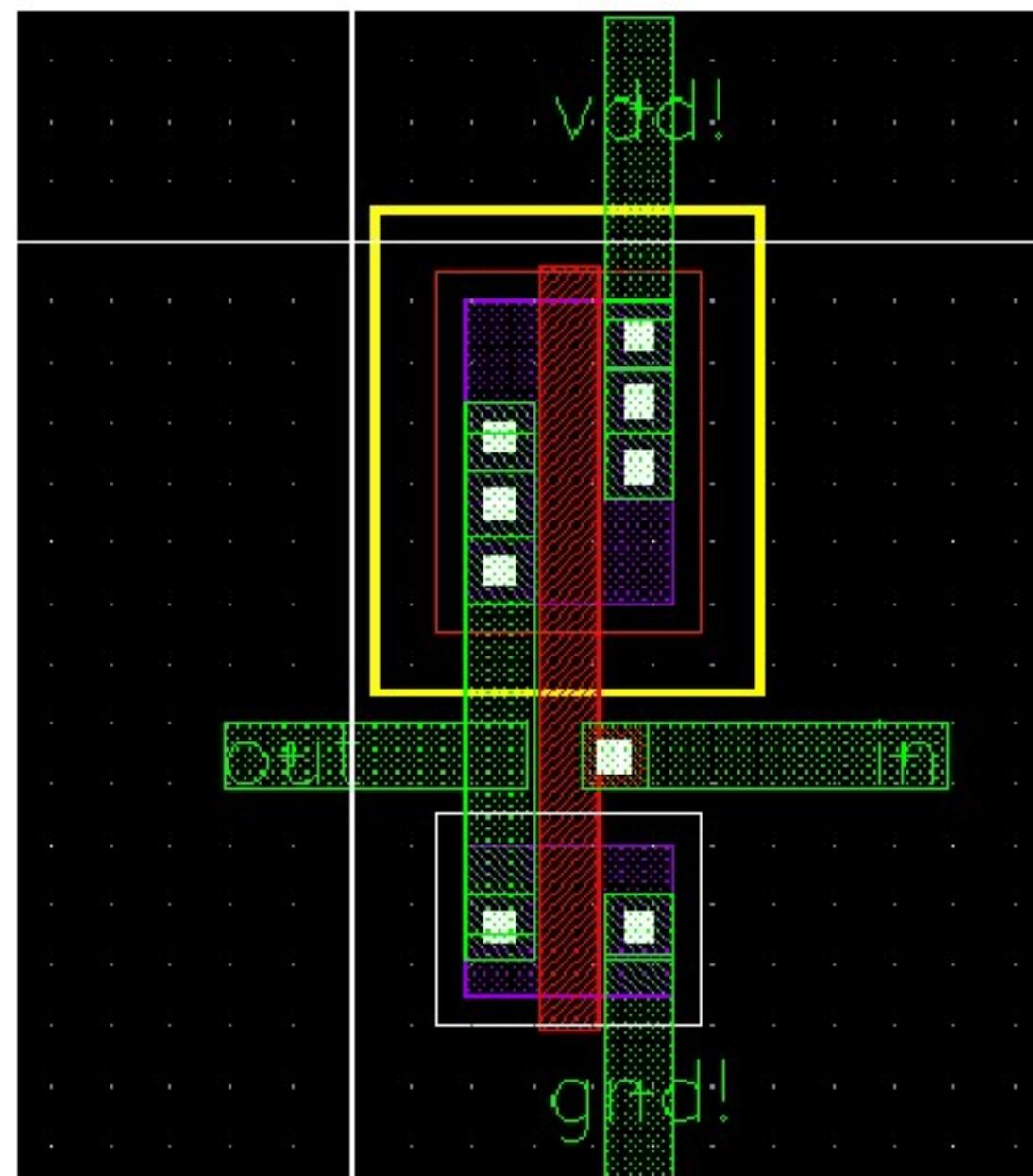
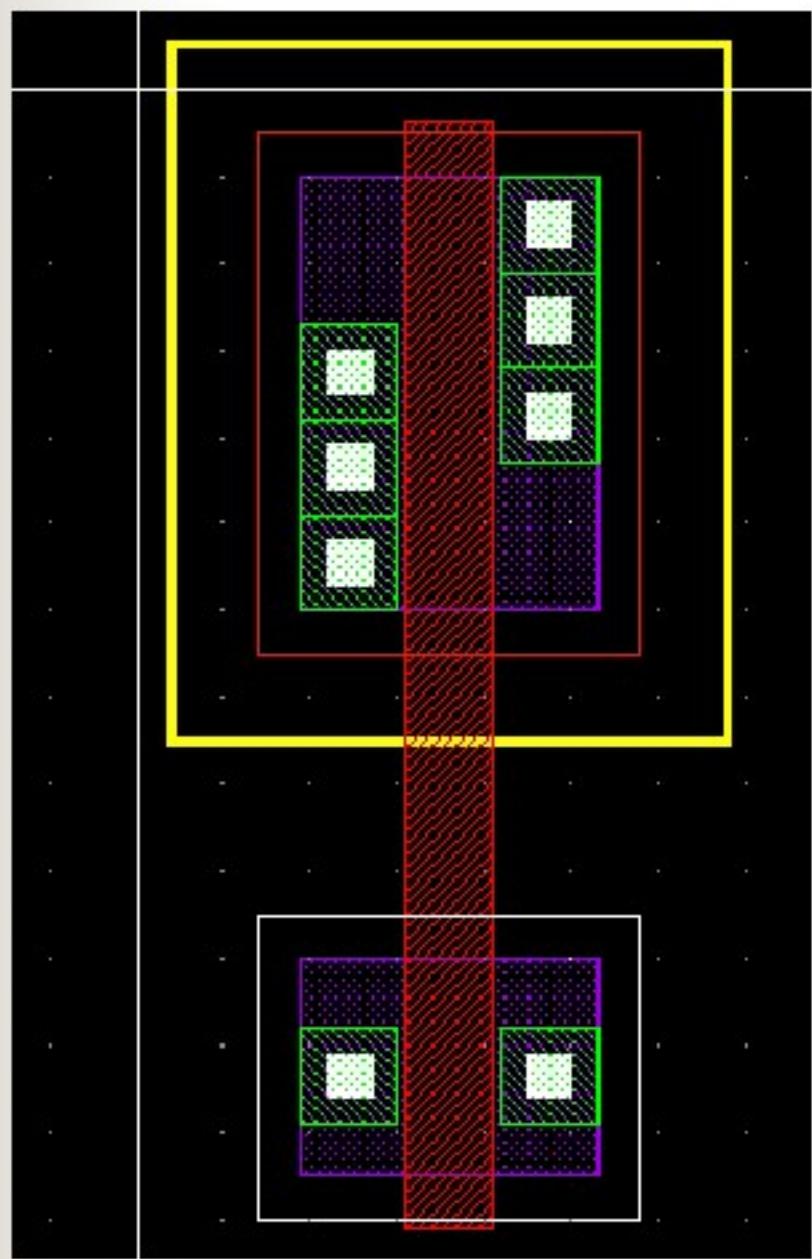


注意一下多晶硅对有源区的覆盖



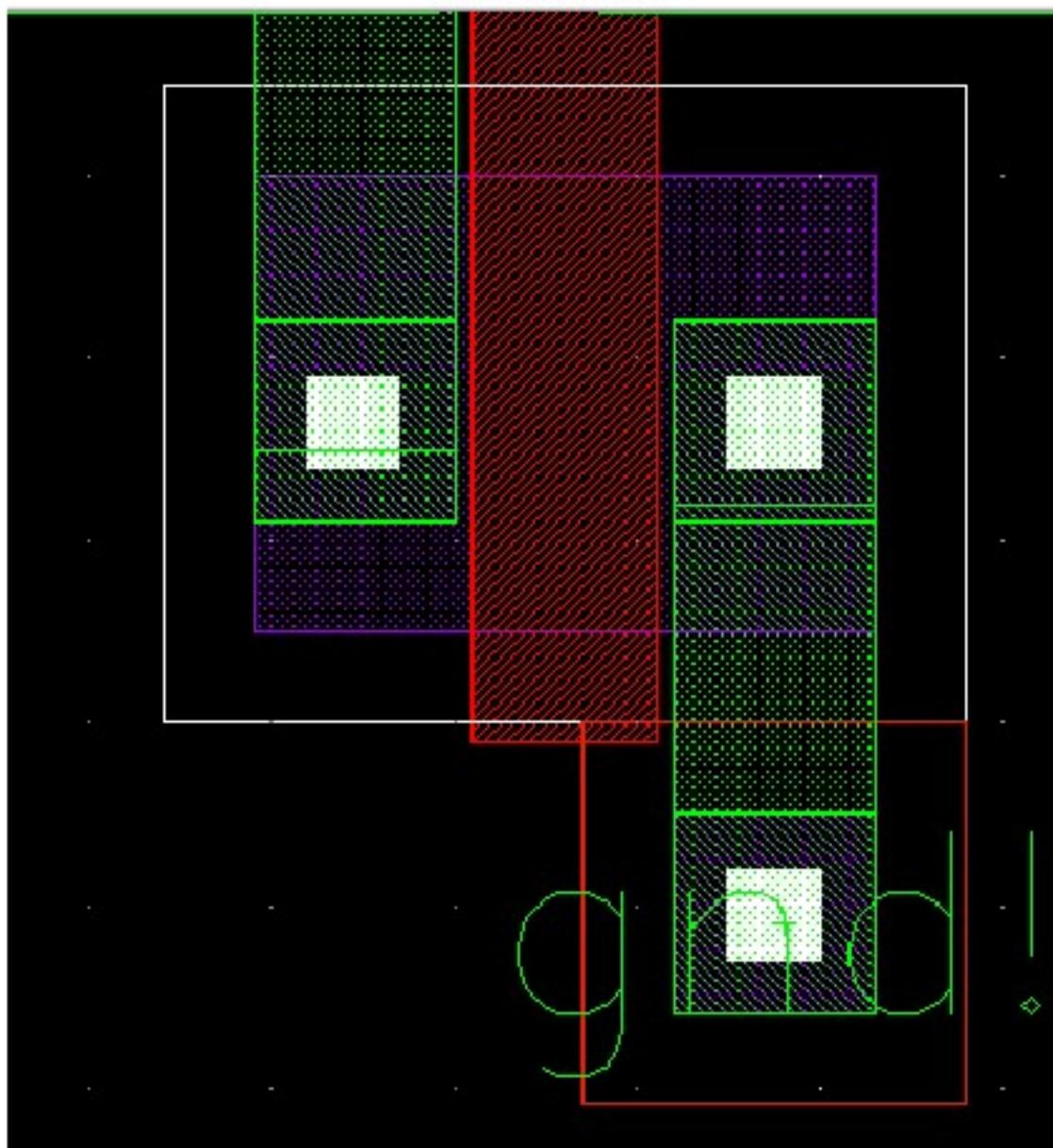
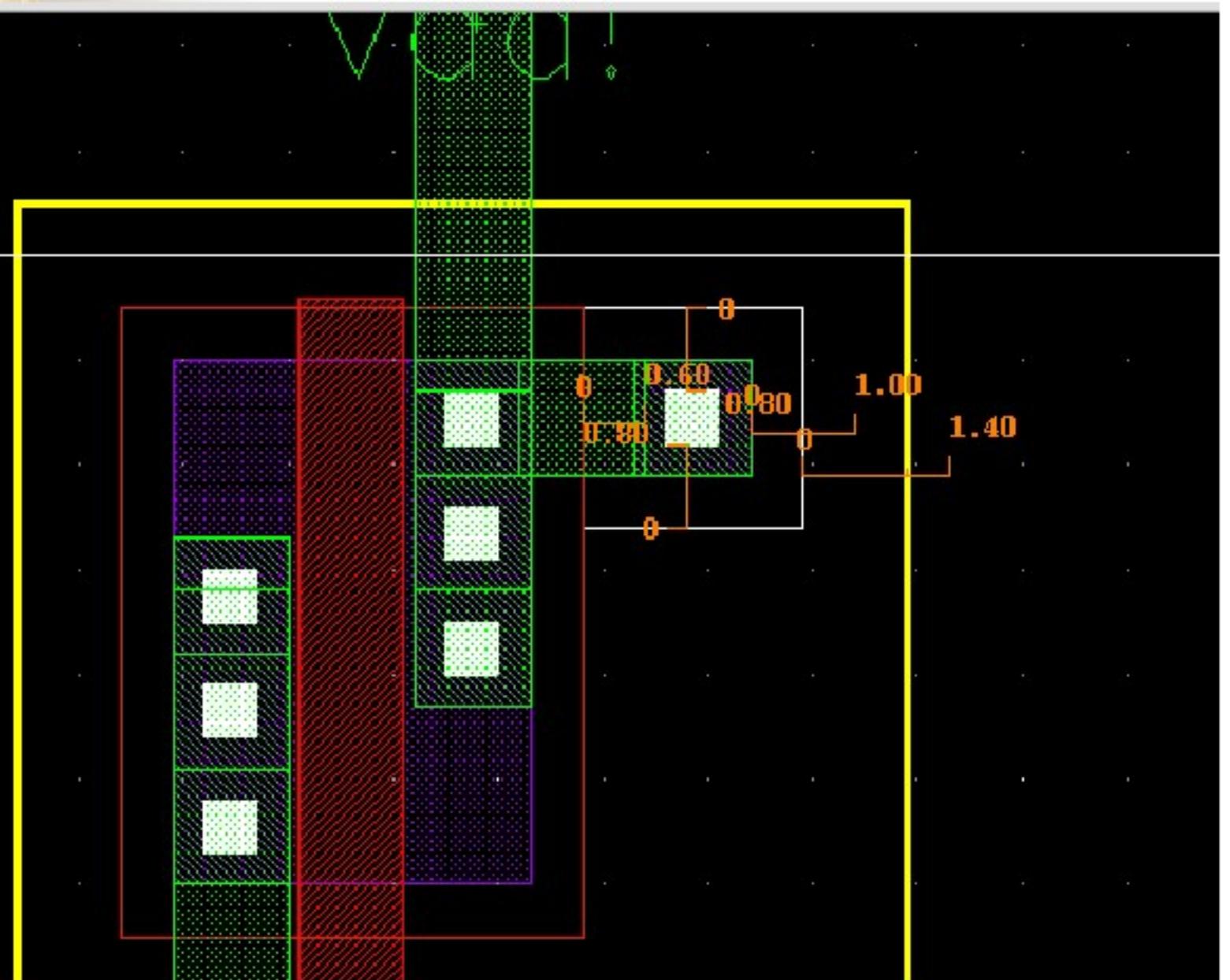


完成反相器版图设计





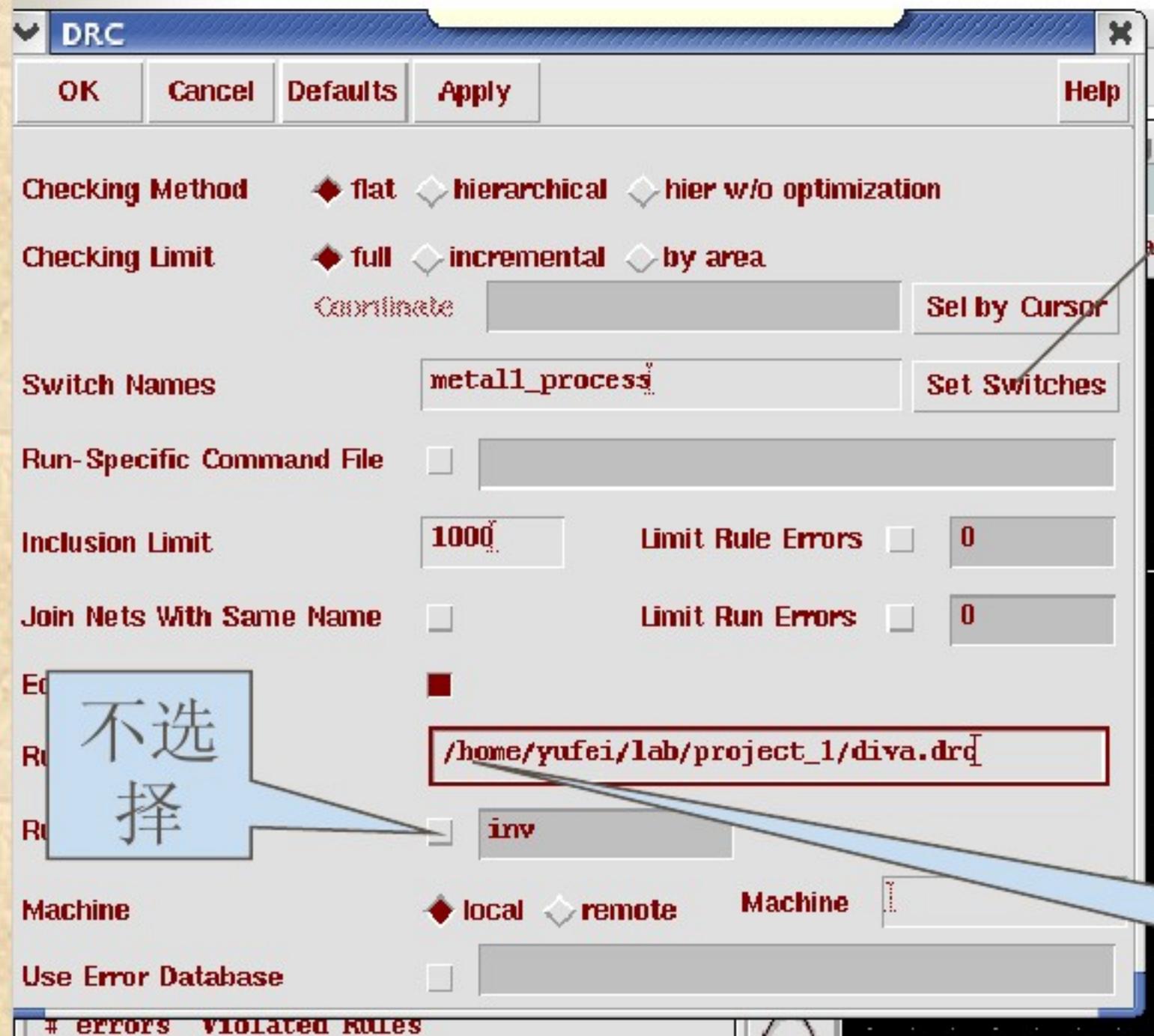
给阱和衬底接上电位



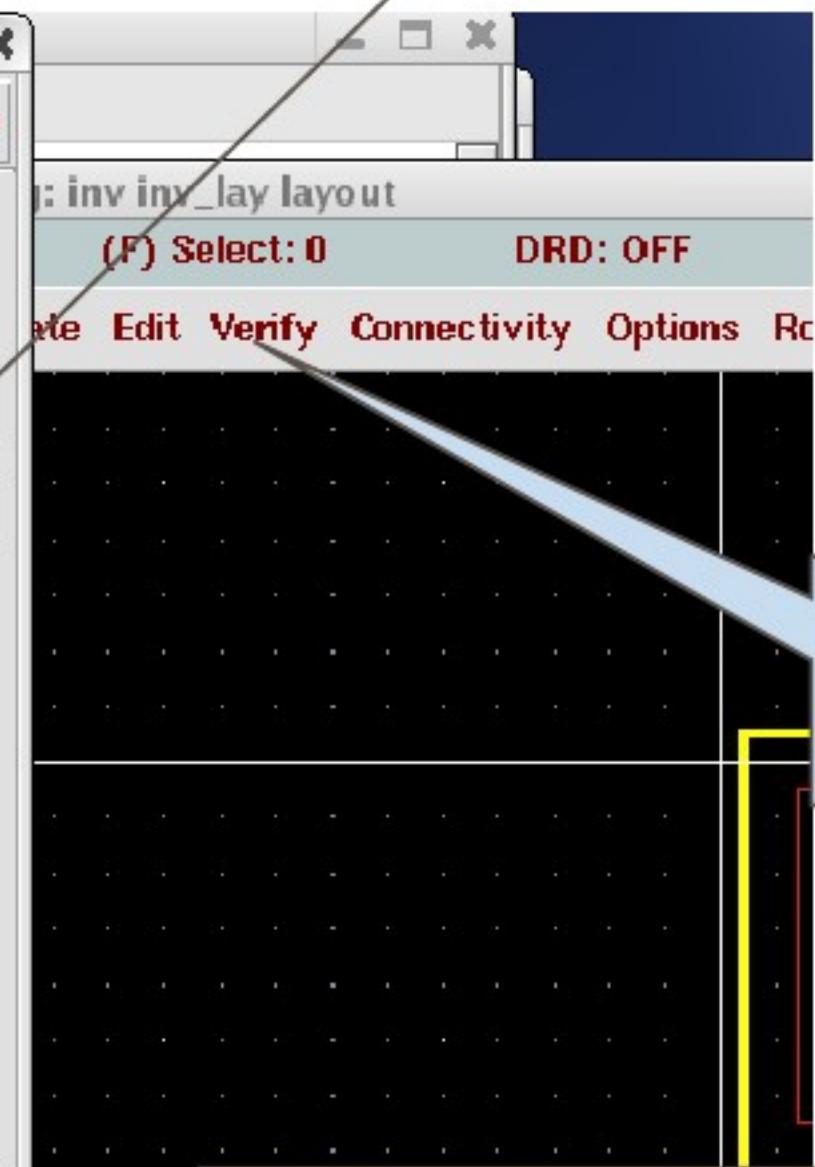


版图检查-DRC(diva)

指定金属层数



不选择



选择
DRC

把Diva的DR
路径写入



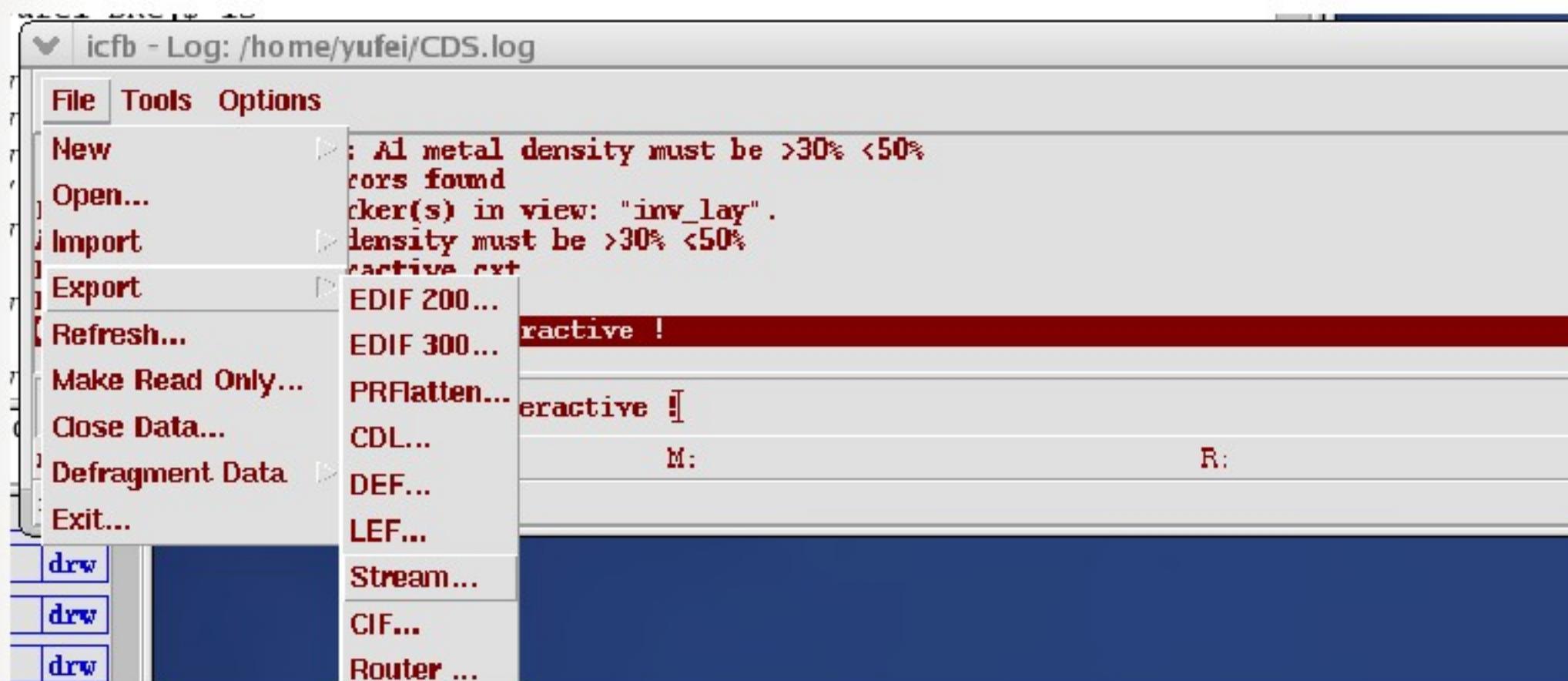
版图检查-DRC (dracula)

■ 六步法:

- 1. 导出GDSII文件
- 2. 进入PDRACULA
- 3. 运行修改好的dracula drc runset:
`/g filename`
- 4. 结束:
`/f`
- 5. jxrun.com
- 6. 在layout editor中setup



导出GDSII文件





```
Terminal
File Edit View Terminal Go Help

*      0.129 Mbytes allocated to the current process.
*      0.129 Mbytes is still in use.
* THE END OF PROGRAM                      TIME = 16:01:45      DATE =21-SEP-2008 *

*/N* AT STAGE: 349

*****
*/N* GDS2OUT (REV. 4.9.06-2006      / LINUX          /GENDATE: 6-JUN/2006 )
      *** ( Copyright 1995, Cadence ) ***
*/N* EXEC TIME =16:01:45      DATE =21-SEP-2008      HOSTNAME = szptyufe
*****
*      0.129 Mbytes allocated to the current process.
*      0.129 Mbytes is still in use.
* THE END OF PROGRAM                      TIME = 16:01:45      DATE =21-SEP-2008 *

* THE END OF PROGRAM *

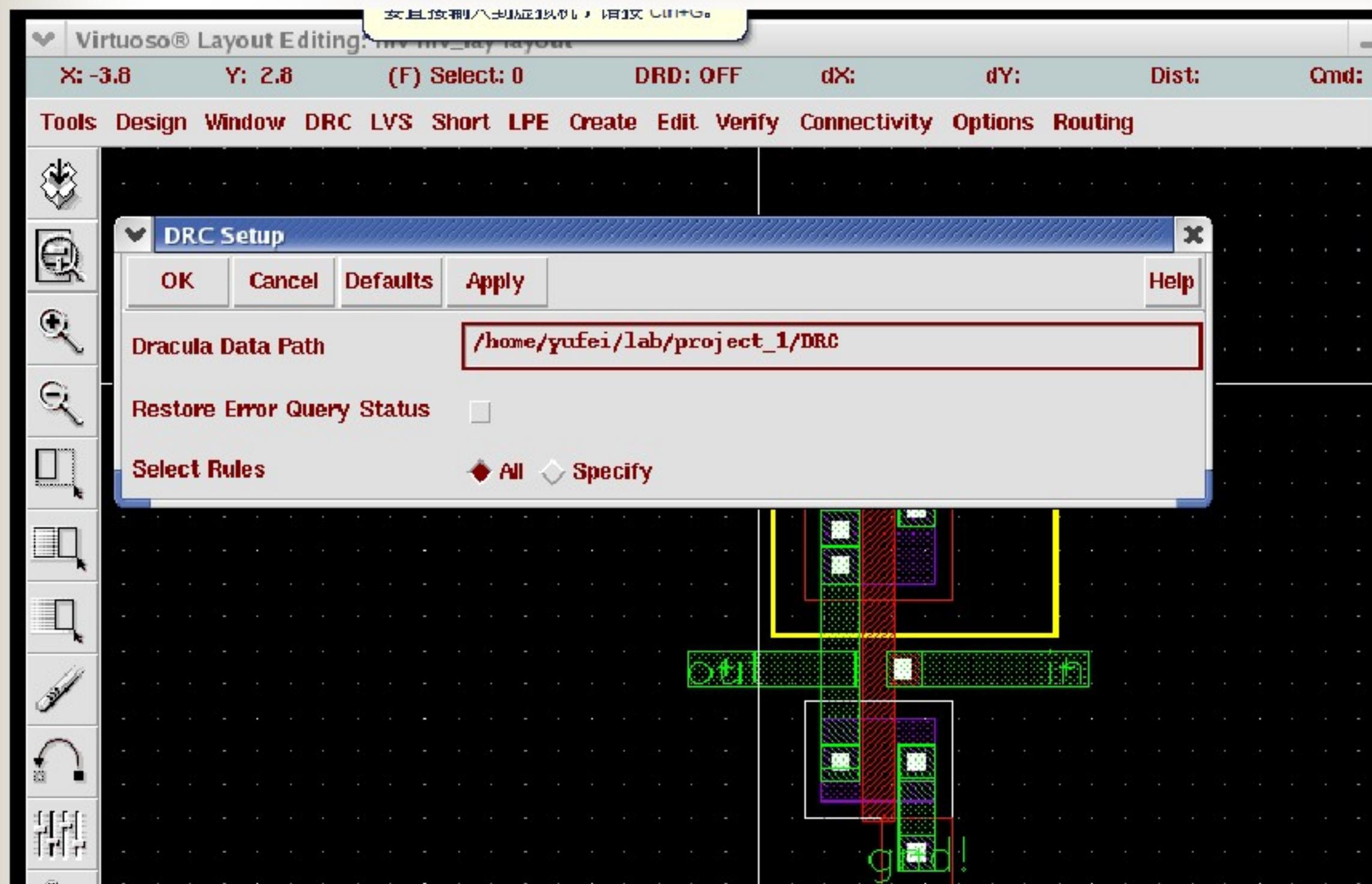
[yufei@szptyufei DRC]$ pwd
/home/yufei/lab/project_1/DRC
[yufei@szptyufei DRC]$ PDRACULA
```



* THE END OF PROGRAM *

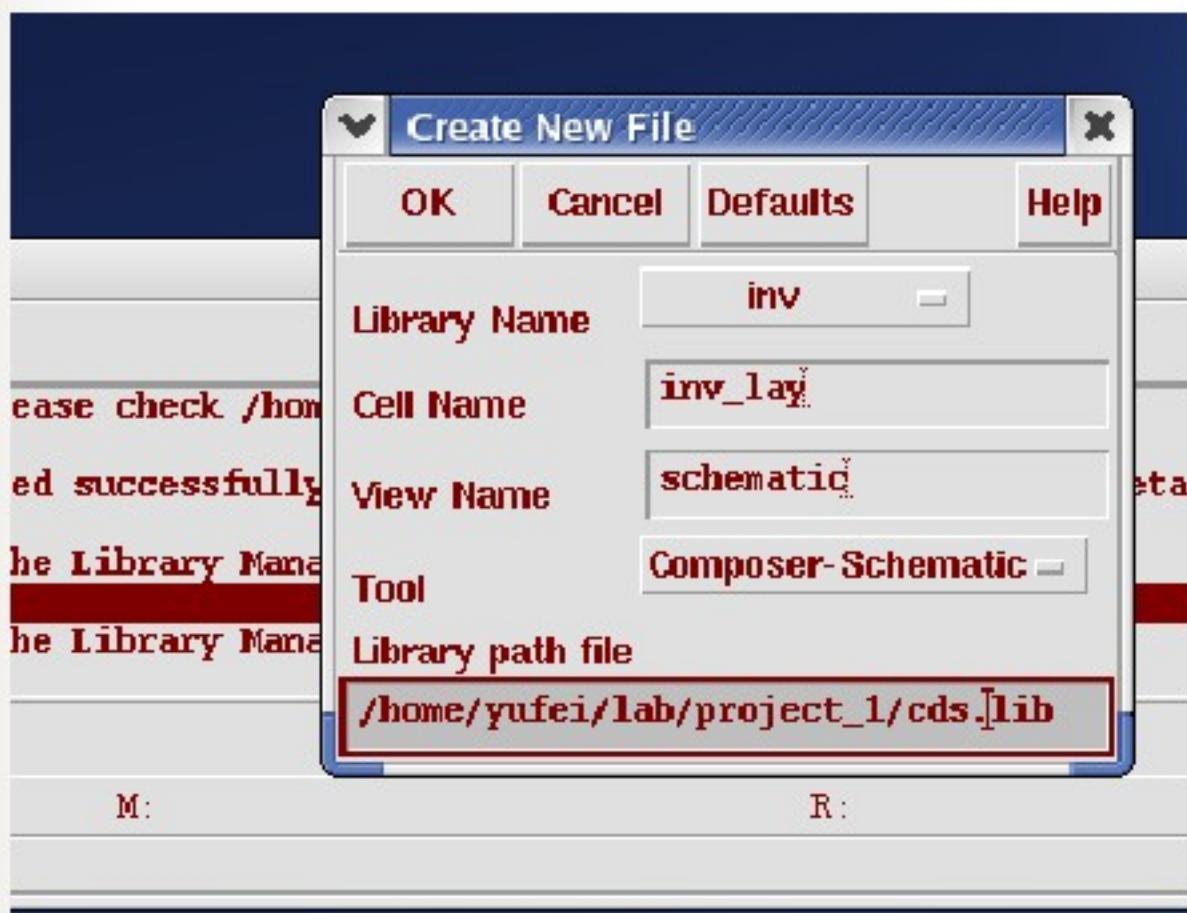
```
[yufei@szptyufei DRC]$ pwd
/home/yufei/lab/project_1/DRC
[yufei@szptyufei DRC]$ PDRACULA
*****
*/N* DRACULA3 (REV. 4.9.06-2006      / LINUX          /GENDATE: 7-JUN/2006 )
      *** ( Copyright 1995, Cadence ) ***
*/N* EXEC TIME =16:10:31      DATE =21-SEP-2008      HOSTNAME = szptyufe
*****
:/g chip.drc
```

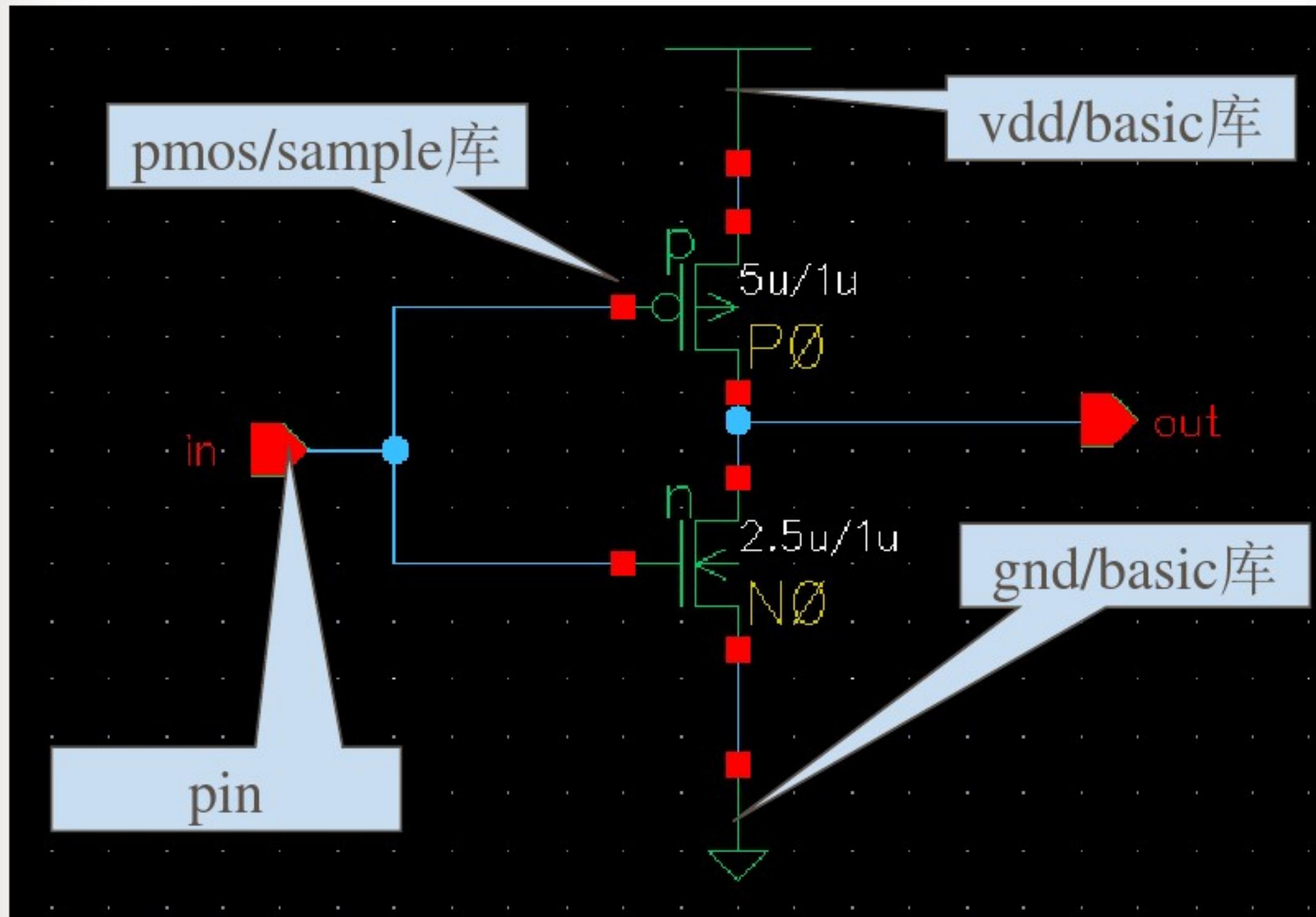
```
COUPON.DAT.LST    DEF.INP          FINFO.DAT
[yufei@szptyufei DRC]$ ll d
ls: d: No such file or directory
[yufei@szptyufei DRC]$ ls *.com
ats.com      jxgout.com     jxrun.com    jxsub.com    stopats.com
atstage.com   jxprechk.com   jxsort.com  restart.com
[yufei@szptyufei DRC]$ jxrun.com
```





画出相应的线路图,注意尺寸







版图检查-LVS (dracula)

- 1. 导出cdl，导出GDSII
- 2. LOGLVS
- 3. cir cdl_filename
- 4. con top_module_name
- 5. x
- 6. PDRACULA
- 7. /g lvs_runset_file (修改文件， GDSII文件名， 顶层模块文件名)
- 8. /f
- 9. jxrun.com
- 10. setup 路径



■ 在lvs.lvs中看报告



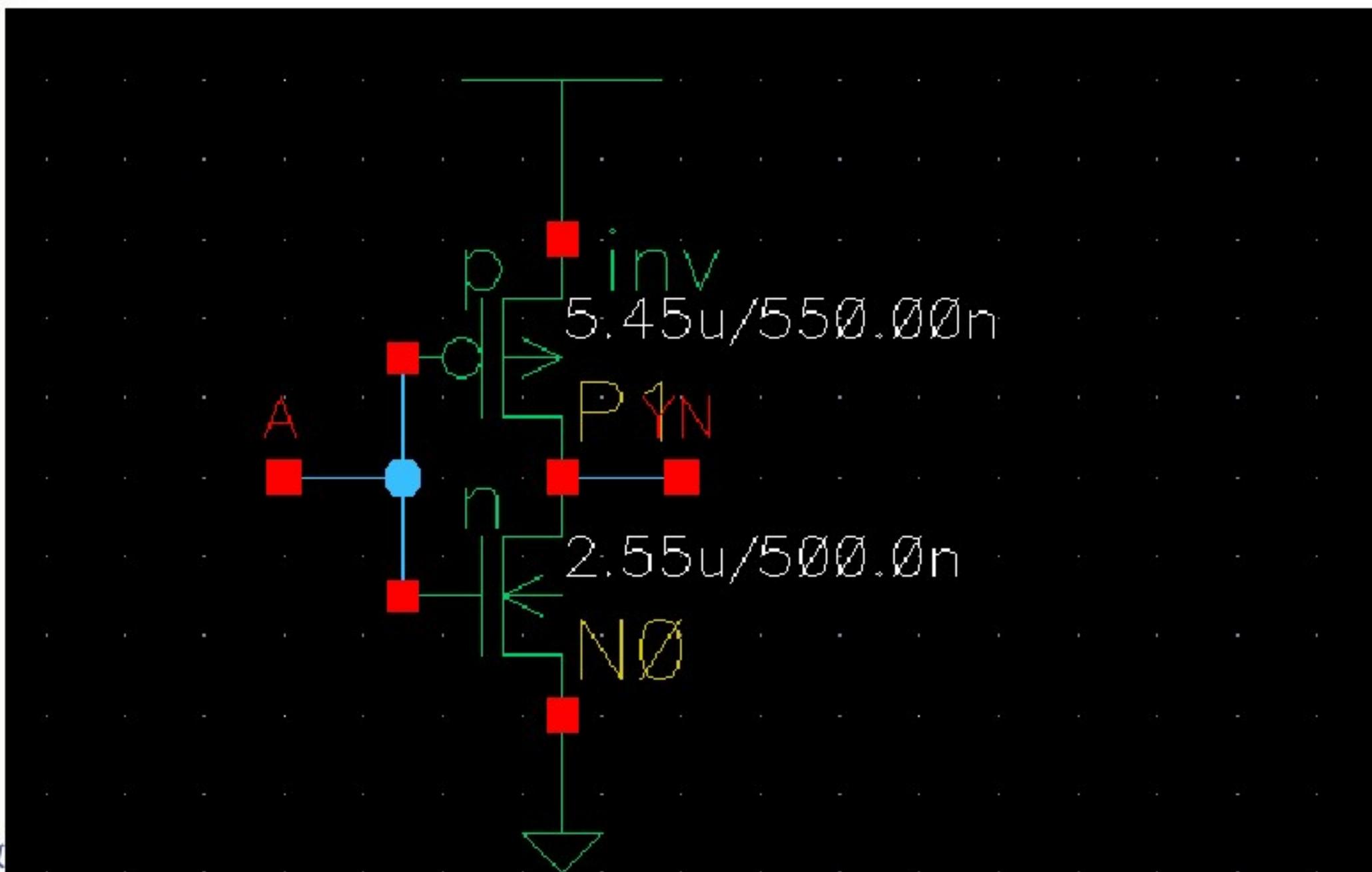
版图验证的标准

- 同时通过LVS和DRC验证
- 也就是做了任何修改之后，都要先跑DRC，再跑LVS



任务

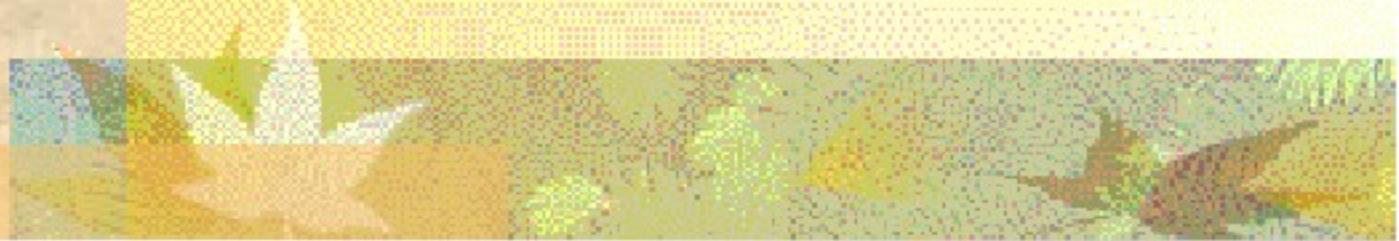
- 完成下面的反向器电路的版图完整设计：





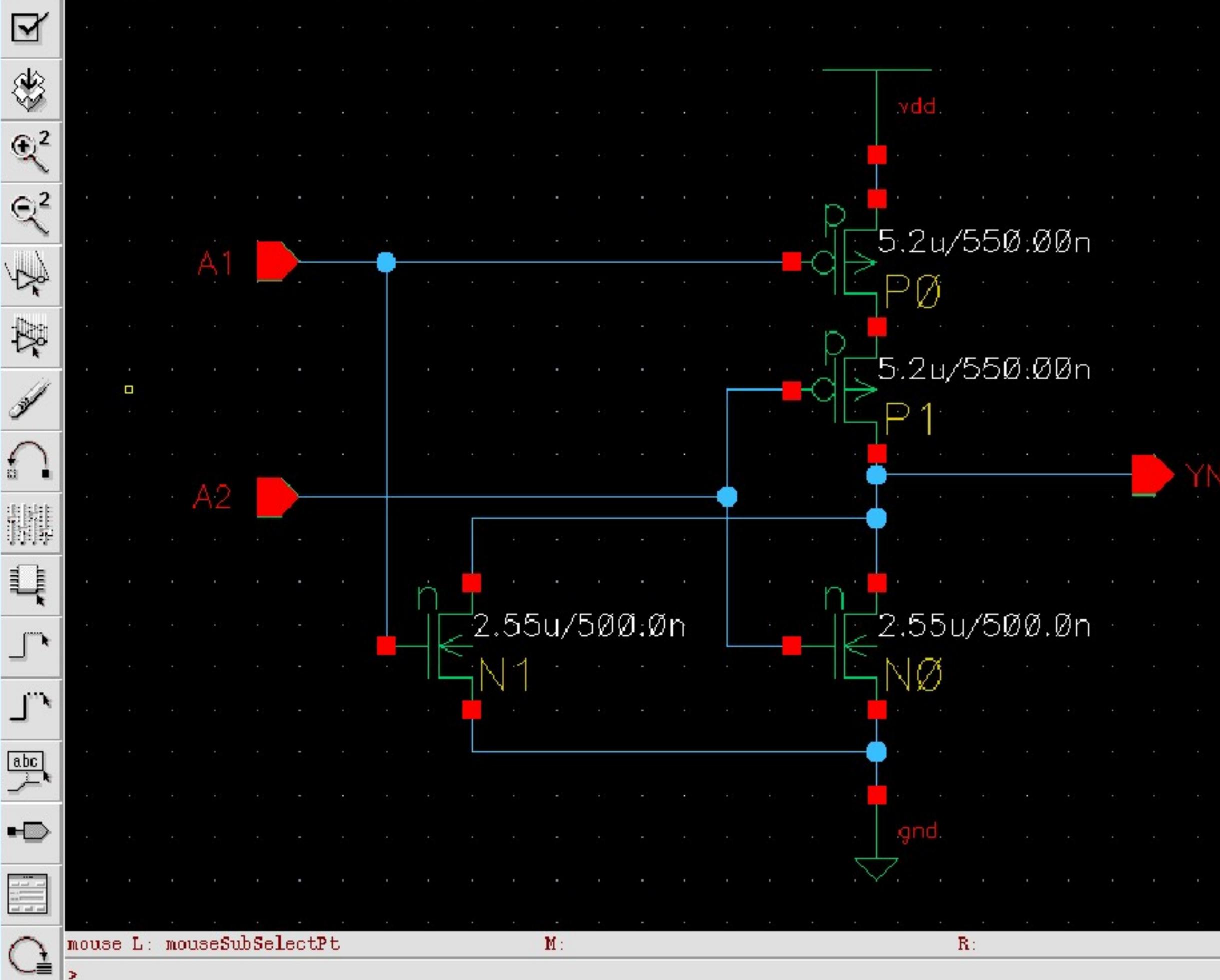
■ 任务检查方式：

在老师指定的文件夹下面建立指定的目录和文本，完成LVS和DRC以后，可以直接找教师检查登记。



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3.或非门版图设计与验证





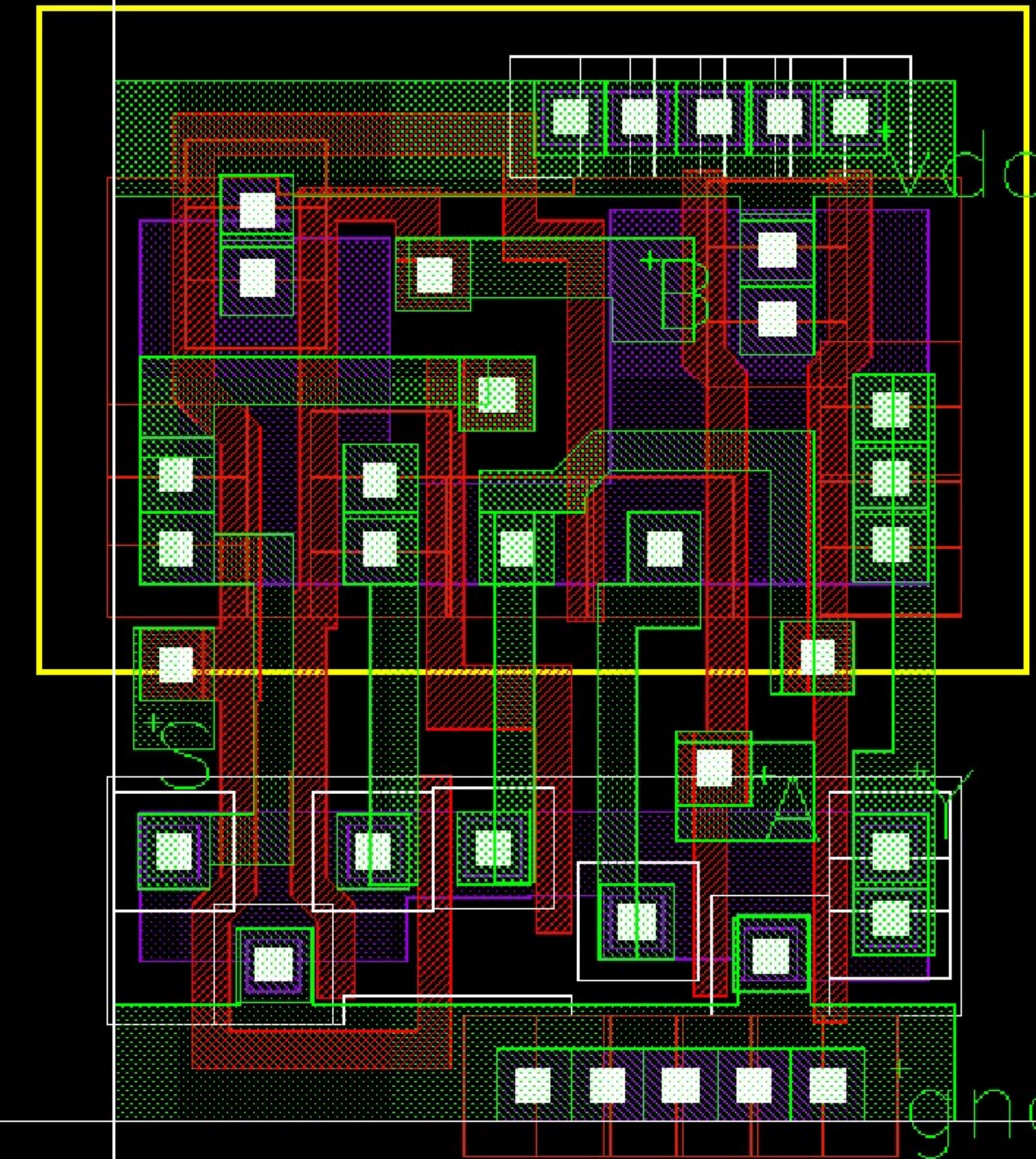
■ 任务检查方式：

在老师指定的文件夹下面建立指定的目录和文本，提交以后，可以直接找教师检查登记。



4.二输入多路选择器提图练习(w13)

- 从教师的目录拷贝lab3文件夹到自己的目录
- 打开版图文件
- 自己设计线路图（基于数字电路）
- 完成LVS即可





5.加分选做设计(w14)

- 1.DFF的设计 (***)
- 2.与非门的设计 (**)
- 3.异或门的设计 (***)
- 4.三输入多路选择器设计 (****)

设计要求：

所有NMOS采用尺寸： L=0.6um W=2um

所有PMOS采用尺寸： L=0.6um W=4um



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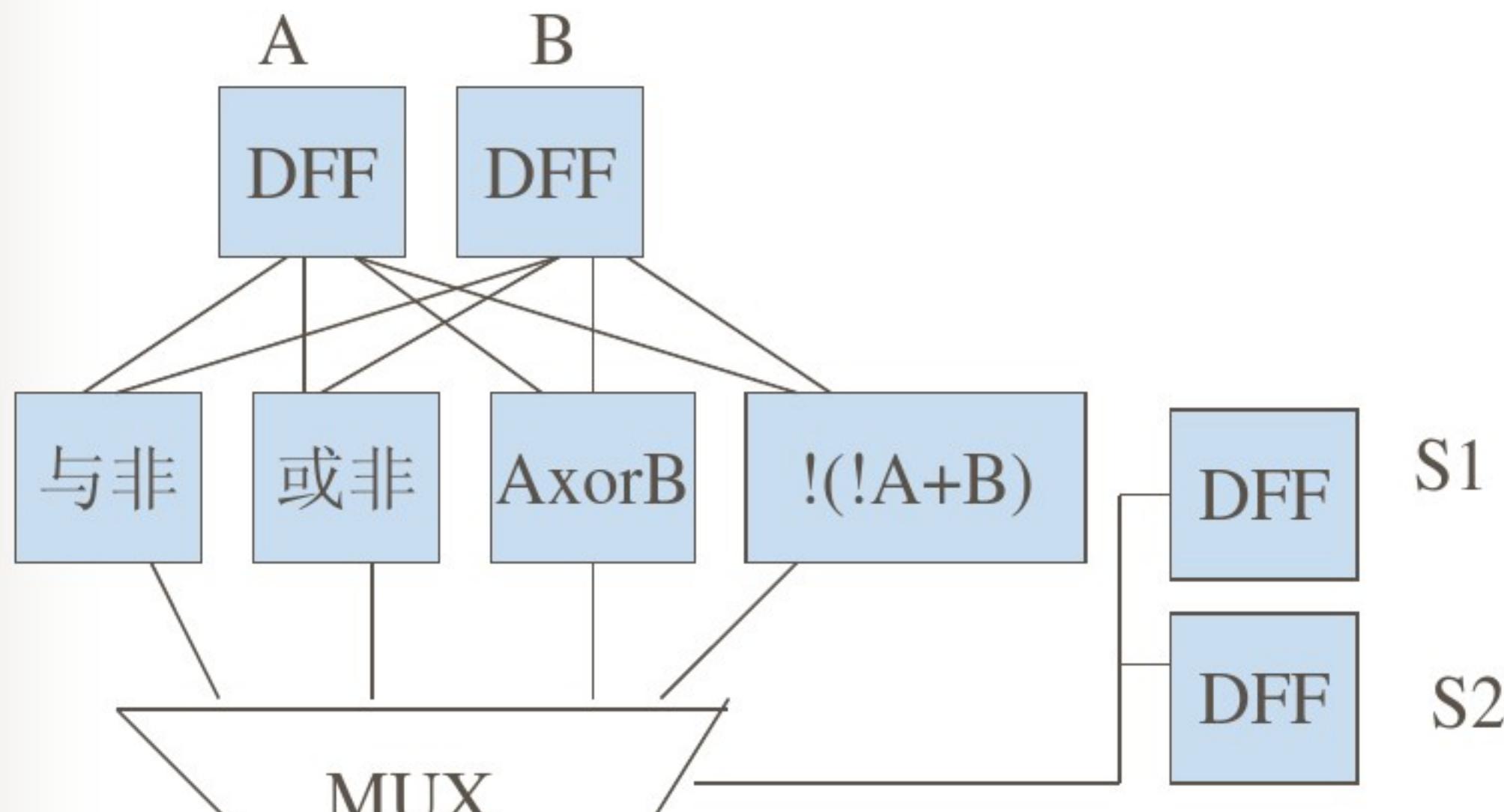
综合课程设计



(W15/W16)

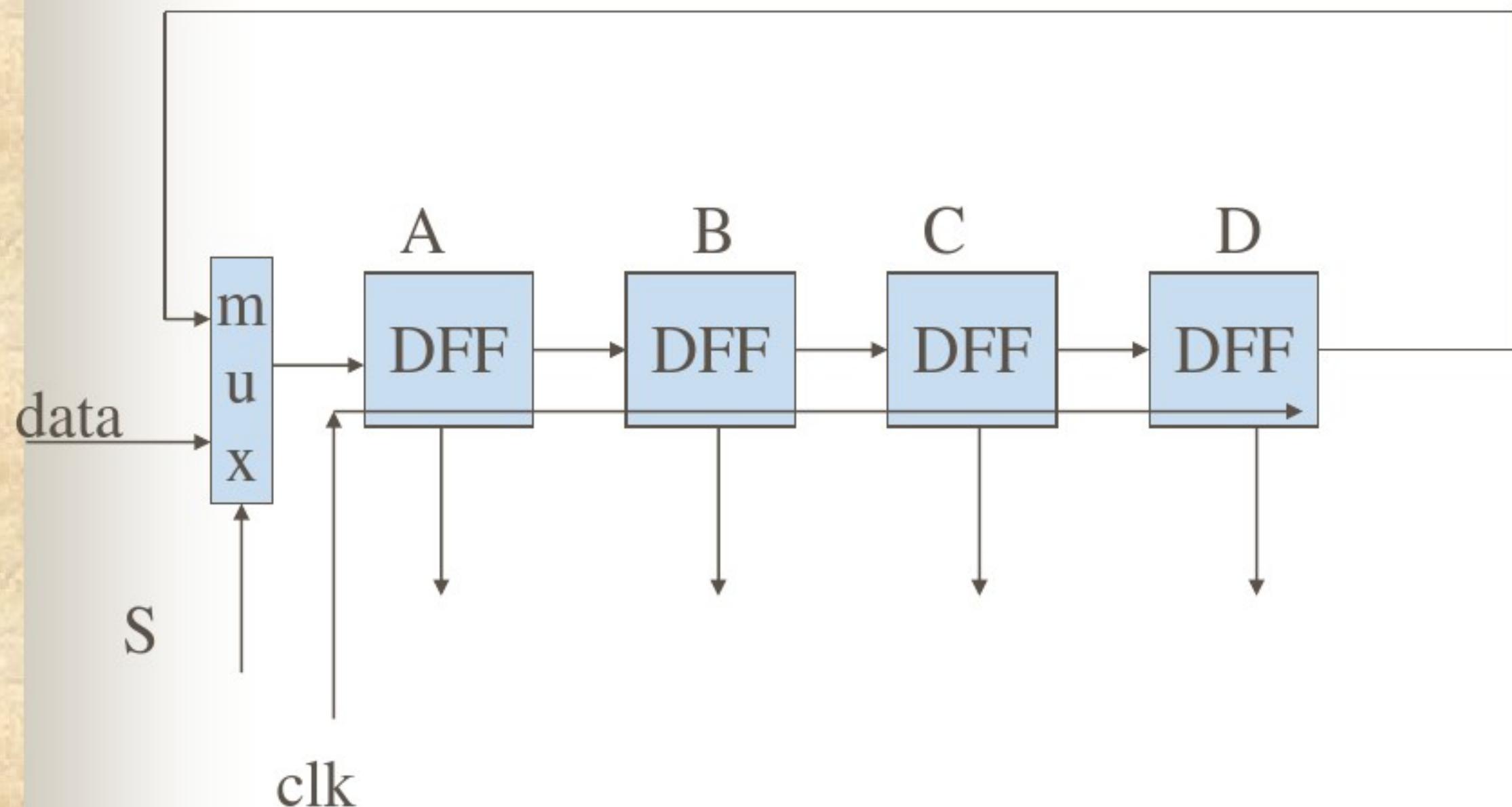


6.课程设计1：小型ALU设计



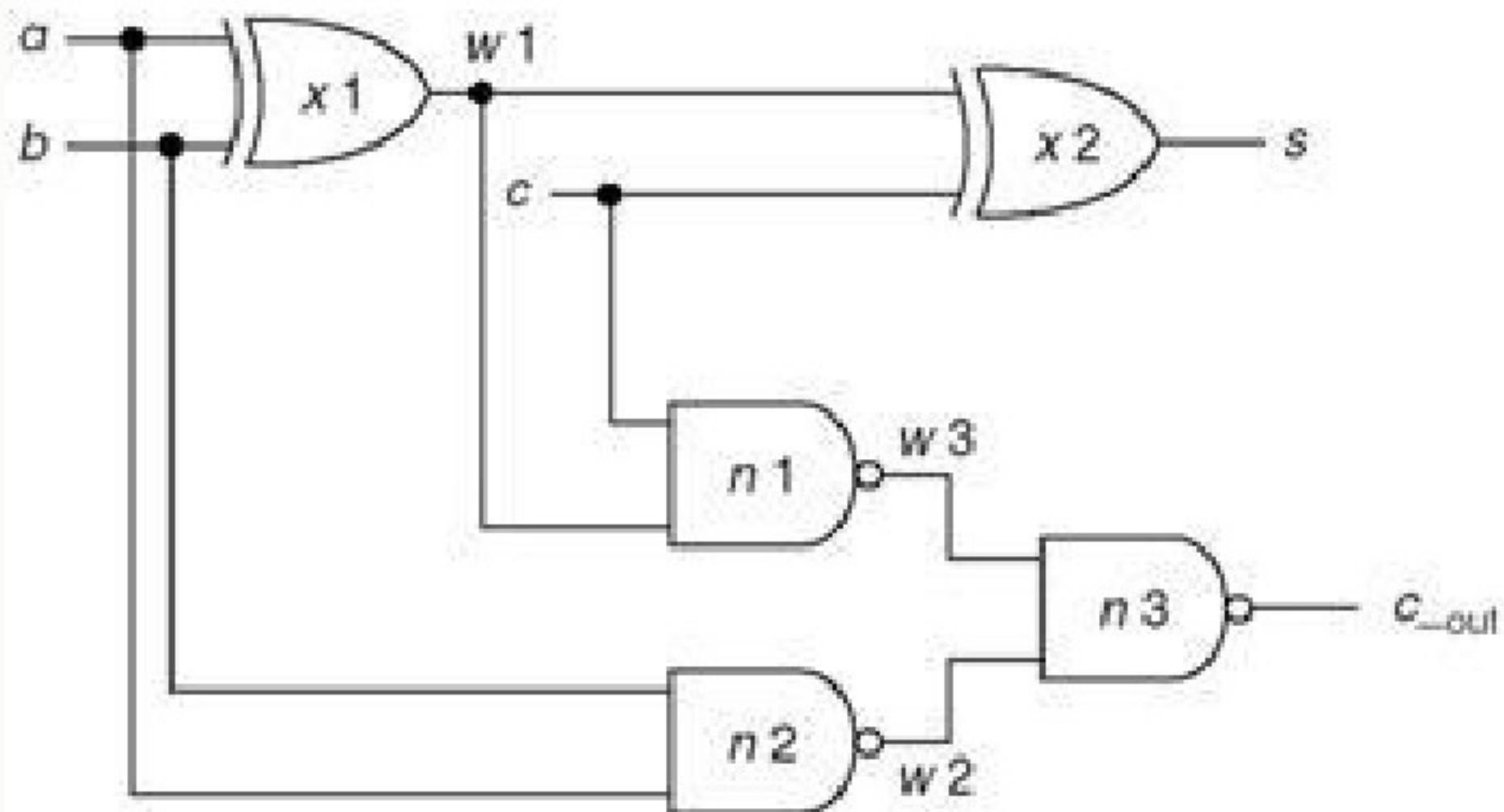


6.课程设计2：移位寄存器设计





6.课程设计3：1位全加器设计





- 从教师的目录拷贝lab4文件夹到自己的目录
- 打开线路图文件
- 自己设计版图
- 完成DRC与LVS
- 分小组完成，5-6个人一组，交一个成果即可，大家需要在一个共同路径，共同的库下面来操作



考试通知安排：

16周 周五2-4节

随堂考试\开卷考试\操作考试

微电子1班需要调课到16周五

(注意：考工是闭卷，考一个完整设计)