

Analog Circuit Design and Analysis

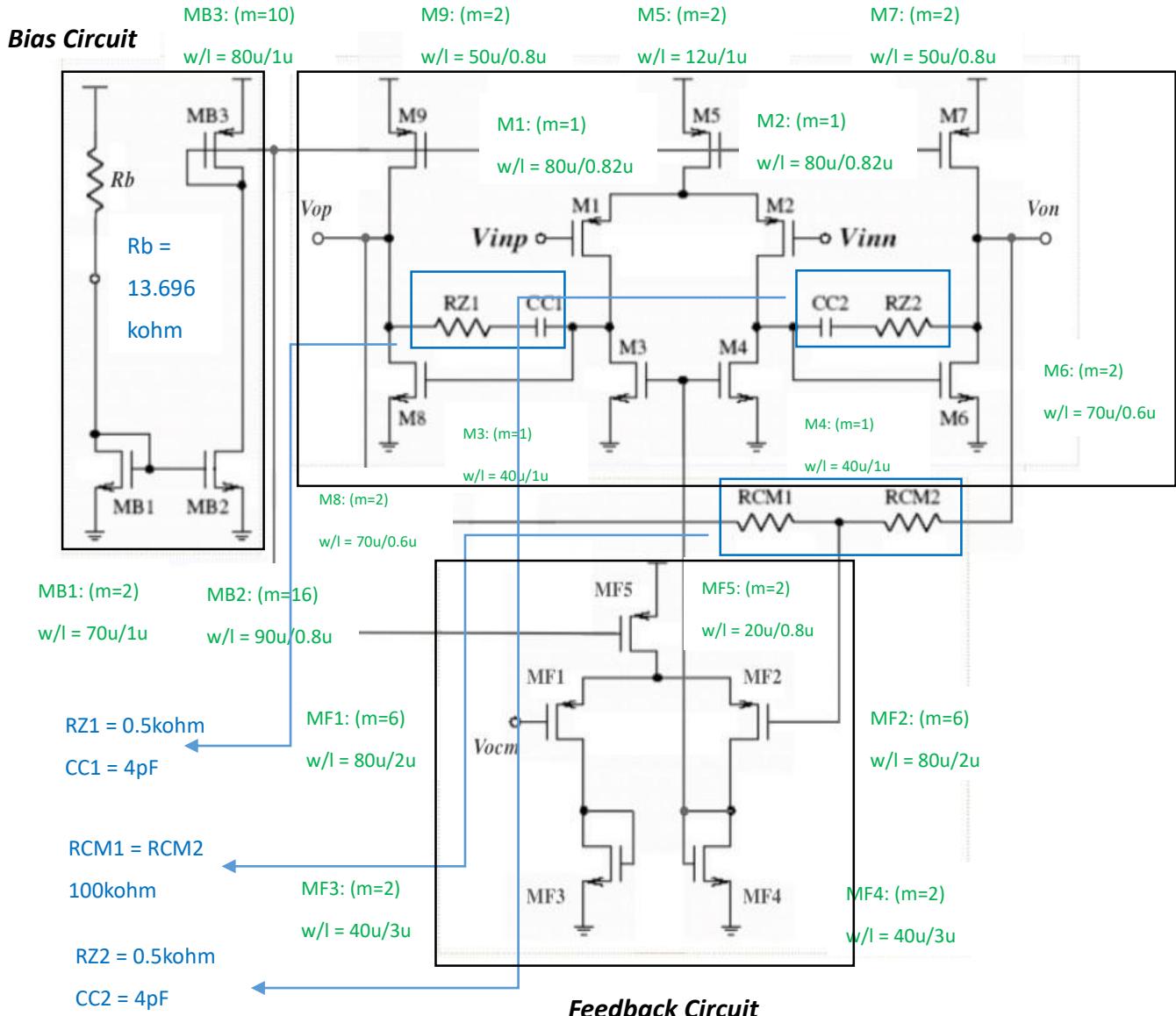
Final Project

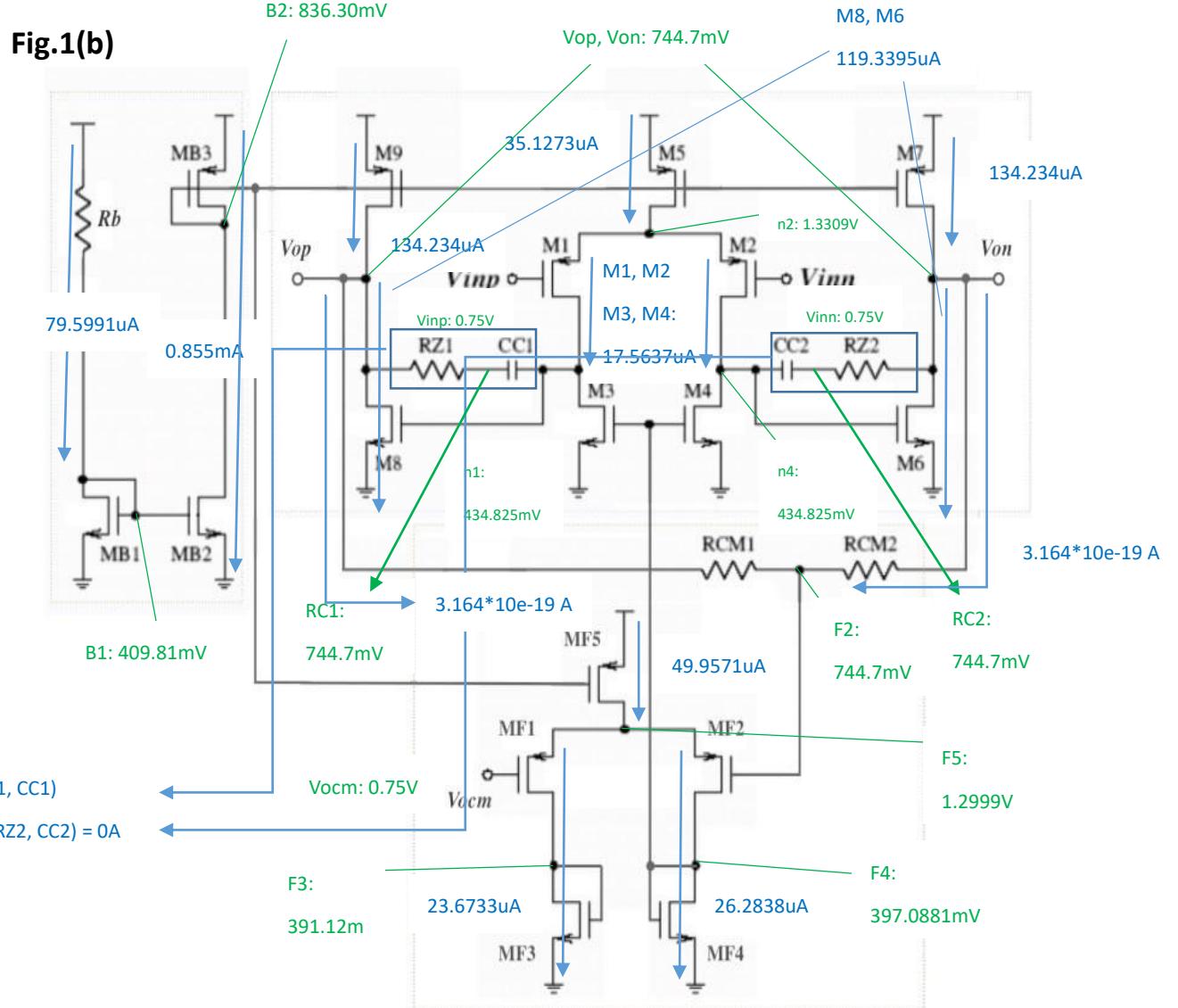
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1. Schematic

Fig.1 (a)

Amplifier Circuit





List. 1

subckt	xop	xop	xop	xop	xop	xop
element	1:mb1	1:mb2	1:mb3	1:m1	1:m2	1:m3
model	0:n_18.1	0:n_18.1	0:p_18.1	0:p_18.1	0:p_18.1	0:n_18.1
region	Saturati	Saturati	Saturati	Saturati	Saturati	Saturati
id	79.5991u	855.2452u	-855.2452u	-17.5637u	-17.5637u	17.5637u
ibs	-1.185e-20	-1.269e-19	7.882e-20	599.3919a	599.3919a	-2.643e-21
ibd	-4.1056f	-85.8995f	23.5259f	3.7757f	3.7757f	-1.2582f
vgs	409.8101m	409.8101m	-663.6974m	-580.9046m	-580.9046m	397.0881m
vds	409.8101m	836.3026m	-663.6974m	-896.0796m	-896.0796m	434.8250m
vbs	0.	0.	0.	169.0954m	169.0954m	0.
vth	385.0995m	397.5862m	-494.5452m	-545.4632m	-545.4632m	385.1256m
vdsat	74.8246m	70.9328m	-171.7373m	-85.6671m	-85.6671m	68.8820m
vod	24.7106m	12.2238m	-169.1522m	-35.4414m	-35.4414m	11.9625m
beta	43.5059m	565.3361m	57.1420m	6.9980m	6.9980m	12.4243m
gam eff	507.4459m	507.4459m	557.0846m	555.9022m	555.9022m	507.4459m
gm	1.5749m	17.5545m	8.4002m	314.8901u	314.8901u	364.3341u
gds	18.2755u	200.9301u	44.0931u	1.0175u	1.0175u	4.1475u
gmb	327.4191u	3.6016m	2.5536m	87.8304u	87.8304u	75.9181u
cdtot	195.9133f	1.8589p	917.3910f	85.7914f	85.7914f	55.6852f
cgtot	781.3105f	6.0313p	5.2090p	360.2746f	360.2746f	204.1887f
cstot	836.4926f	6.5256p	6.0839p	397.2817f	397.2817f	213.2105f
cbtot	531.1308f	4.8087p	2.9353p	241.6562f	241.6562f	151.3195f
cgs	614.1605f	4.4261p	4.5650p	285.1917f	285.1917f	152.0172f
cgd	51.0705f	531.2864f	288.5002f	28.7115f	28.7115f	14.7190f

subckt	xop	xop	xop	xop	xop	xop
element	1:m4	1:m5	1:m6	1:m7	1:m8	1:m9
model	0:n_18.1	0:p_18.1	0:n_18.1	0:p_18.1	0:n_18.1	0:p_18.1
region	Saturati	Saturati	Saturati	Saturati	Saturati	Saturati
id	17.5637u	-35.1273u	119.3395u	-134.2335u	119.3395u	-134.2335u
ibs	-2.643e-21	3.465e-21	-1.776e-20	1.246e-20	-1.776e-20	1.246e-20
ibd	-1.2582f	288.6464a	-7.4607f	3.3715f	-7.4607f	3.3715f
vgs	397.0881m	-663.6974m	434.8250m	-663.6974m	434.8250m	-663.6974m
vds	434.8250m	-169.0954m	744.7003m	-755.2997m	744.7003m	-755.2997m
vbs	0.	0.	0.	0.	0.	0.
vth	385.1256m	-494.6075m	421.9585m	-497.2496m	421.9585m	-497.2496m
vdsat	68.8820m	-172.5444m	73.9961m	-172.3202m	73.9961m	-172.3202m
vod	11.9625m	-169.0899m	12.8665m	-166.4478m	12.8665m	-166.4478m
beta	12.4243m	2.5431m	74.5932m	8.9707m	74.5932m	8.9707m
gam eff	507.4459m	557.0846m	507.4460m	557.0846m	507.4460m	557.0846m
gm	364.3341u	318.3569u	2.4265m	1.3301m	2.4265m	1.3301m
gds	4.1475u	46.7249u	30.3856u	7.7060u	30.3856u	7.7060u
gmb	75.9181u	97.7319u	487.2257u	402.1827u	487.2257u	402.1827u
cdtot	55.6852f	66.5804f	183.4788f	112.7220f	183.4788f	112.7220f
cgtot	204.1887f	241.3707f	460.4794f	525.3640f	460.4794f	525.3640f
cstot	213.2105f	273.2772f	524.8550f	622.8060f	524.8550f	622.8060f
cbtot	151.3195f	139.3679f	422.7629f	323.5857f	422.7629f	323.5857f
cgs	152.0172f	206.0607f	331.3815f	454.2645f	331.3815f	454.2645f
cgd	14.7190f	21.1690f	51.8670f	35.9646f	51.8670f	35.9646f

subckt	xop	xop	xop	xop	xop
element	1:mf1	1:mf2	1:mf3	1:mf4	1:mf5
model	0:p_18.1	0:p_18.1	0:n_18.1	0:n_18.1	0:p_18.1
region	Saturati	Saturati	Saturati	Saturati	Saturati
id	-23.6733u	-26.2838u	23.6733u	26.2838u	-49.9571u
ibs	4.2567f	4.2567f	-3.562e-21	-3.955e-21	4.775e-21
ibd	23.5838f	23.4569f	-2.2635f	-2.2980f	367.8986a
vgs	-549.8541m	-555.1538m	391.1200m	397.0881m	-663.6974m
vds	-908.7341m	-902.7660m	391.1200m	397.0881m	-200.1459m
vbs	200.1459m	200.1459m	0.	0.	0.
vth	-540.8759m	-540.8759m	335.5464m	335.5227m	-497.2468m
vdsat	-69.1788m	-71.4613m	85.0206m	88.3590m	-172.6732m
vod	-8.9782m	-14.2779m	55.5736m	61.5654m	-166.4506m
beta	17.0769m	17.0628m	8.0292m	8.0316m	3.5703m
gam eff	555.6955m	555.6955m	507.4459m	507.4459m	557.0846m
gm	472.0302u	514.9824u	417.8099u	451.0849u	476.3443u
gds	617.3768n	679.8549n	2.9267u	3.1765u	32.7139u
gmb	132.0689u	144.0588u	86.0171u	92.6880u	144.5361u
cdtot	511.7867f	512.2241f	113.8405f	113.7977f	60.1992f
cgtot	4.3428p	4.5067p	1.4667p	1.4901p	213.6452f
cstot	4.1917p	4.4371p	1.5058p	1.5375p	248.5543f
cbtot	2.4981p	2.5044p	586.4076f	586.2834f	136.3657f
cgs	3.2371p	3.4480p	1.2740p	1.3028p	182.4553f
cgd	172.2783f	172.2909f	27.6764f	27.6270f	18.0811f

2. Spice Code

*** Final ***

.subckt my_op vinp vinn vdd vss vop von vocm

*** Bias Circuit ***

MB1 B1 B1 vss vss n_18 w = 70u l = 1u m = 2

MB2 B2 B1 vss vss n_18 w = 90u l = 0.8u m = 16

MB3 B2 B2 vdd vdd p_18 w = 80u l = 1u m = 10

Rb VDD B1 13.696k

*** Amplifier Circuit ***

M1 n1 vinp n2 vdd p_18 w = 80u l = 0.82u m = 1

M2 n4 vinn n2 vdd p_18 w = 80u l = 0.82u m = 1

M3 n1 F4 vss vss n_18 w = 40u l = 1u m = 1

M4 n4 F4 vss vss n_18 w = 40u l = 1u m = 1

M5 n2 B2 vdd vdd p_18 w = 12u l = 1u m = 3

M6 Von n4 vss vss n_18 w = 70u l = 0.6u m = 2

M7 Von B2 vdd vdd p_18 w = 50u l = 0.8u m = 2

M8 Vop n1 vss vss n_18 w = 70u l = 0.6u m = 2

M9 Vop B2 vdd vdd p_18 w = 50u l = 0.8u m = 2

*** Feedback Circuit ***

MF1 F3 vocm F5 vdd p_18 w = 80u l = 2u m = 6

MF2 F4 F2 F5 vdd p_18 w = 80u l = 2u m = 6

MF3 F3 F3 vss vss n_18 w = 40u l = 3u m = 2

MF4 F4 F4 vss vss n_18 w = 40u l = 3u m = 2

MF5 F5 B2 vdd vdd p_18 w = 20u l = 0.8u m = 2

*** passive component ***

RZ1 Vop rc1 0.5k

RZ2 rc2 Von 0.5k

RCM1 Vop F2 100k

RCM2 F2 Von 100k

CC1 rc1 n1 4p

CC2 n4 rc2 4p

.ends

3. Simulation

3.1 Open-loop differential mode AV response

Fig. 3.1(a)

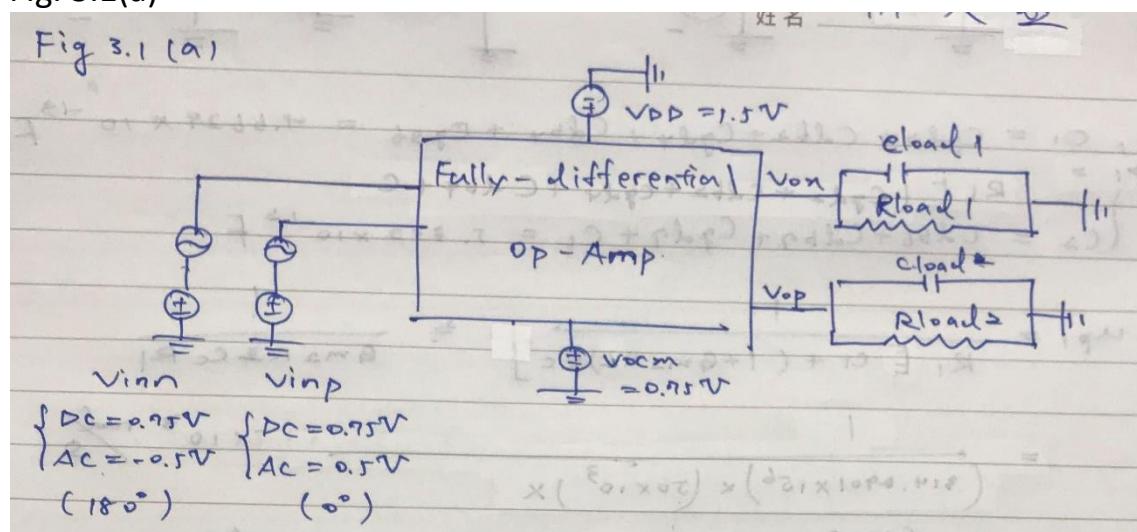


Fig. 3.1(b)

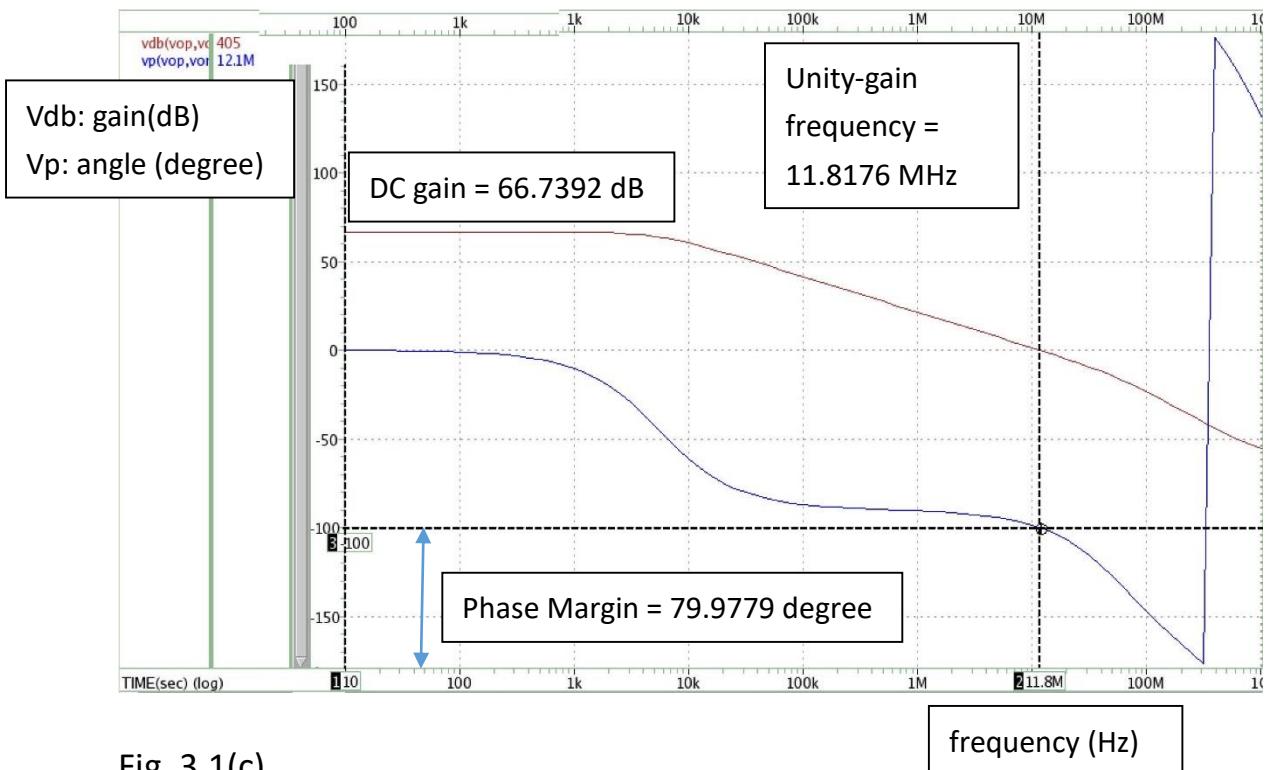


Fig. 3.1(c)

poles (rad/sec)		poles (hertz)	
real	imag	real	imag
-34.5042k	0.	-5.49151k	0.
-1.89027x	-17.0656x	-300.845k	-2.71607x
-1.89027x	17.0656x	-300.845k	2.71607x
-142.101x	0.	-22.6161x	0.
-194.153x	0.	-30.9003x	0.
-202.172x	0.	-32.1767x	0.
-208.162x	0.	-33.1300x	0.
-423.519x	0.	-67.4051x	0.
-423.999x	0.	-67.4815x	0.
-987.976x	0.	-157.241x	0.

Output first 10 Zeros, (total 20)

Use .option pz_num = NUM to control output number, (default:10)

zeros (rad/sec)		zeros (hertz)	
real	imag	real	imag
-1.93986x	16.6123x	-308.739k	2.64393x
-1.93986x	-16.6123x	-308.739k	-2.64393x
-1.94580x	-16.6056x	-309.684k	-2.64287x
-1.94580x	16.6056x	-309.684k	2.64287x
-142.171x	0.	-22.6272x	0.
-193.810x	0.	-30.8459x	0.
-202.339x	-406.688	-32.2033x	-64.7264
-202.339x	406.688	-32.2033x	64.7264
-208.170x	0.	-33.1313x	0.
-423.514x	8.12843k	-67.4043x	1.29368k

Dis. 3.1(d)

gain:

$$\left\{ \begin{array}{l} R_{load} = 50k\Omega \\ g_{m2} = 314.89 \times 10^{-6}, \quad g_{m6} = 2.4265 \times 10^{-3} \\ r_{o2} // r_{o4} = \frac{1}{g_{ds2}} // \frac{1}{g_{ds4}} \\ = (9.828 \times 10^5 \Omega) // (2.411 \times 10^5 \Omega) \\ = 1.956 \times 10^5 \Omega \\ r_{o6} // r_{o7} = \frac{1}{g_{ds6}} // \frac{1}{g_{ds7}} // R_{load} \\ // R_{load} = (1.2977 \times 10^5 \Omega) // (3.291 \times 10^4 \Omega) // (5 \times 10^4 \Omega) \\ = 1.7214 \times 10^4 \Omega \end{array} \right.$$

$$\therefore \left\{ \begin{array}{l} A_{stage1} = -g_{m2} \cdot (r_{o2} // r_{o4}) = -60.9627 \\ A_{stage2} = -g_{m6} \cdot (r_{o6} // r_{o7} // R_{load}) = -41.7698 \end{array} \right.$$

$$\therefore \left\{ \begin{array}{l} A = A_{stage1} \cdot A_{stage2} = 2546.4 \\ \text{difference} = 17.21 \% \end{array} \right. \leftrightarrow \text{sim: } 2192.5$$

The error of calculation gain might result from the body effect we ignore, if we take body effect into consideration, then the result might be expected to be more accurate. In addition, the error may also result from the rounding error.

frequency response:

$$\Rightarrow C_1 = C_{d2} + C_{d6} + C_{d4} + C_{d8} + C_{ds6} = 4.6629 \times 10^{-13} F$$

$$\Rightarrow C_2 = C_{d6} + C_{d7} + C_{ds7} + C_L = 5.372 \times 10^{-13} F$$

$$\Rightarrow w_{p1} = \frac{1}{R_1 [C_1 + (1+G_{m2}R_2)C_c]} = \frac{1}{G_{m2}R_2 C_c R_1} = 32.815 \times 10^3 rad/s$$

$$w_{p2} = \frac{G_{m2}C_c}{C_1 C_2 + C_c (C_1 + C_2)} = 1.152 \times 10^6 rad/s$$

$$w_{z1} = \frac{1}{C_2 (\frac{G_{m2}}{R_2} + R)} = 1.392 \times 10^6 rad/s$$

$$\Rightarrow f_{p1} = 5.143 \times 10^3 Hz$$

$$f_{p2} = 1.034 \times 10^3 Hz$$

$$f_{z1} = 2.215 \times 10^5 Hz$$

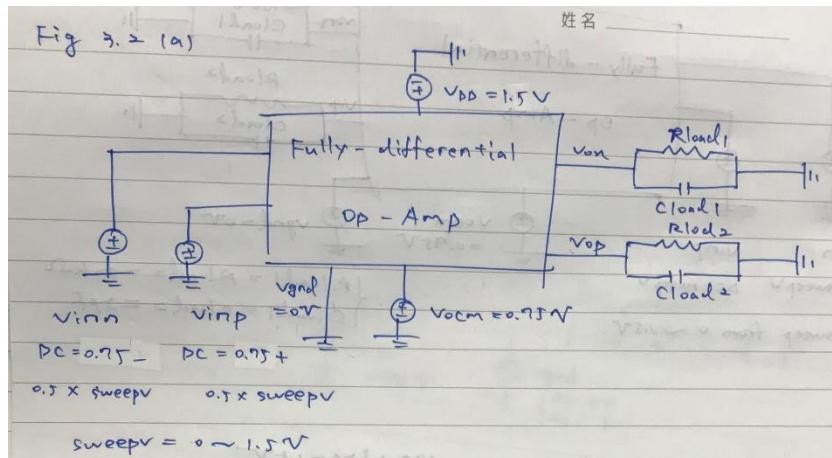
transfer function:

$$\frac{V_o}{V_{id}} = \frac{G_{m1}(G_{m2} - sC_c)R_1R_2}{1 + s[C_1R_1 + C_2R_2 + C_c(G_{m2}R_1R_2 + R_1 + R_2)] + s^2 [C_1C_2 + C_c(C_1 + C_2)]R_1R_2}$$

The final result is quite different from the actual result, I consider that it might result from the calculating error and the effective resistance and effective capacitance I might ignore. Consequently, the final error error might be a little bit large. Most importantly, we ignore the imaginary part, so the result can not be the accurate value.

3.2 Open-loop differential mode DC sweep

Fig3.2(a)

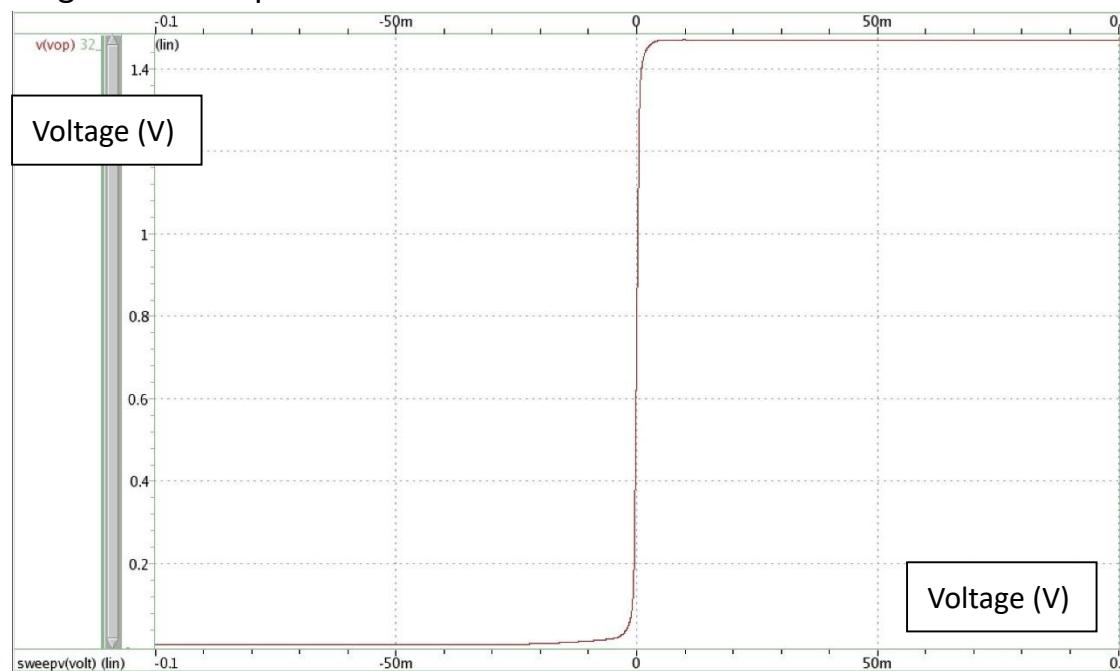


$$R_{load1} = R_{load2} = 50\text{kohm}$$

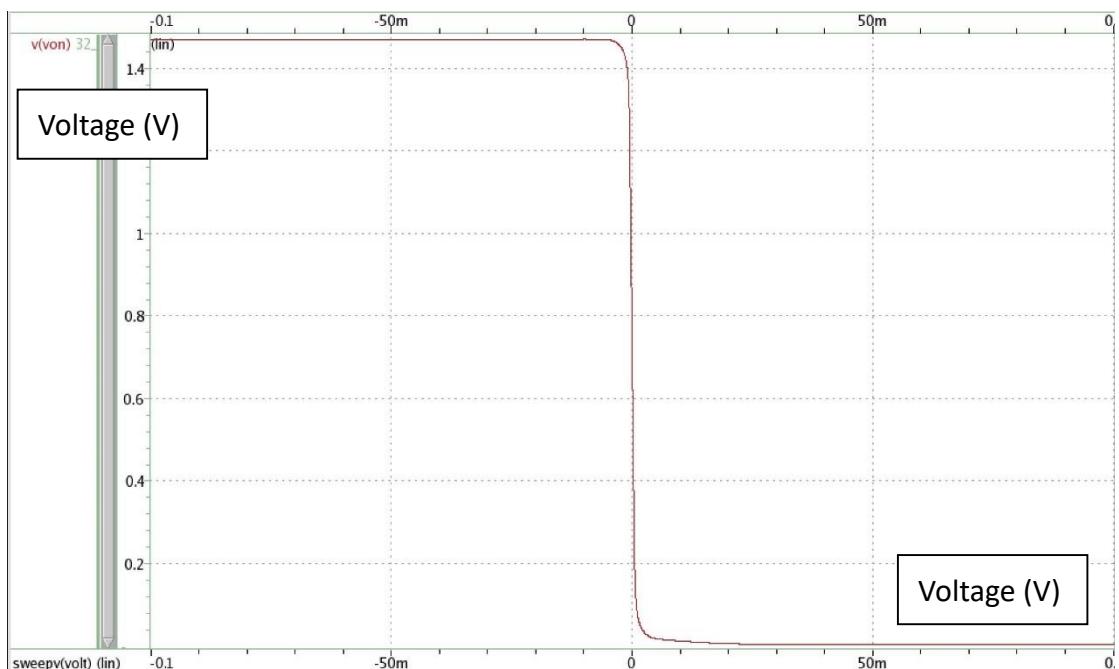
$$C_{load1} = C_{load2} = 5\text{pF}$$

Fig. 3.2(b)

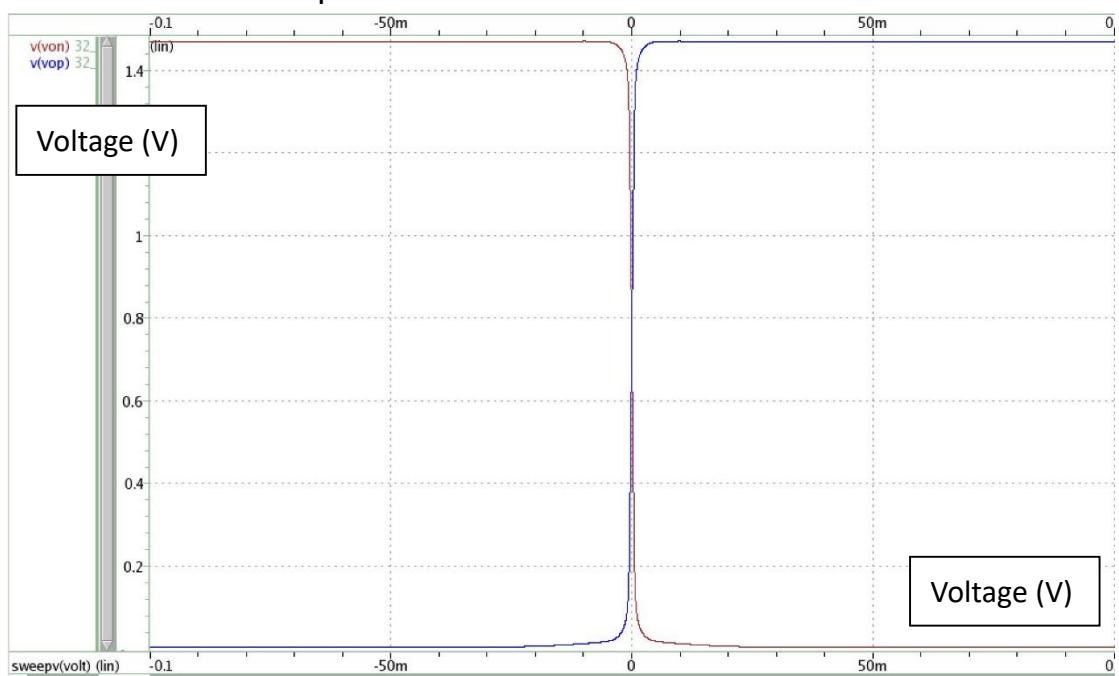
Single-ended vop:



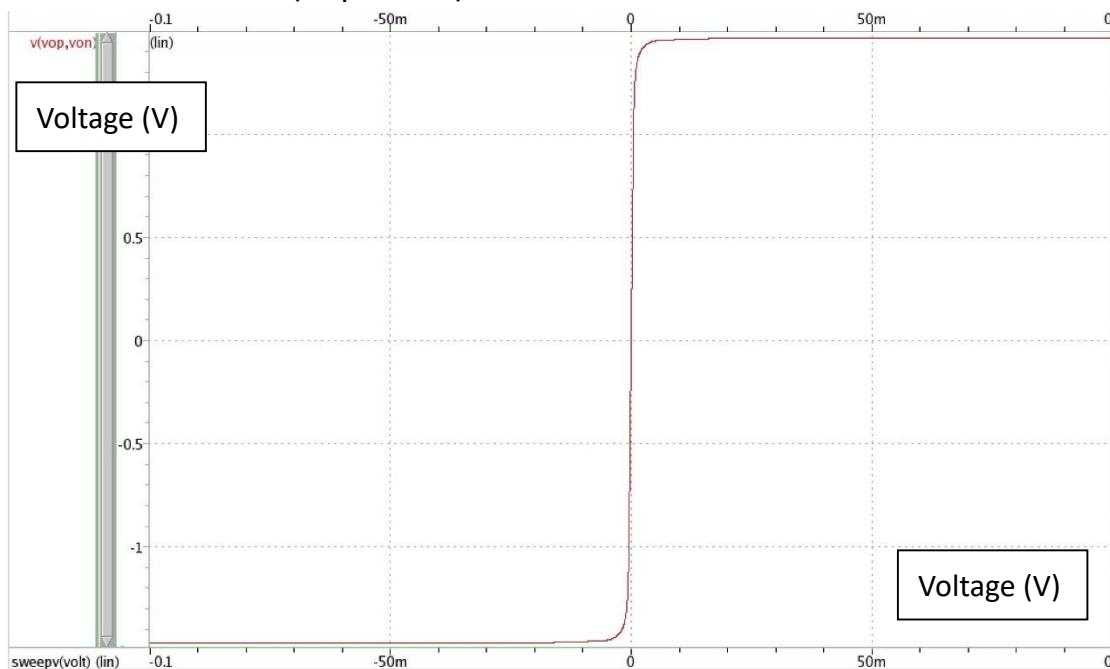
Single-ended von:



Combination of two plots:



Differential result: $(V_{op} - V_{on})$



By the “equation builder”, I try to find the voltage gain by finding the slope in differential plot when $x = 0$. The result is shown below:

Mixed-Signal Equation Builder@ws47				
	Name	Equation (click here to edit min/max)	Target	Result
<input type="checkbox"/>	slope(v(vop,von),0)		D0/32_dc-dm_v2.sw0	2172.46 X
	Input new equation here			

The .lis result is 2172.5, and the DC slope is 2172.46. Difference is equal to 0%. We could find that they are exactly same!

3.3 Open-loop common mode AC response

Fig. 3.3(a)

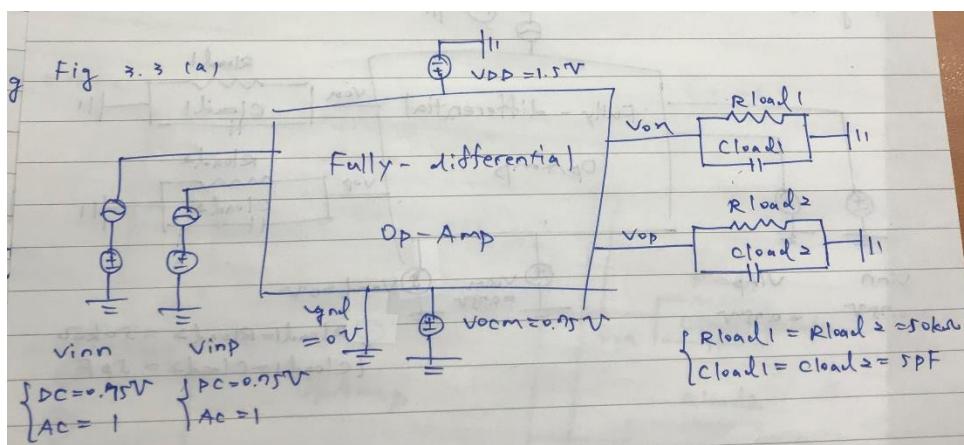
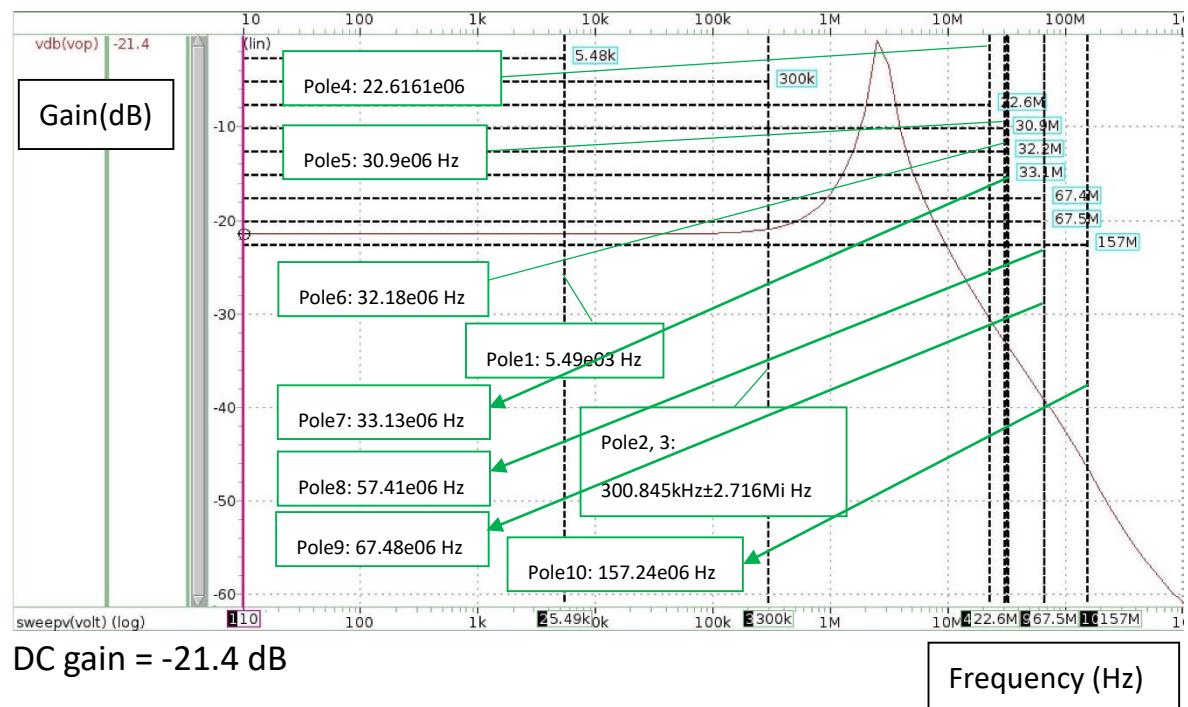


Fig. 3.3(b)

The poles and zeros are exactly as same as the ones of differential mode, them the poles and zeros are shown in the plot below:

● Poles



● Zero

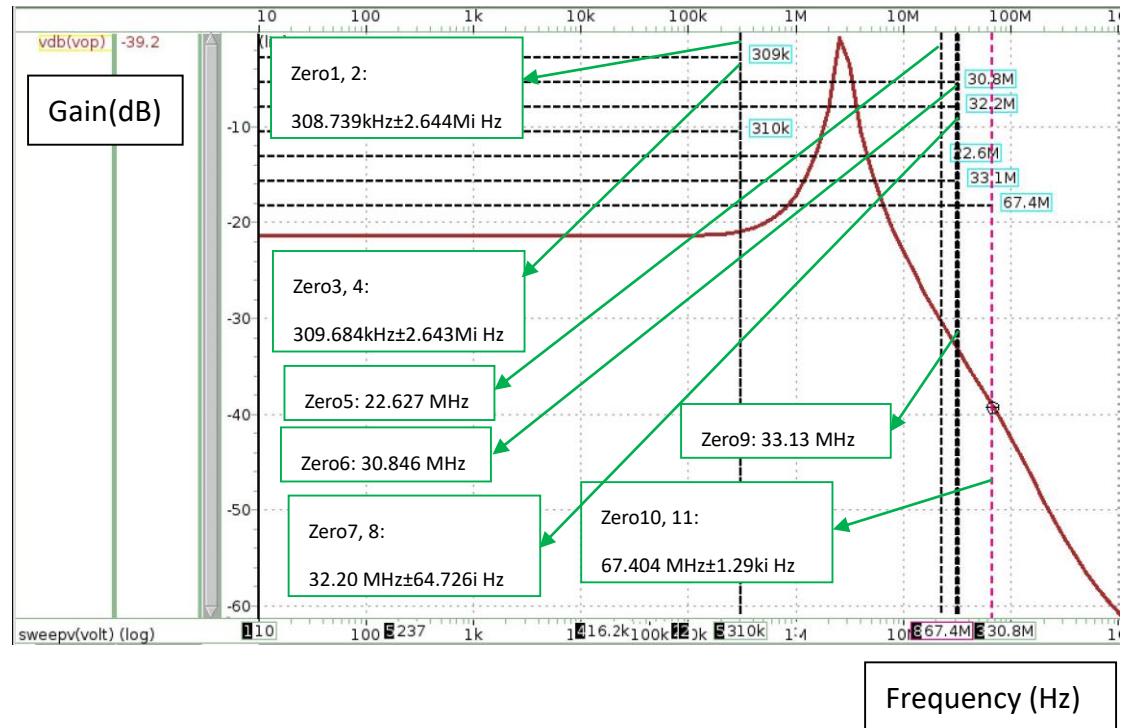


Fig. 3.3(c)

Output first 10 Poles, (total 13)
Use .option pz_num = NUM to control output number, (default:10)

poles (rad/sec)		poles (hertz)	
real	imag	real	imag
-34.5042k	0.	-5.49151k	0.
-1.89027x	-17.0656x	-300.845k	-2.71607x
-1.89027x	17.0656x	-300.845k	2.71607x
-142.101x	0.	-22.6161x	0.
-194.153x	0.	-30.9003x	0.
-202.172x	0.	-32.1767x	0.
-208.162x	0.	-33.1300x	0.
-423.519x	0.	-67.4051x	0.
-423.999x	0.	-67.4815x	0.
-987.976x	0.	-157.241x	0.

Output first 10 Zeros, (total 20)
Use .option pz_num = NUM to control output number, (default:10)

zeros (rad/sec)		zeros (hertz)	
real	imag	real	imag
-1.93986x	16.6123x	-308.739k	2.64393x
-1.93986x	-16.6123x	-308.739k	-2.64393x
-1.94580x	-16.6056x	-309.684k	-2.64287x
-1.94580x	16.6056x	-309.684k	2.64287x
-142.171x	0.	-22.6272x	0.
-193.810x	0.	-30.8459x	0.
-202.339x	-406.688	-32.2033x	-64.7264
-202.339x	406.688	-32.2033x	64.7264
-208.170x	0.	-33.1313x	0.
-423.514x	8.12843k	-67.4043x	1.29368k

Dis. 3.3(d)

Since the poles and zeros are as same as the ones in 3.1(c) (differential mode), so I utilize the same method to calculate the poles and zeros.
The calculation is shown in next page.

frequency response:

$$\Rightarrow C_1 = C_{gd2} + C_{db2} + C_{gd4} + C_{db4} + C_{gg6} = 4.6629 \times 10^{-13} F$$

$$C_2 = C_{db6} + C_{db7} + C_{gd7} + C_L = 5.372 \times 10^{-13} F$$

$$\Rightarrow w_{p1} = \frac{1}{R_1 [C_1 + (1+G_m2)C_C]} = \frac{1}{G_m2 R_2 C_C R_1} = 32.315 \times 10^3 \text{ rad/s}$$

$$w_{p2} = \frac{G_m2 C_C}{C_1 C_2 + C_C (C_1 + C_2)} = 1.152 \times 10^6 \text{ rad/s}$$

$$w_{z1} = \frac{1}{C_C (\frac{1}{G_m2} - R)} = 1.392 \times 10^6 \text{ rad/s}$$

$$\Rightarrow f_{p1} = 5.143 \times 10^3 \text{ Hz}$$

$$f_{p2} = 1.858 \times 10^5 \text{ Hz}$$

$$f_{z1} = 2.215 \times 10^5 \text{ Hz}$$

transfer function:

$$\frac{V_o}{V_{id}} = \frac{G_m2 (G_m2 - s C_C) R_1 R_2}{1 + s[C_1 R_1 + C_2 R_2 + C_C (G_m2 R_1 R_2 + R_1 + R_2)] + s^2 [C_1 C_2 + C_C (C_1 C_2 + C_C (C_1 + C_2))]} R_1 R_2$$

It is difficult to calculate an exactly same value in simulation result, for there are lots of effective resistance and effective capacitance in the circuit we ignore. Also, we ignore the imaginary part of poles and zeros. Consequently, the error would be large.

3.4 Open-loop common mode DC sweep

Fig. 3.4(a)

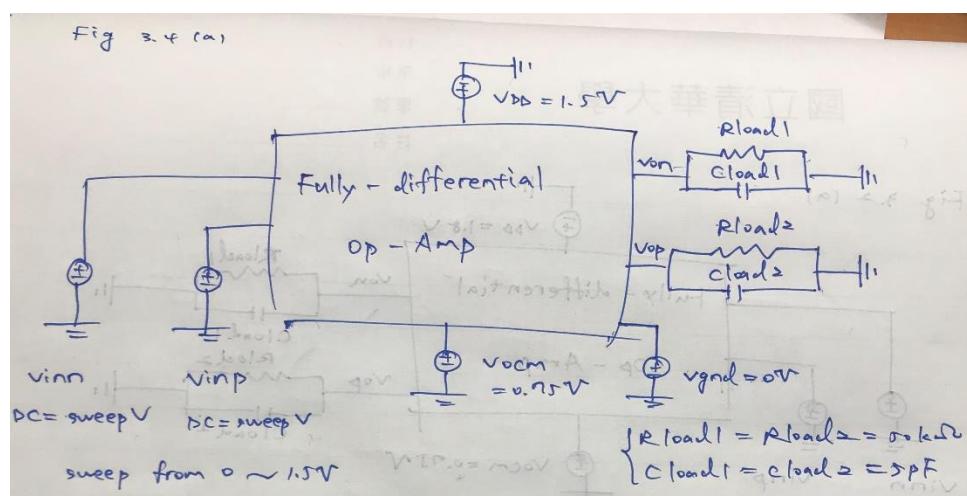
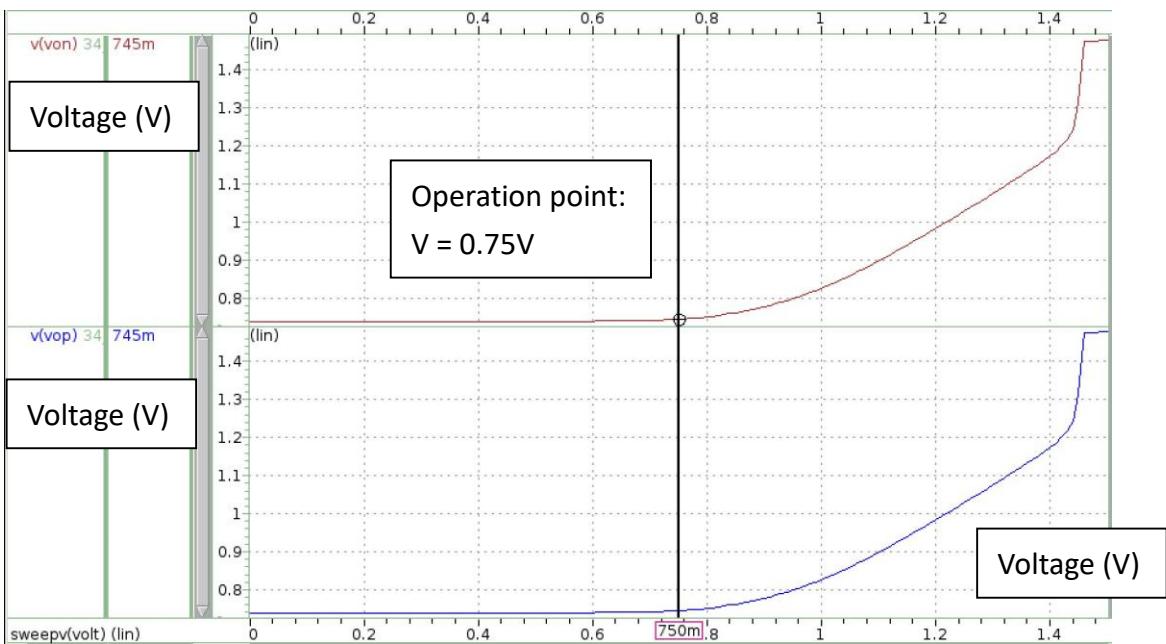


Fig. 3.4(b)



By the “equation builder”, I try to find the voltage gain by finding the slope in differential plot when x = common mode input voltage = 0.75V.
The result is shown below:

Mixed-Signal Equation Builder@ws47				
	Name	Equation (click here to edit min/max)	Target	Result
<input checked="" type="checkbox"/>	slope(v(vop),0.75)		D0/34_dc-cm.sw0	0.078392 X
	Input new equation here			

The .lis result is -21.417dB, and the DC slope is $0.078392 = -22.1146$ dB.
Difference = 3.26%. we could find that the results are quite same.

3.5 Open-loop power supply + AC response

Fig. 3.5(a)

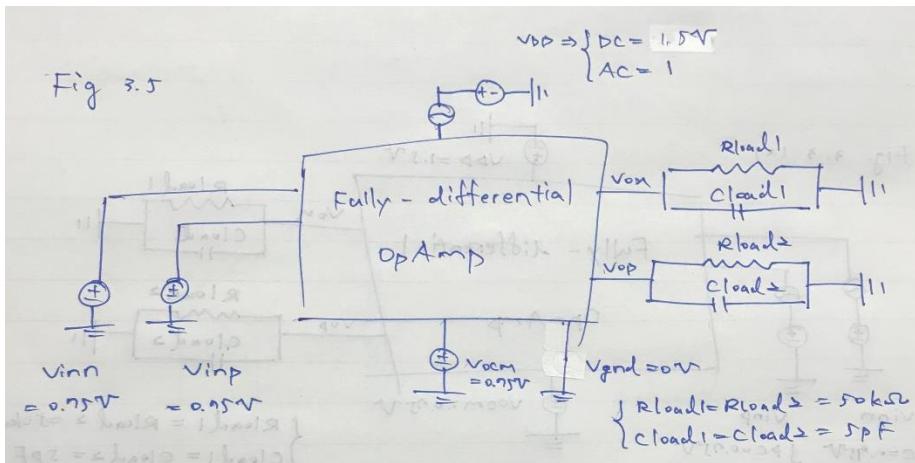
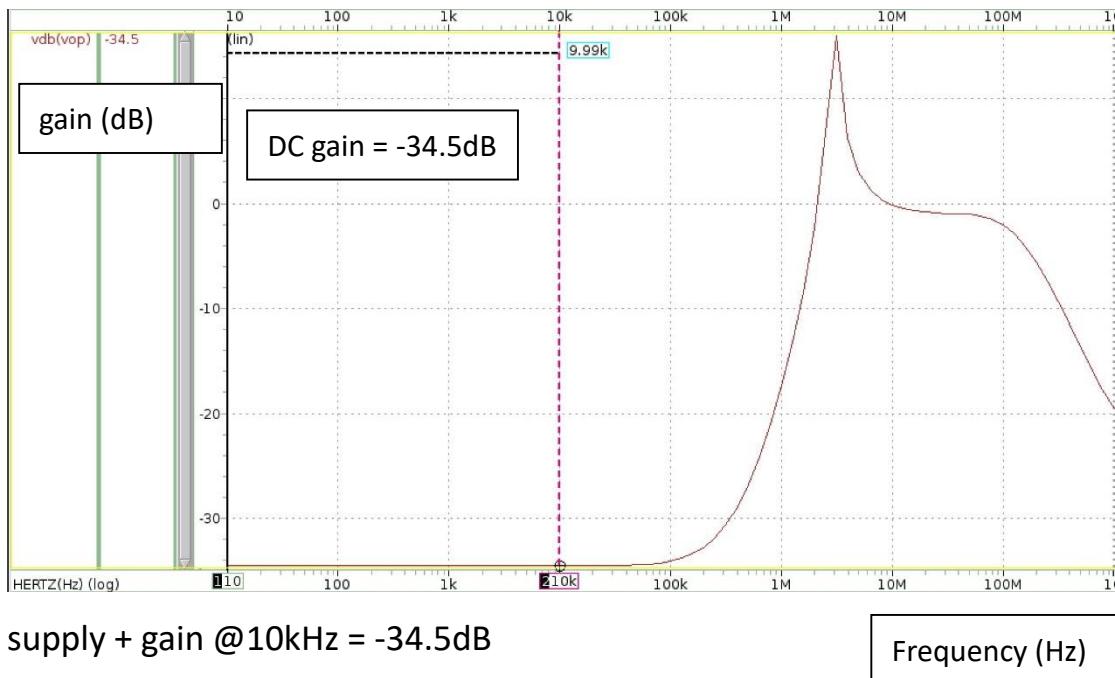
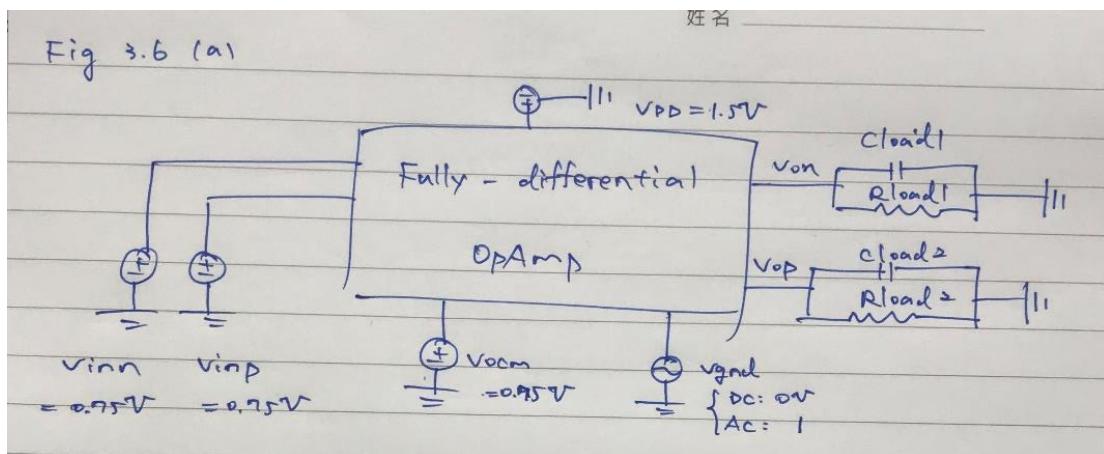


Fig. 3.5(b)



3.6 Open-loop power supply – AC response

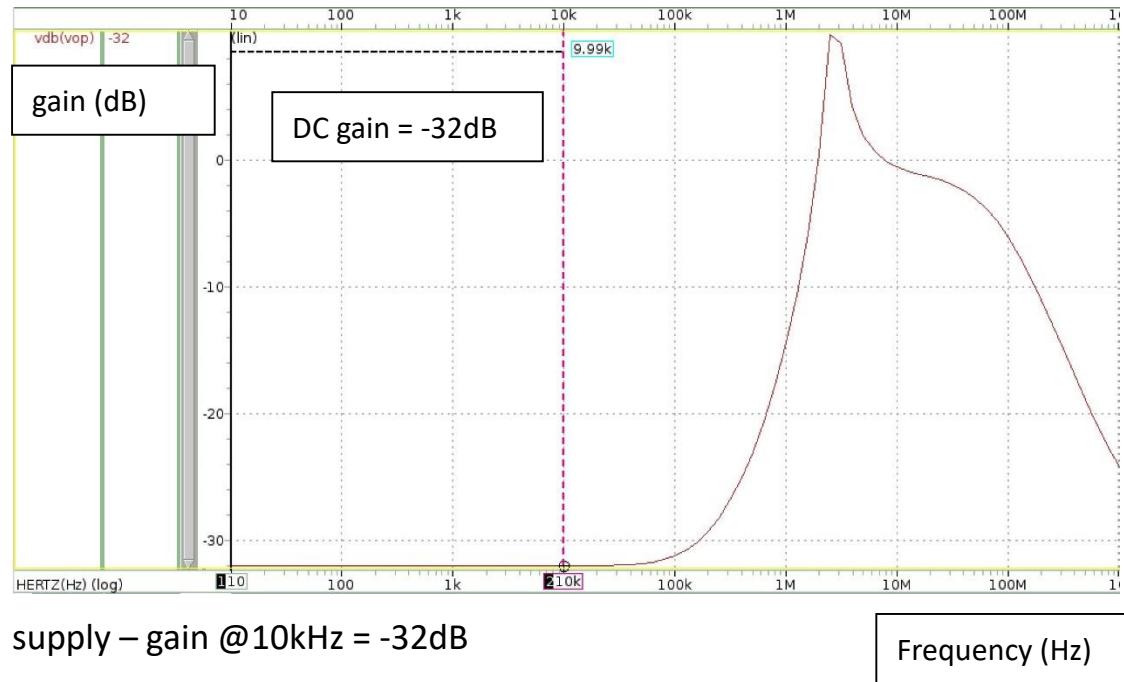
Fig. 3.6(a)



$$R_{load1} = R_{load2} = 50\text{k}\Omega$$

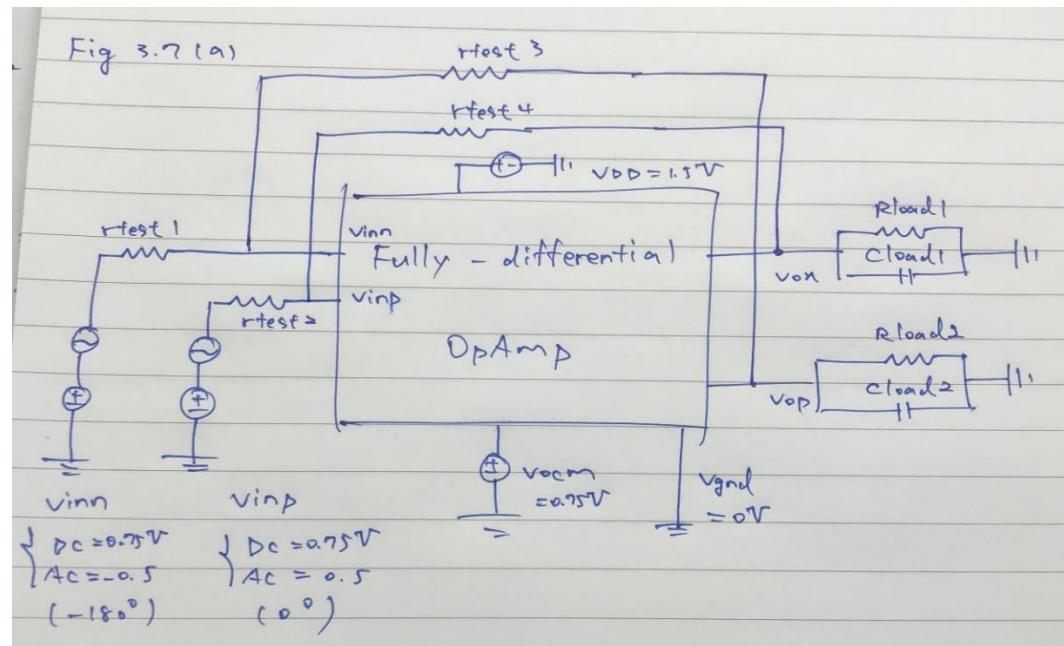
$$C_{load1} = C_{load2} = 5\text{pF}$$

Fig. 3.6(b)



3.7 Closed-loop differential mode AC response

Fig. 3.7(a)



$$r_{test1} = r_{test2} = r_{test3} = r_{test4} = 500\text{Kohm}$$

$$R_{load1} = R_{load2} = 50\text{kohm}$$

$$C_{load1} = C_{load2} = 5\text{pF}$$

Fig. 3.7(b)

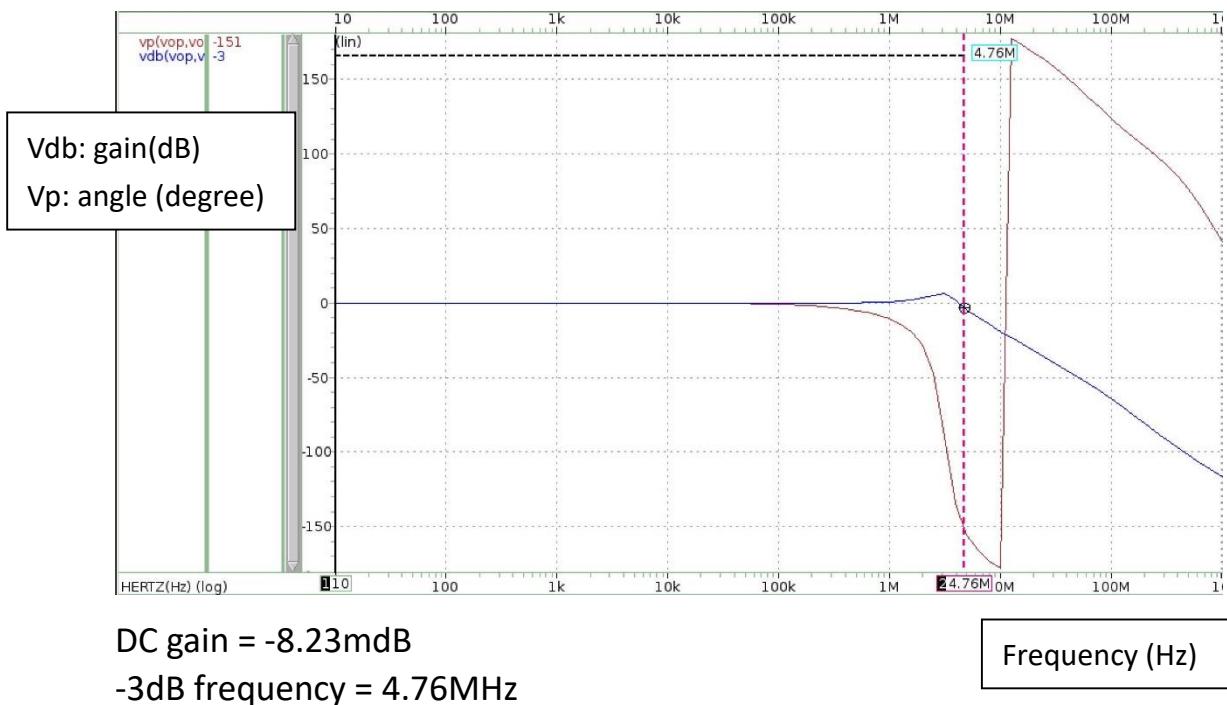


Fig. 3.7(c)

```
***** operating point information tnom= 25.000 temp= 25.000 *****
***** operating point status is all simulation time is 0.
      node      =voltage      node      =voltage      node      =voltage
+0:test1    = 750.0000m 0:test2    = 750.0000m 0:vdd      = 1.5000
+0:vinn     = 747.2353m 0:vinp     = 747.2353m 0:vocm     = 750.0000m
+0:von      = 744.4706m 0:vop      = 744.4706m 0:vss      = 0.
+1:b1       = 409.8101m 1:b2       = 836.3026m 1:f2       = 744.4706m
+1:f3       = 390.9891m 1:f4       = 397.2157m 1:f5       = 1.2998
+1:n1       = 434.8328m 1:n2       = 1.3289   1:n4       = 434.8328m
+1:rcl      = 744.4706m 1:rc2      = 744.4706m
```

By the picture as above, we could find that von/vinn = -(744.4706mV / 747.2353mV) = -0.9963 which is approaches to -1.

Fig. 3.7(d)

**** small-signal transfer characteristics

v(vop,von)/vinn	= -999.0530m
input resistance at vinn	= 676.4273k
output resistance at v(vop,von)	= 27.0228

Dis. 3.7(e)

In the simulation, we could find that the input impedance is quite large, and the output impedance is quite small. This condition is quite same as the ideal case (Z_{in} is quite large, Z_{out} is quite small). Consequently, we could know that this result makes sense.

3.8 Closed-loop differential mode DC sweep

Fig. 3.8(a)

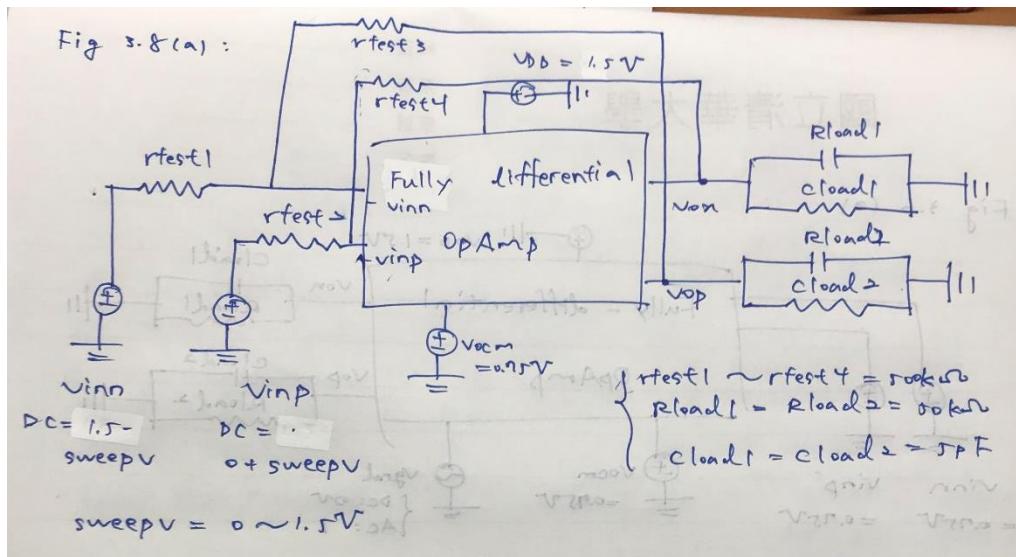
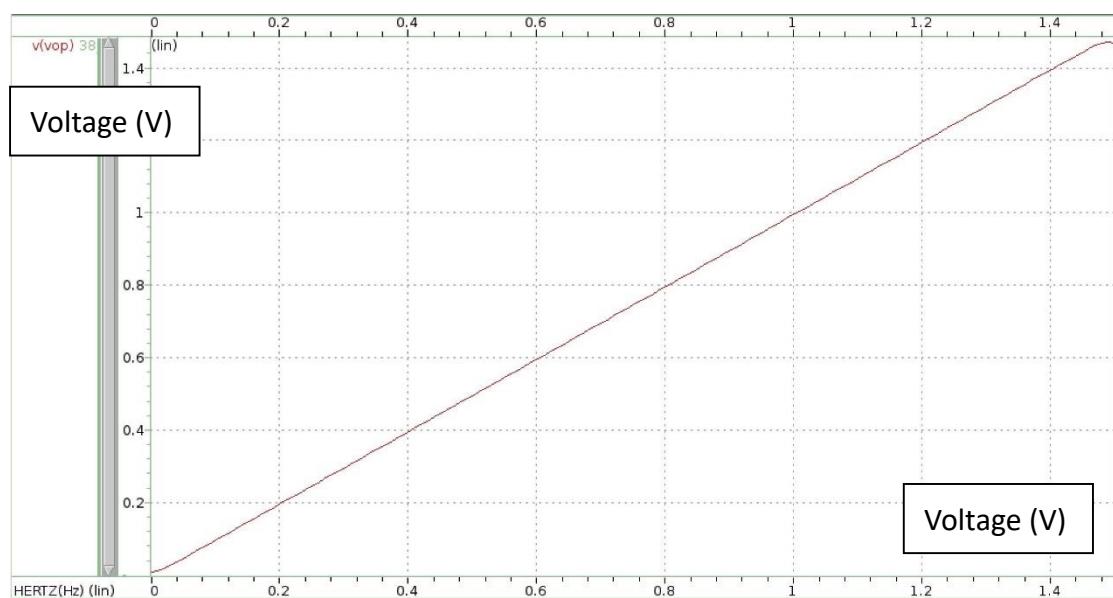
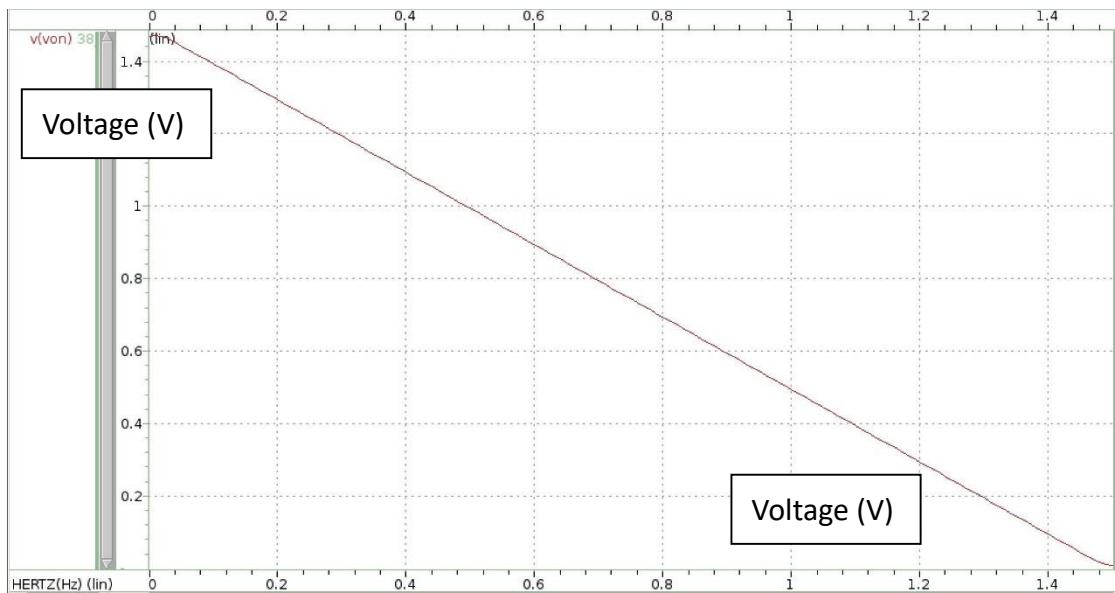


Fig. 3.8(b)

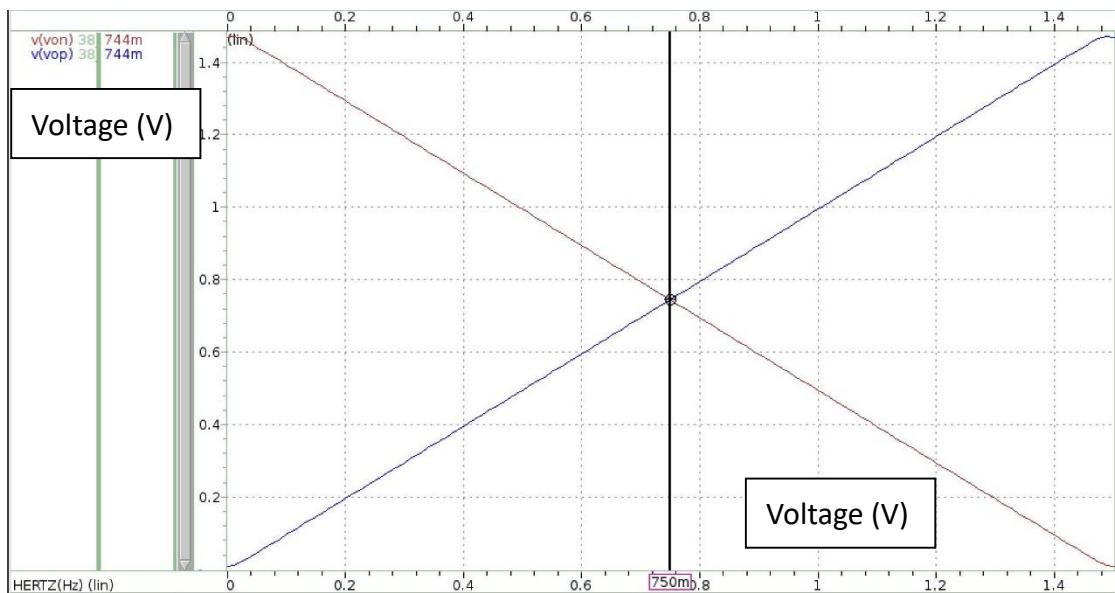
Single-ended: (Vop)



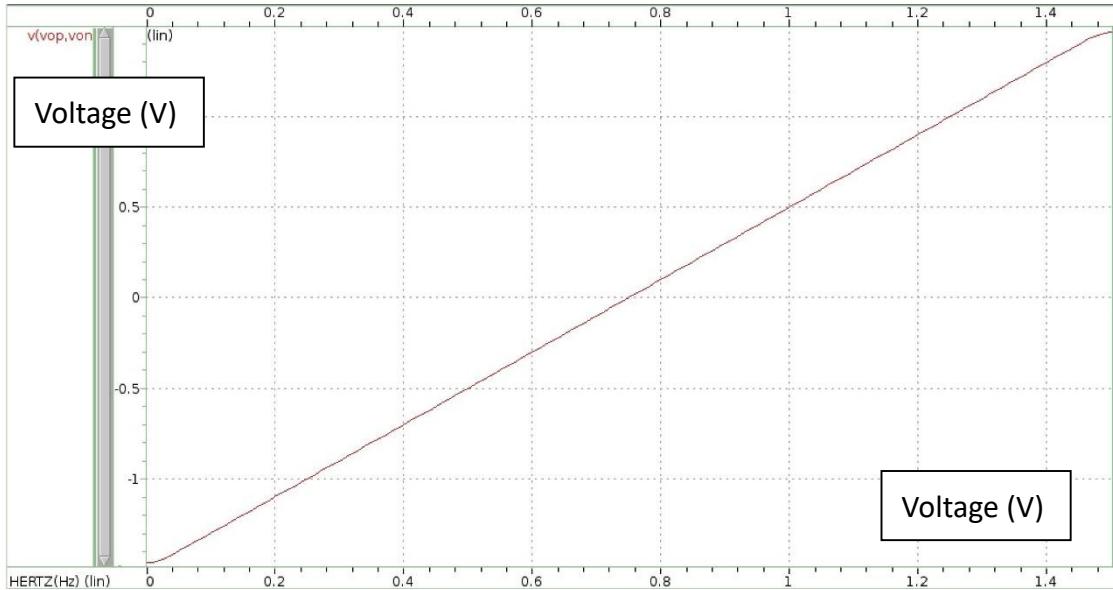
Single-ended: (Von)



Single-ended combination:



Differential:



By the “equation builder”, I try to find the voltage gain by finding the slope in differential plot when $x = \text{common mode input voltage} = 0.75\text{V}$. The result is shown below:

<input checked="" type="checkbox"/>	Name	Equation (click here to edit min/max)	Target	Result	
<input type="checkbox"/>	slope(v(vop),0.75)	D0/38_closed-dc_dm.sw0		0.999051	
	Input new equation here				

The .lis result is 0.999, and the DC slope is 0.999. Difference is equal to 0%. We could find that they are exactly same!

3.9 Closed-loop step +response

Fig. 3.9(a)

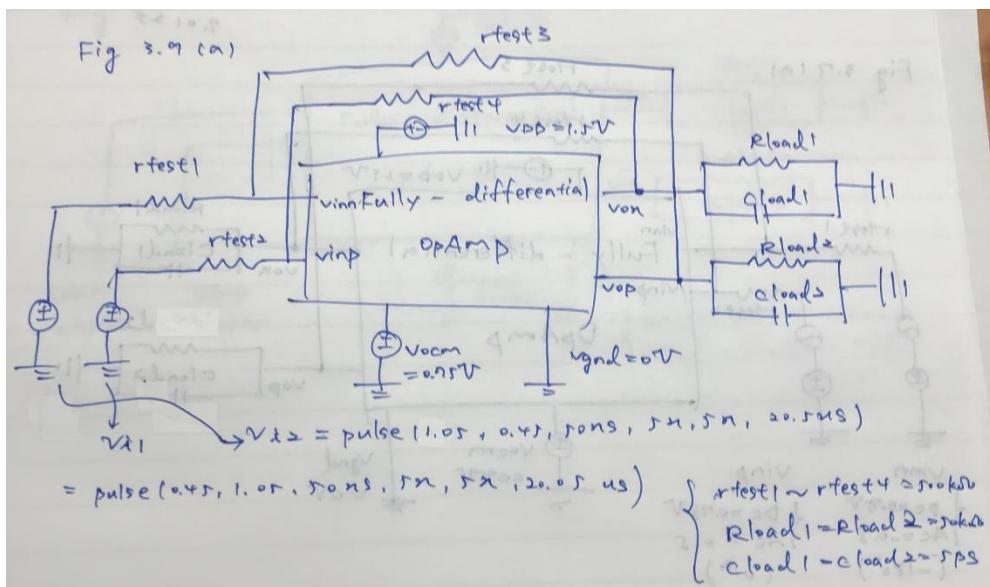
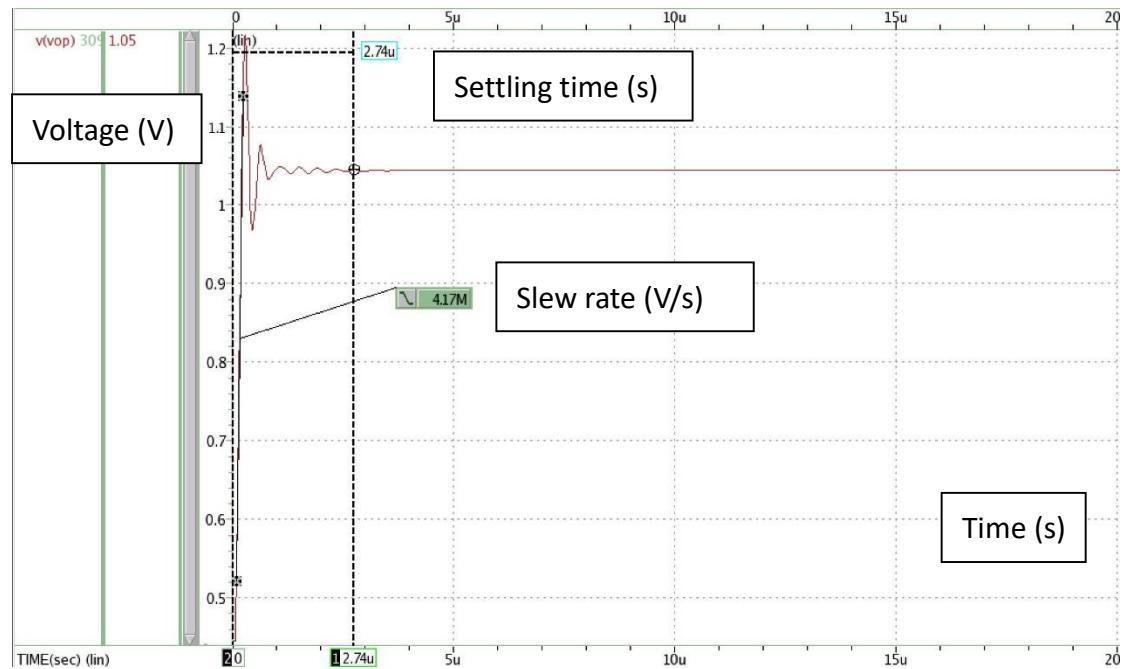


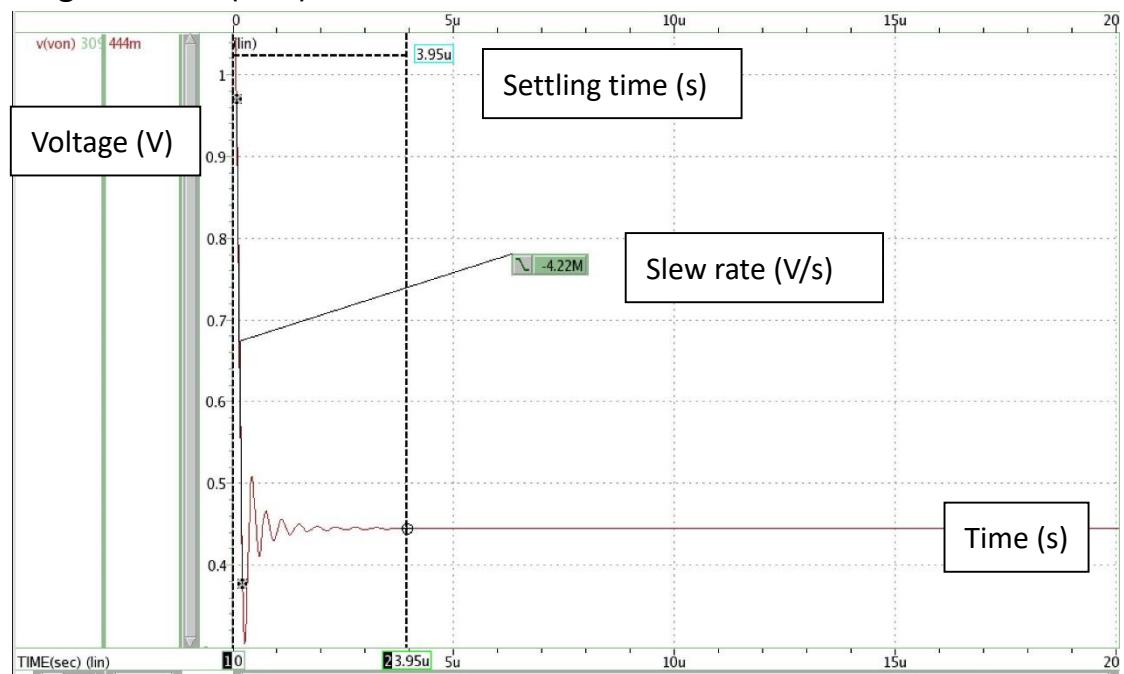
Fig. 3.9(b)

Fig. 3.9(c)

Single-ended: (V_{op})



Single-ended: (V_{on})



Differential:

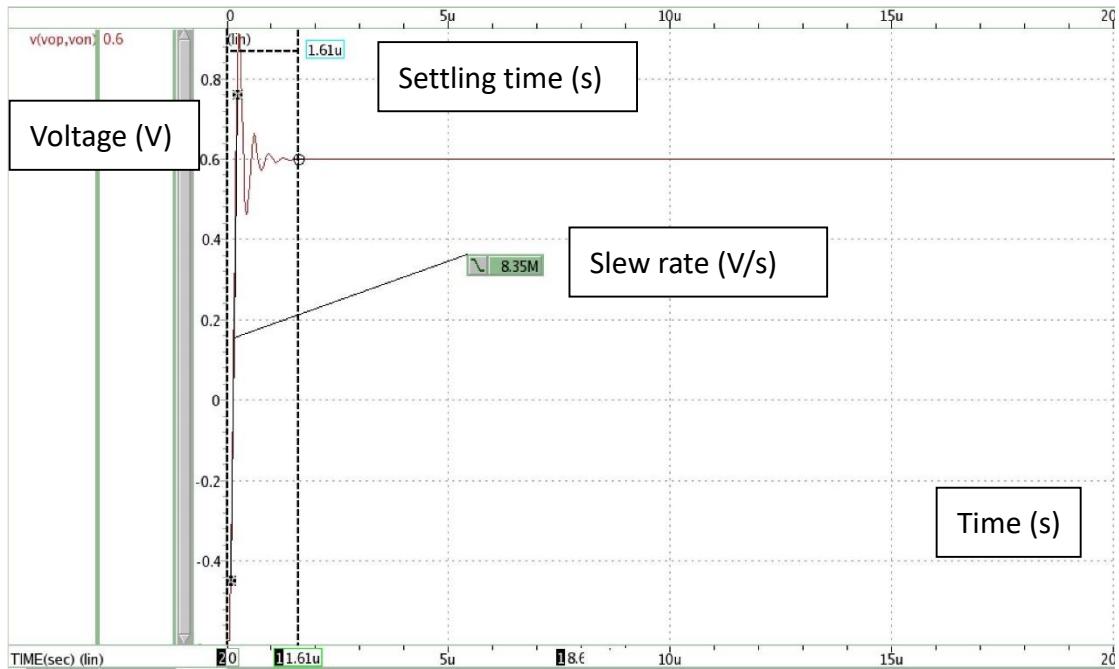


Fig. 3.9(d)

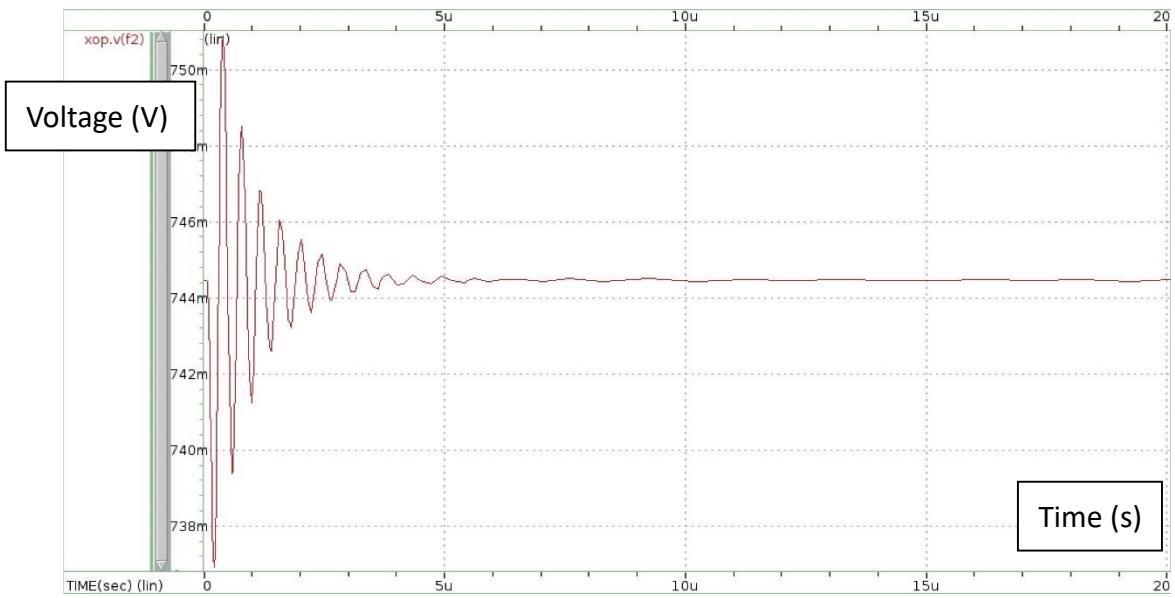


Fig. 3.9(e)

In the beginning, the waveform of voltage is oscillating, however, with the time goes through, the voltage becomes more and more stable and approaches to a constant.

The higher the rate is, the better the design is; also, the less the settling time is, the faster the voltage becomes stable.

3.10 Closed-loop step – response

Fig. 3.10(a)

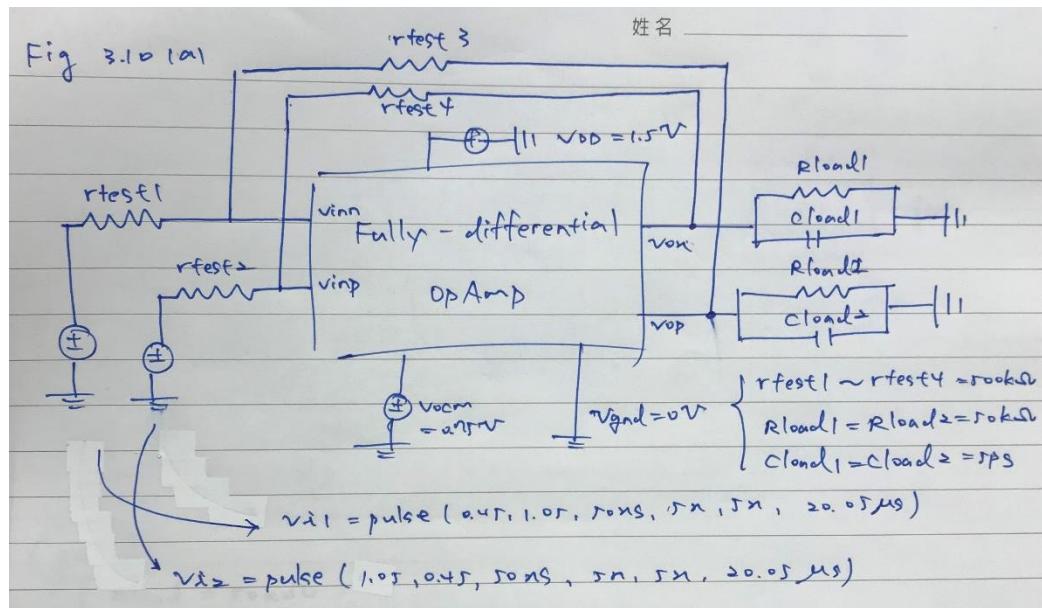
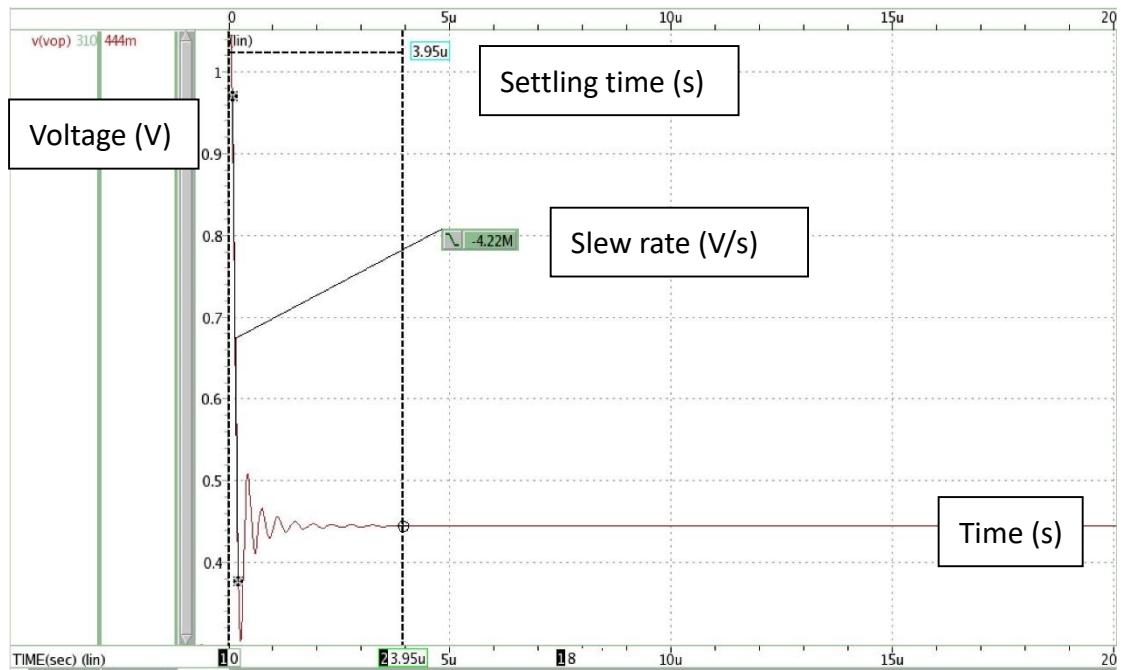


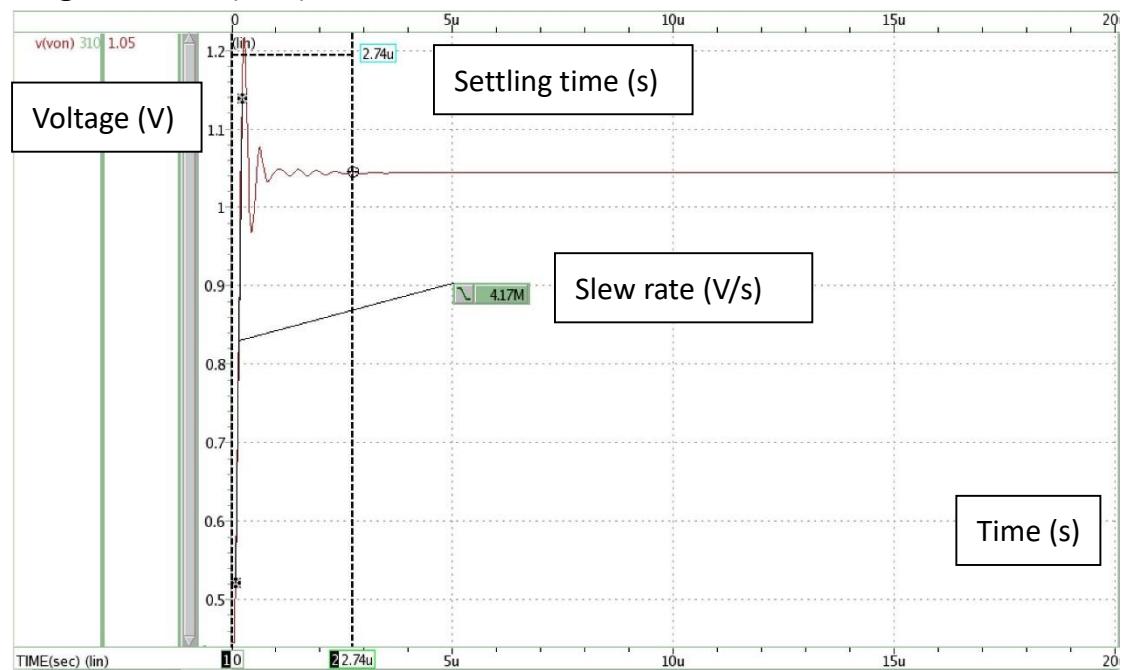
Fig. 3.10(b)

Fig. 3.10(c)

Single-ended: (V_{OP})



Single-ended: (V_{on})



Differential:

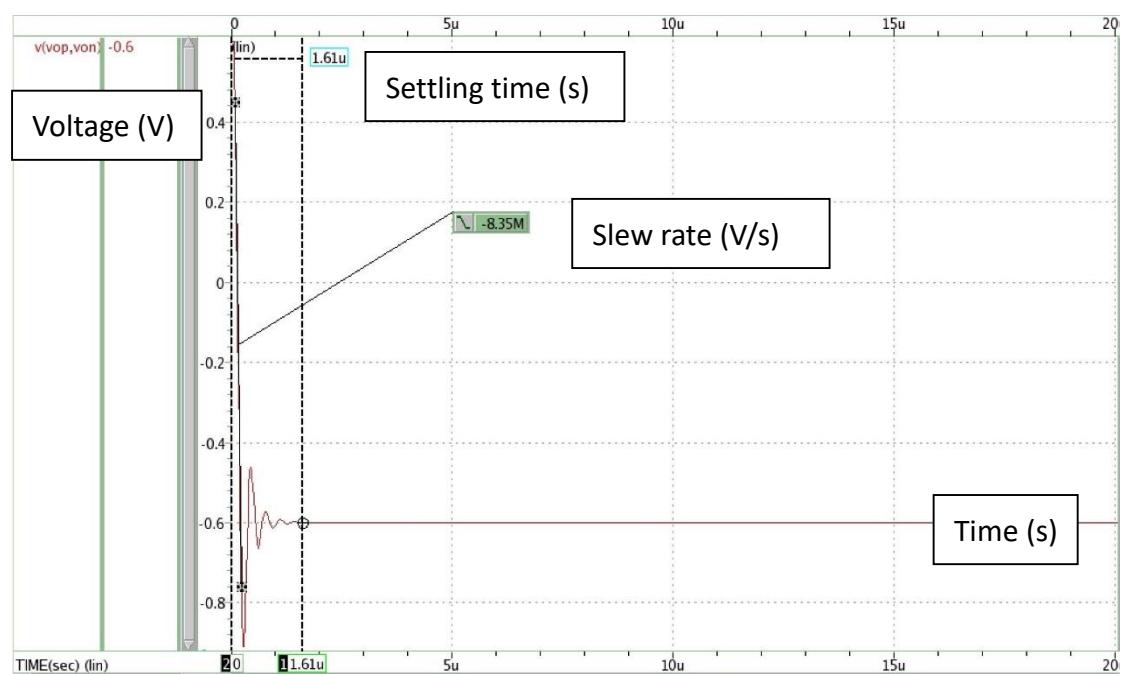
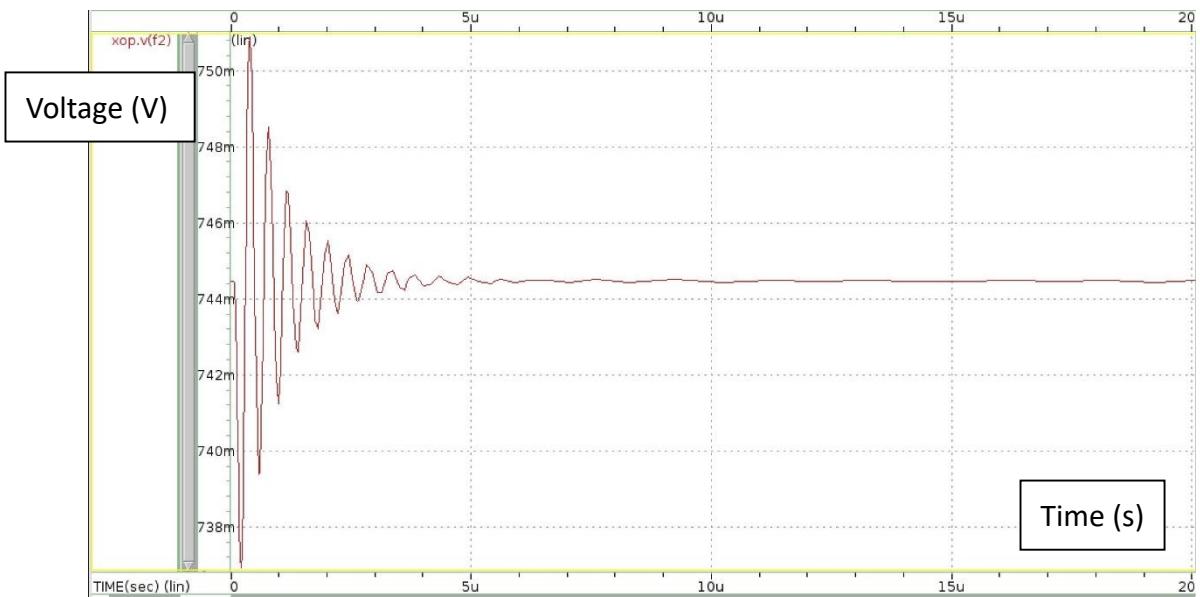


Fig. 3.10(d)



4. Performance Table

Design Items	Specifications	My Work
Technology	CIC pseudo 0.18um technology	
Supply voltage	1.5V , as small as possible	1.5V
Vicm, Vocm	0.75V / 0.75V	0.75V/0.75V
Supply current	< 5mA , as small as possible	1.2884mA
Loading	5pF / 50KΩ (for each output)	5pF/50Kohm
Compensation R, C,	Open for design	4pF/0.5Kohm
Open-loop simulation		
DC gain	> 60dB , as large as possible	66.7392
G-BW	> 1MHz , as large as possible	11.8176 MHz
P.M.	> 45 °	79.9779 °
C.M.R.R. @10KHz	>80dB	88.897dB
P.S.R.R. + @10KHz	> 80dB	101.256dB
P.S.R.R. - @10KHz	> 80dB	98.746dB
Closed-loop simulation		

Differential swing of 1.2V (step signal)		
S.R.+ (10% ~ 90%)	> 1 V/us	8.35V/us
S.R.- (90% ~ 10%)	> 1 V/us	-8.35V/us
Settling+ (to 0.1%)	< 10 us	1.6116us
Settling- (to 0.1%)	< 10 us	1.6116us
FoM		
Small signal	GBW (MHz) x CL (pF) / Power (mW)	25.487
Large signal +	SR+ (V/us) x CL (pF) / Power (mW)	18.008
Large signal -	SR- (V/us) x CL (pF) / Power (mW)	18.008

name	Total I < 5mA	Rcompensation Kohm	Ccompensation < 10pF	Av > 60dB	Unity-GBW > 1MHz	PM > 45	Aclose near -1	SR+ V/us	SR- V/us	settling ns	FoM1	FoM2	FoM3
柳奕丞	1.288	100	4	66.7392	11.8176	79.9779	-0.999	8.35	8.35	6240	25.4865424	18.008109	18.008109

5. Design Concerns

When designing my circuit, I tried to increase the voltage gain by increasing current flows through the amplifier circuit. Obviously, we need to adjust the MOSFET sizes in bias circuit. Since I couldn't decide a proper resister above MB1 in the beginning, so I appended a current source at the top of MB1 to test what amount of current I need. After all the other MOS is designed, then I can remove the current source and adjust the resistance to achieve same drain current as previous. Moreover, we need to consider the headroom problem at MB3, M5, M7, and M9. Consequently, I made the size ratio of MB2 is larger than the one of MB1 to supply adequate current to M5, M7, M9. Afterward, I decreased the size ratio of MB3 so that the vgs in M5, M7, M9 could be reduced and generated more drain current (by the current mirror). By doing so, I could prevent them from being in linear region. In phase margin part, we need to adjust the capacitor (CC1, CC2) and resistor (RZ1, RZ2) to achieve enough phase margin. If I increase the capacitance, the phase margin and voltage gain will become larger though, but the unity-gain frequency will decrease and the power consumption will increase. Moreover, if I increase resistance, the unity-gain frequency will increase significantly, but the phase margin will become smaller. Consequently, I need to design the capacitance and resistance carefully by the concerns above.

Also, I design the transconductance at the first level is smaller than the one at the second level. By doing so, I could obtain a more stable system.

Since the voltage and current of feedback circuit are supplied by amplifier circuit and bias circuit, so I decided to design it later than the other two circuits. If the amplifier circuit and bias circuit are designed well, then it is easy to make all the MOSFET in feedback circuit be in saturation region.

6. Discussion

At first, I had no idea where to change the size first, and I try to alter the ones with no analysis. Obviously, I failed then. In order to make all the MOSFET in saturation region, I tried to analyze the characteristic of each part of circuit (bias, amplifier, feedback), and I altered the sizes of MOSFET in bias circuit first.

First, I tried to alter the sizes in bias circuit to supply adequate amount of current to other parts, then I changes the sizes of M5, M7, and M9 to ensure that they can supply enough current to prevent the MOSFET below being in cutoff. After settling proper sizes of M5, M7, and M9, I started to change the sizes of MOSFET below to ensure all the one is in saturation. After doing so, design of the bias circuit and the amplifier circuit are accomplished.

Second, the altering method in feedback circuit is quite similar to the previous method, I tried to adjust the MF5 to ensure that it can supply enough current to prevent the MOSFET below being in cutoff. After doing so, I changed the sizes of MOSFET below to make all the MOSFET below be in saturation region. If all the step above is accomplished, then the design of fully differential circuit is accomplished.

In the design process, my first design couldn't achieve 60dB, after I changed the sizes in two stages (especially stage 2). Finally, my final design is around 66dB and met the specification. In addition, I first set a random value to compensation resistance and capacitance (take loading resistor and capacitor for reference). When I finished designing my circuit and do my report for a while, I found that I can change the compensation resistance and capacitance to achieve higher unity-gain frequency. However, the deadline was close and had no time to fixed all of the parameters and fixed my previous report, so it was a pity that I

forgot to change the value of compensation resistance and capacitance again to achieve better performance.

課程心得與建議：

這門課是未來從事類比 IC 設計的入門課程，雖然平時在寫作業的時候常常需要花很長時間調整每個 MOSFET 的 size，希望可以達到題目要求的 specification，甚至希望可以有更好的 FOM，但在這個過程中著實學習到設計簡單 AIC circuit 的實務經驗，了解遇到一個電路該如何從各個角度進行分析，確保可以有一個性能良好的電路供大家使用，我認為這段經驗將有助於自己未來從事相關工作。另外，這門課是電子學的延伸，內容前半部大致上是複習，與電子學大同小異，但在學期後半部開始講到 OpAmp 的設計以及 Feedback 機制，對我來說就是一個新的領域，而內容也是我特別感興趣的一環，可以了解到實務工作上是如何看更細微的參數進行分析、評估電路設計優劣，並且在放大倍率有限的狀況下如何加上好幾級電路讓 voltage gain 上升數十倍，這部分讓我著實感到驚奇！

對於課程建議部分，個人會希望以後可以在作業的 FOM 設一個 baseline，雖然自己認為用 competition 的立意良好，迫使我們思考更多方式增加題目要觀察的 FOM，但因為時間有限，這個過程變成沒有盡頭，再加上有其他科目的壓力，可能很難有辦法把全部時間都花在設計 AIC 電路上。

這學期謝謝老師和助教！老師在教學方面認真，除了補齊我在以前電子學沒有學好的部分，並在後面的 **topic** 更深入了解類比電路設計所需考慮的因素，我認為相當實用！在助教時間詢問助教問題時也相當有幫助，可以確切了解自己的問題所在，在討論區也可以解決作業上遇到的疑難雜症。這學期真的很謝謝您們！

Hspice code:

*** Final ***

.subckt my_op vinp vinn vdd vss vop von vocm

*** Bias Circuit ***

MB1 B1 B1 vss vss n_18 w = 70u l = 1u m = 2

MB2 B2 B1 vss vss n_18 w = 90u l = 0.8u m = 16

MB3 B2 B2 vdd vdd p_18 w = 80u l = 1u m = 10

Rb VDD B1 13.696k

*** Amplifier Circuit ***

M1 n1 vinp n2 vdd p_18 w = 80u l = 0.82u m = 1

M2 n4 vinn n2 vdd p_18 w = 80u l = 0.82u m = 1

M3 n1 F4 vss vss n_18 w = 40u l = 1u m = 1

M4 n4 F4 vss vss n_18 w = 40u l = 1u m = 1

M5 n2 B2 vdd vdd p_18 w = 12u l = 1u m = 3

M6 Von n4 vss vss n_18 w = 70u l = 0.6u m = 2

M7 Von B2 vdd vdd p_18 w = 50u l = 0.8u m = 2

M8 Vop n1 vss vss n_18 w = 70u l = 0.6u m = 2

M9 Vop B2 vdd vdd p_18 w = 50u l = 0.8u m = 2

*** Feedback Circuit ***

MF1 F3 vocm F5 vdd p_18 w = 80u l = 2u m = 6

MF2 F4 F2 F5 vdd p_18 w = 80u l = 2u m = 6

MF3 F3 F3 vss vss n_18 w = 40u l = 3u m = 2

MF4 F4 F4 vss vss n_18 w = 40u l = 3u m = 2

MF5 F5 B2 vdd vdd p_18 w = 20u l = 0.8u m = 2

*** passive component ***

RZ1 Vop rc1 0.5k

RZ2 rc2 Von 0.5k

RCM1 Vop F2 100k

RCM2 F2 Von 100k

CC1 rc1 n1 4p

CC2 n4 rc2 4p

.ends