ECE411 MP4 Presentation

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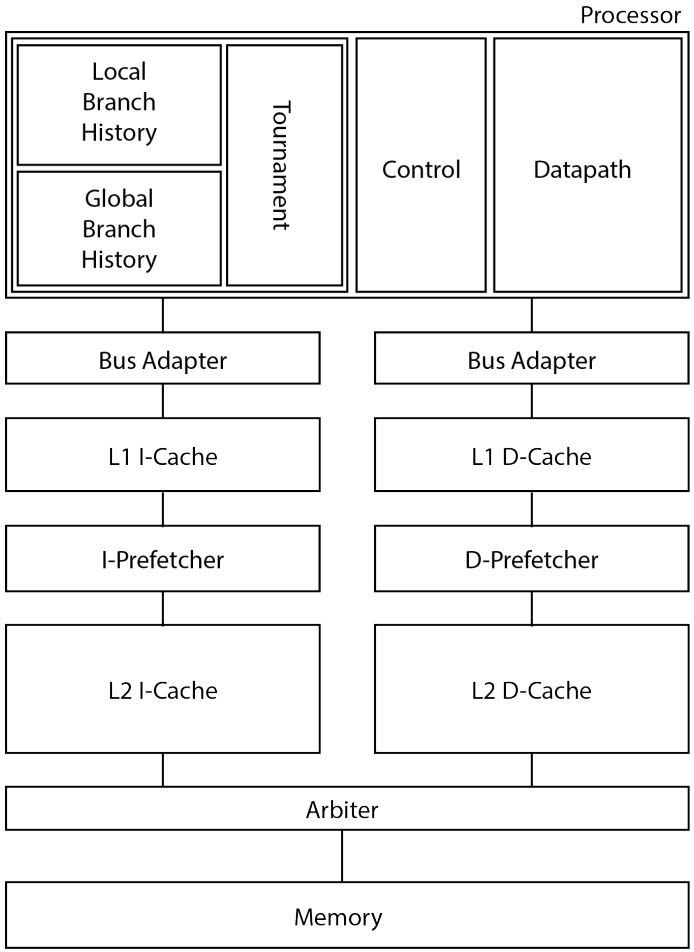
Overview

- 5-stage pipeline
  - forwarding and hazard detection
- Branch prediction
  - Local+ Global + Tournament
- Caches
  - 1- or 2-cycle hit
  - 2-, 4- or 8-way pseudo LRU
  - Fully parameterized
- Prefetch
  - Instructions and data



Single Parameterized Module

- Cacheline size
- Number of sets
- 2, 4 or 8 ways
- 1 or 2 response cycle

- BRAM for 2-cycle caches
- All parameterized into single module

```
module cache #(
    parameter s_offset   = 5,
    parameter s_index    = 3,
    parameter way_deg    = 1,
    parameter resp_cycle = 0
)
```

Cache Performance

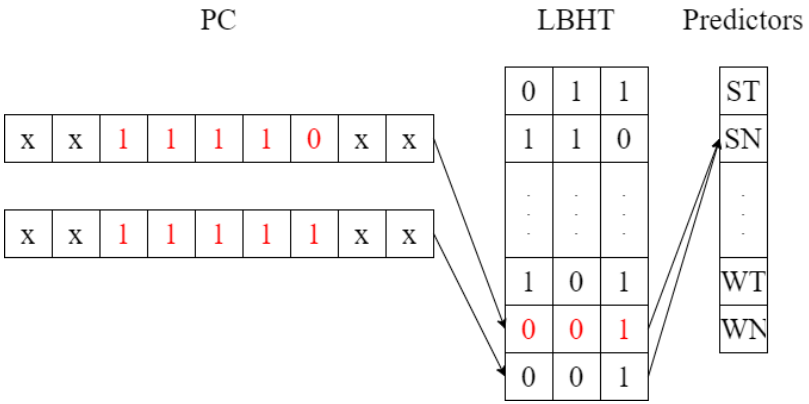
	mp4-cp3.s	comp1.s	comp2.s	comp3.s
L1 I-Cache				
L1 I-Cache Hit Rate	99.94%	95.75%	91.46%	91.46%
L2 I-Cache				
Speedup with L2 I-Cache	1.01	1.01	2.77	4.09
L1 D-Cache				
L1 D-Cache Hit Rate	99.75%	99.23%	97.93%	97.93%
L2 D-Cache				
Speedup with L2 D-Cache	2.72	1.00	1.01	0.99

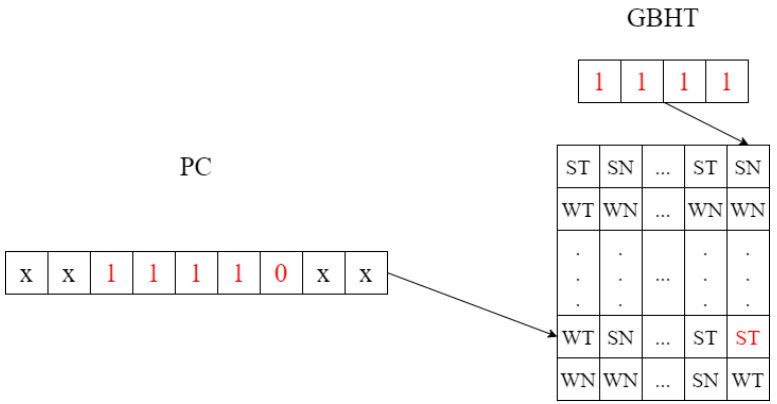
Branch Prediction

- Local Branch History Table
- Global Branch History Table
- Tournament Branch Prediction

Accuracy (%)	Average
Static Not-Taken	27.53
LBHT	87.29
GBHT	82.42
Tournament	88.83

Speedup	Average
LBHT	1.10
GBHT	1.08
Tournament	1.10





Prefetcher

- Located between L1 cache and L2 cache
- Two states: normal read and prefetch
- Block the new incoming read if prefetching is ongoing

Speedup	Average speedup compared with baseline*
Instruction Prefetcher Only	1.005968053
Data Prefetcher Only	1.032382609
Instruction and Data Prefetcher Together	1.038498598

*Baseline is our processor with all other advanced features enabled

Overall Performance

	mp4-cp3.s	comp1.s	comp2.s	comp3.s
Baseline		720755	4521285	3639265
Final Design	560220	422820	1032724	708804
Total Speedup		1.70	4.38	5.13

Logic utilization	87 %
Total registers	20017
Total pins	165 / 292 (57 %)
Total virtual pins	0
Total block memory bits	1,197,568 / 2,939,904 (41 %)

Fmax	Restricted Fmax	Clock Name	Note
107.74 MHz	107.74 MHz	clk	

Thanks!
Q&A