

## Bloc Teclat

The diagram illustrates the internal logic of the keyboard block. It features a 4x3 keypad matrix with columns labeled Column[2], Column[1], and Column[0], and rows labeled Row[0], Row[1], Row[2], and Row[3]. The keypad is connected to a 74LS191 Counter (U3) via a 74LS139 Decoder (U4:A). The counter's output (Q0-Q3) is connected to four NOT gates (U5, U6, U8, U9) to produce Row[0] through Row[3]. The counter is also connected to a 74LS161 Counter (U28) via a 74LS161 Counter (U31) and a 74LS161 Counter (U12) to produce End2sec and Reset2Sec signals.

### Bloc General

The diagram illustrates the general block structure of the circuit. It features a 555 timer (U18) configured as a monostable multivibrator. The trigger (pin 1) and ground (pin 5) are connected to ground. The reset (pin 4) is connected to VCC. The timing network consists of a resistor R11 (6.9k) and a capacitor C2 (10nF) connected to pins 6 and 7. The output (pin 3) is labeled 'Time'. A pull-up resistor R12 (69k) is connected between the output and VCC. A capacitor C4 (10nF) is connected to the output. A NOT gate (U42) is shown with input 'PCI' and output 'PCIReset'.

The diagram illustrates a memory system architecture. It features two 74LS157 4-to-1 multiplexers, U15 and U17, which are used to route data from a 27C256 EPROM to a set of LEDs. The EPROM is configured with its address lines (A0-A14) connected to the data inputs (D0-D14) of the multiplexers. The output of the multiplexers is connected to the LEDs. The system is controlled by a 74LS194 register, which provides a clock signal (CLK) to the multiplexers and a master reset signal (MR) to the EPROM. The EPROM is also connected to a 5V supply and ground. The LEDs are connected to a common ground and a 5V supply through current-limiting resistors.

## Bloc Intents

The diagram illustrates the internal logic of the 'Bloc Intents' block, which is composed of several integrated circuits (ICs) and logic gates.

**74LS95 (U2 and U19):** Two 74LS95 flip-flop chips are used. U2 is connected to the 'ResetTries' input (pin 6) and the 'TWasteTry' input (pin 9). U19 is connected to the 'ResetTries' input (pin 6) and the 'TWasteTry' input (pin 9). Both chips have their 'Q' outputs (Q0, Q1, Q2, Q3) connected to the 'Tries' outputs (Tries[9], Tries[8], Tries[7], Tries[6] for U2 and Tries[5], Tries[4], Tries[3], Tries[2] for U19).

**74LS109 (U14:A and U14:B):** Two 74LS109 flip-flop chips are used. U14:A is connected to the 'ResetTries' input (pin 5) and the 'TWasteTry' input (pin 4). U14:B is connected to the 'ResetTries' input (pin 5) and the 'TWasteTry' input (pin 12). Both chips have their 'Q' outputs (Q0, Q1, Q2, Q3) connected to the 'Tries' outputs (Tries[1], Tries[0] for U14:A and Tries[1], Tries[0] for U14:B).

**Logic Gates:**

- U16 (OR gate):** An OR gate with two inputs: 'PCI' and 'LoadTries'. Its output is 'ResetTries'.
- U20 (NOT gate):** A NOT gate with one input: 'Tries[0]'. Its output is 'GameOver'.

**Resistors:** A series of resistors (R3, R4, R13, R14, R15, R17, R18, R19, R20, R21) are connected to the 'Tries' outputs (Tries[9], Tries[8], Tries[7], Tries[6], Tries[5], Tries[4], Tries[3], Tries[2], Tries[1], Tries[0]) to provide a pull-up to the power supply.

### Bloc Número

The circuit diagram for the 'Bloc Número' (Number Block) is a complex digital logic design. It includes several 74LS109 counters, 74LS194 shift registers, 74LS273 registers, and various logic gates (AND, OR, NOR, NOT). The circuit manages game state including number generation, statistics display, and game over conditions. Key components include U27 (74LS85), U29:B (74LS109), U10:B (74LS109), U23 (74LS194), U24 (74LS194), U26 (74LS85), U29:A (74LS109), U39 (OR), U40 (NOR), U32:A (74LS109), U37 (NOR), U25 (74LS273), U33 (74LS273), U34 (74LS273), U22 (74LS194), and U41 (NOR). The circuit is interconnected with various inputs like PCI, TSetNumber, and outputs like NumberA[0-3], NumberB[0-3], and game status signals.